# 3A, 2MHz, Synchronous Step-Down Converter

## General Description

The RT8082 is a high efficiency synchronous, step-down DC/DC converter. Its input voltage range is from 2.7V to 5.5V and provides an adjustable regulated output voltage from 1V to 5V while delivering up to 3A of output current.

The internal synchronous low on-resistance power switches increase efficiency and eliminate the need for an external Schottky diode. The switching ripple voltage is easily smoothed-out by small package filtering elements due to a fixed operating frequency of 2MHz. The 100% duty cycle provides low dropout operation extending battery input range in portable systems. Current mode operation with external compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

The RT8082 operates in forced continuous PWM Mode, which minimizes ripple voltage and reduces the noise and RF interference.

## Ordering Information

RT8082 □□

- Package Type
  QW : WDFN-12E 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

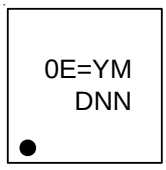
## Features

- **High Efficiency : Up to 95%**
- **2MHz Fixed Frequency PWM Operation**
- **No Schottky Diode Required**
- **1V Reference Allows Low Output Voltage**
- **Output Current up to 3A**
- **Forced Continuous Mode Operation**
- **Low Dropout Operation : 100% Duty Cycle**
- **Enable Function**
- **Power Good Function**
- **Internal Soft-Start**
- **RoHS Compliant and Halogen Free**

## Applications

- LCD TV and Monitor
- Notebook Computers
- Distributed Power Systems
- IP Phones
- Digital Cameras

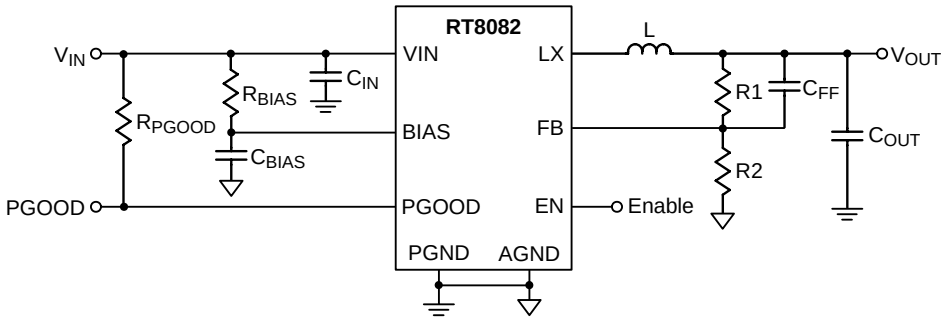
## Marking Information




0E= : Product Code

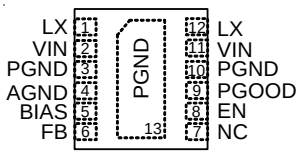
YMDNN : Date Code

## Simplified Application Circuit



## Pin Configurations

(TOP VIEW)

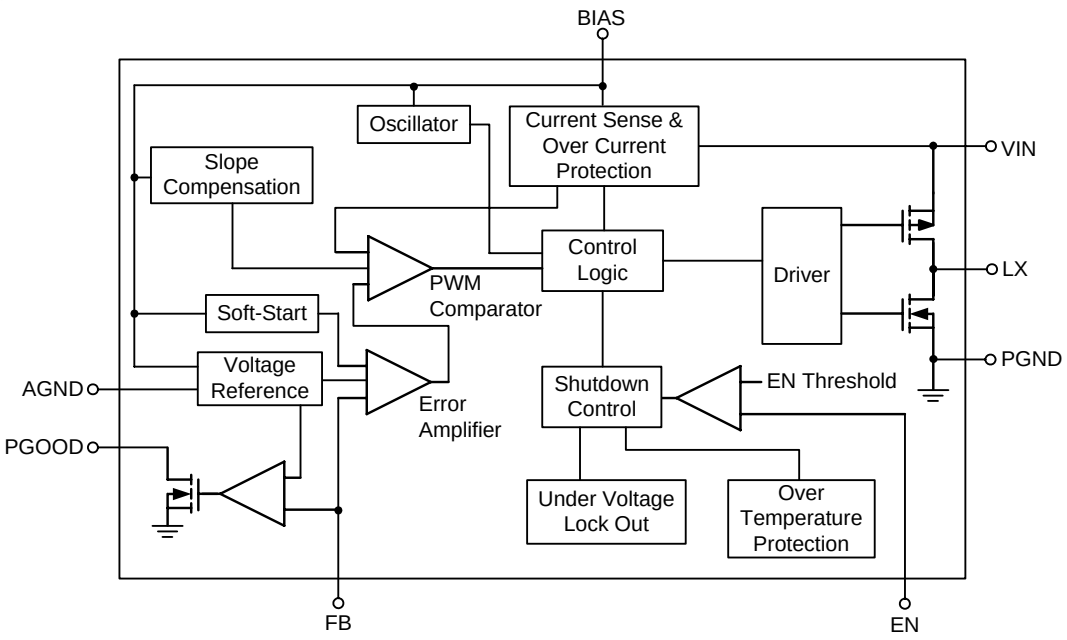



WDFN-12E 3x3

## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1, 12 | LX | Internal Power MOSFET Switches Output. Connect these pins to the inductor together. |
| 2, 11 | VIN | Power Input. Decouple this pin to GND with two 10μF capacitors. |
| 3, 10, 13 (Exposed Pad) | PGND | Power Ground. The exposed pad must be soldered to a large PCB and connected to ground for maximum power dissipation. |
| 4 | AGND | Analog Ground. Provides the return path for control circuit and internal reference. |
| 5 | BIAS | Analog Power Input. Decouple this pin to AGND with a minimum 0.1μF ceramic capacitor. |
| 6 | FB | Feedback Input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 1V typically. |
| 7 | NC | No Internal Connection. |
| 8 | EN | Enable Control Input. Floating this pin or connecting this pin to logic high will enable the device and pulling this pin to logic low will disable the device. |
| 9 | PGOOD | Power Good Indicator. This pin is an open drain logic output that is pulled to ground when the output voltage is within ±7% of regulation point. |

## Function Block Diagram




## Operation

During normal operation, the internal high side power switch (P-MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the peak inductor current reaches the value defined by the output voltage ($V_{COMP}$) of the error amplifier. The error amplifier adjusts its output voltage by comparing the feedback signal from a resistive voltage divider on the FB pin with an internal 1V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier increases its output voltage to allow the average inductor current traces the new load current. When the high side power MOSFET turns off, the low side power switch (N-MOSFET) turns on until the beginning of the next clock cycle.

## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN, BIAS ---------- –0.3V to 6V
- LX Pin Switch Voltage ---------- –0.3V to ($V_{IN}$ + 0.3V)
- Other Pins ---------- –0.3V to ($V_{IN}$ + 0.3V)
- LX Pin Switch Current ---------- 5A
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  WDFN-12E 3x3 ---------- 1.667W
- Package Thermal Resistance (Note 2)
  WDFN-12E 3x3, $\theta_{JA}$ ---------- 60°C/W
  WDFN-12E 3x3, $\theta_{JC}$ ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.7V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

## Electrical Characteristics

($V_{IN}$ = $V_{EN}$ = 3.6V, $T_A$ = –40°C to 85°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Quiescent Current | $I_Q$ | $V_{FB}$ = 0.9V, Not Switching | -- | 570 | 900 | μA |
| Shutdown Current | $I_{SHDN}$ | $V_{EN}$ = 0V | -- | 1 | 2 | μA |
| Feedback Voltage | $V_{FB}$ | $I_{LOAD}$ = 100mA | 0.98 | 1 | 1.02 | V |
| | | $I_{LOAD}$ = 100mA, $T_A$ = 25°C | 0.99 | 1 | 1.01 | |
| Feedback Leakage Current | $I_{FB}$ | | -- | 1 | -- | nA |
| Line Regulation | | $I_{LOAD}$ = 100mA | -- | 0.07 | -- | %/V |
| Load Regulation | | 20mA < $I_{LOAD}$ < 3A | -- | 0.2 | 0.5 | % |
| Switching Frequency | $f_{OSC}$ | | 1.7 | 2 | 2.3 | MHz |
| High Side Switch On-Resistance | $R_{DS(ON)\_P}$ | $I_{LX}$ = 0.5A | -- | 75 | 150 | mΩ |
| Low Side Switch On-Resistance | $R_{DS(ON)\_N}$ | | -- | 55 | 80 | |
| Peak Current Limit | $I_{LIM}$ | | 3.5 | 5 | -- | A |
| Under Voltage Lockout Threshold | $V_{UVLO}$ | $V_{IN}$ Rising | 2.35 | 2.45 | 2.6 | V |
| Under Voltage Lockout Hysteresis | $\Delta V_{UVLO}$ | | -- | 0.2 | -- | V |
| Power Good Rising Threshold | | $V_{FB}$ Rising (Good), $T_A$ = 25°C | -- | 93 | 90 | % |
| | | $V_{FB}$ Rising (Fault), $T_A$ = 25°C | -- | 107 | 110 | |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Good Falling Threshold | | $V_{FB}$ Falling (Fault), $T_A$ = 25°C | -- | 93 | 90 | % |
| | | $V_{FB}$ Falling (Good), $T_A$ = 25°C | -- | 107 | 110 | |
| Power Good Resistance | | $I_{PGOOD}$ = 500μA | -- | 145 | 250 | Ω |
| Enable Threshold Voltage | | EN Rising | 0.5 | 0.85 | 1.3 | V |
| Enable Voltage Hysteresis | | | -- | 50 | -- | mV |
| Enable Input Current | | | -- | 0.1 | 2 | μA |
| Over Temperature Protection | | | -- | 160 | -- | °C |
| Over Temperature Protection Hysteresis | | | -- | 20 | -- | °C |

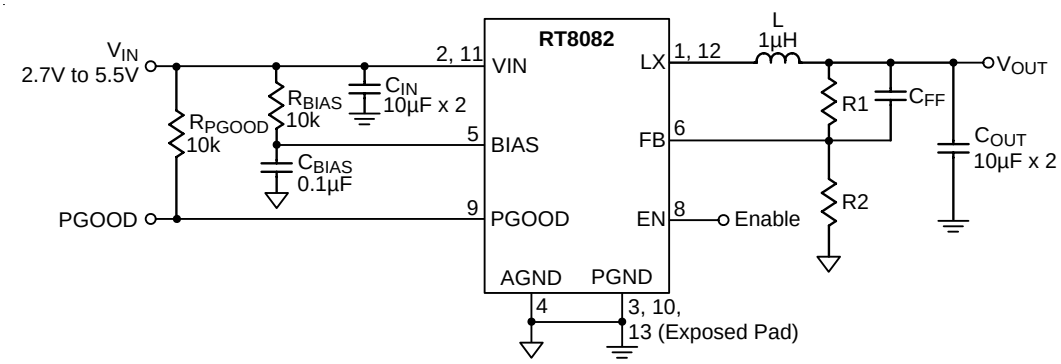
**Note 1.** Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** $\theta_{JA}$ is measured at $T_A$ = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. $\theta_{JC}$ is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Typical Application Circuit

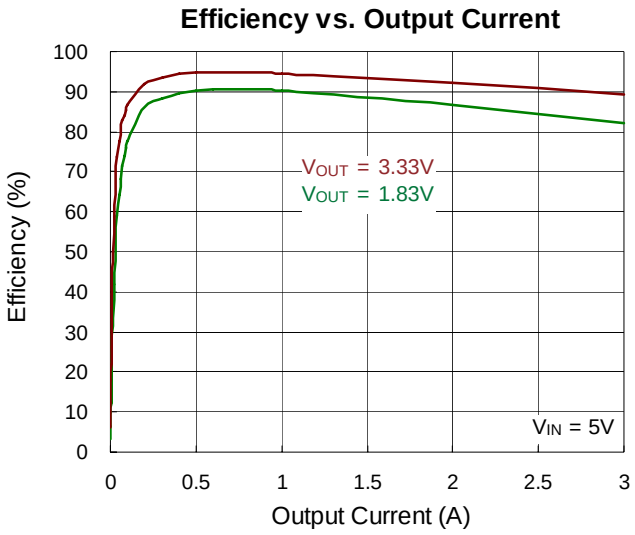


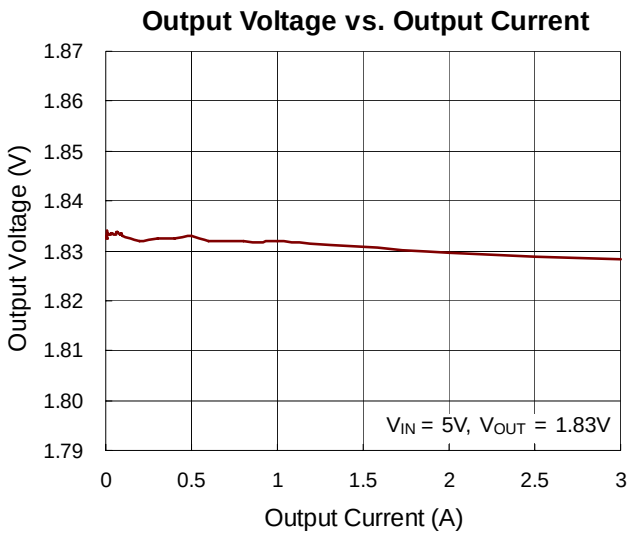

**Note : Using all Ceramic Capacitors**

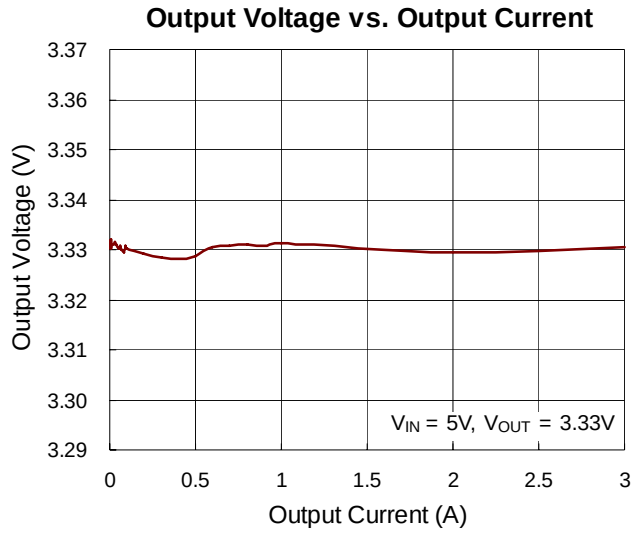
**Table 1. Suggested Components Selection**

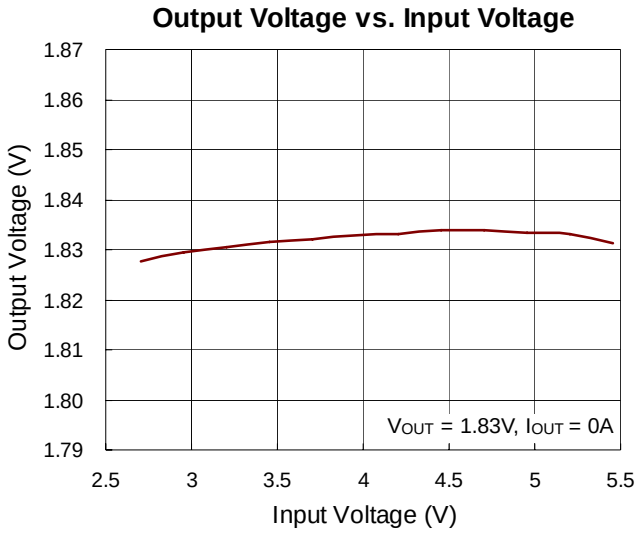
| $V_{OUT}$ (V) | R1 (kΩ) | R2 (kΩ) | $C_{FF}$ (pF) | L (µH) | $C_{OUT}$ (µF) |
|---|---|---|---|---|---|
| 3.3 | 27.6 | 12 | 82 | 2 | 10 x 2 |
| 2.5 | 18 | 12 | 330 | 1.5 | 10 x 2 |
| 1.8 | 9.6 | 12 | 150 | 1 | 10 x 2 |
| 1.5 | 6 | 12 | Open | 1 | 10 x 2 |
| 1.2 | 6 | 30 | Open | 1 | 10 x 2 |
| 1.0 | 0 | Open | Open | 1 | 10 x 2 |

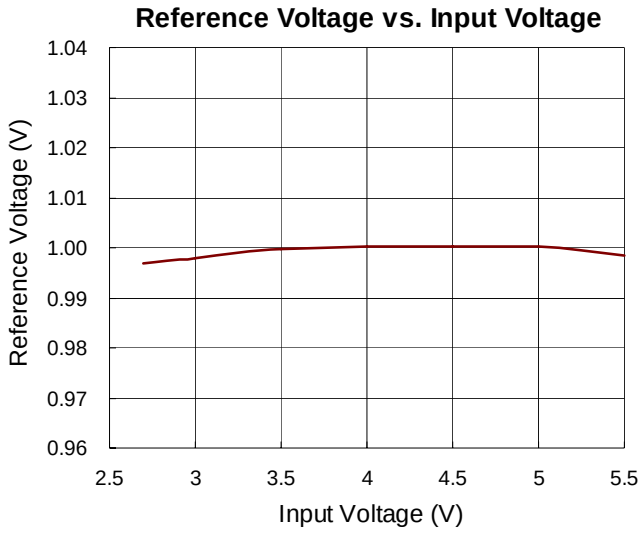
## Typical Operating Characteristics

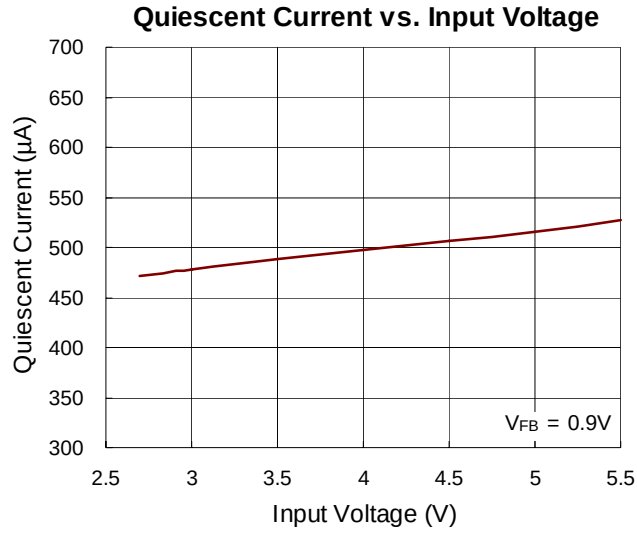


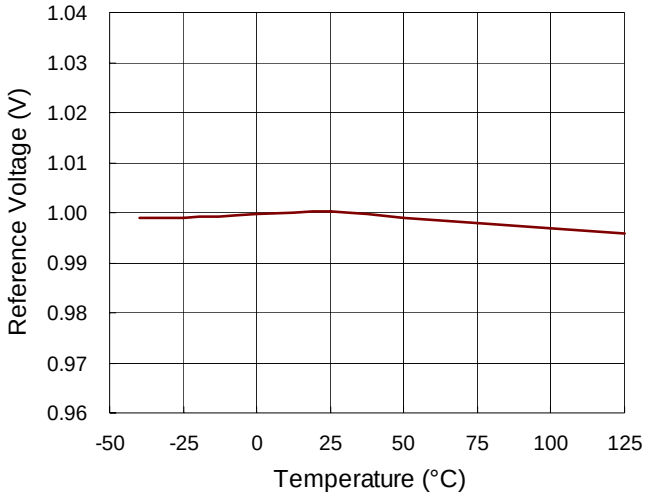



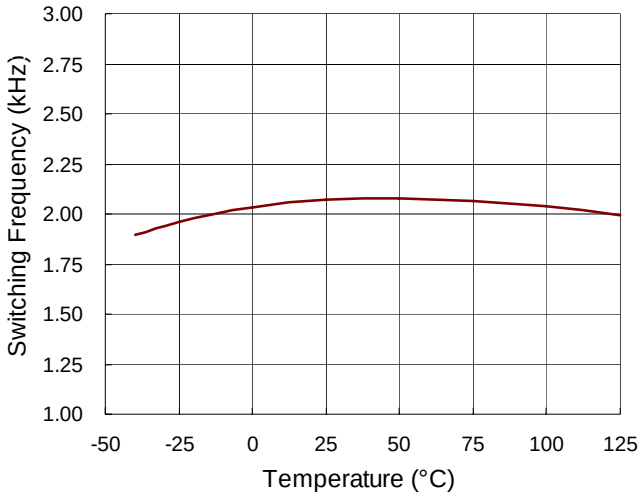



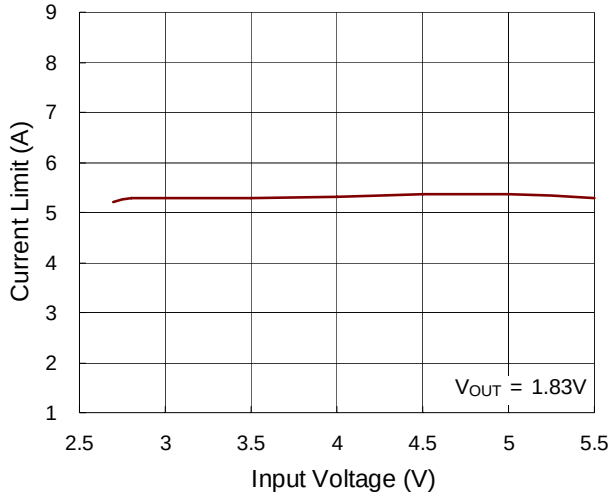
### Reference Voltage vs. Temperature



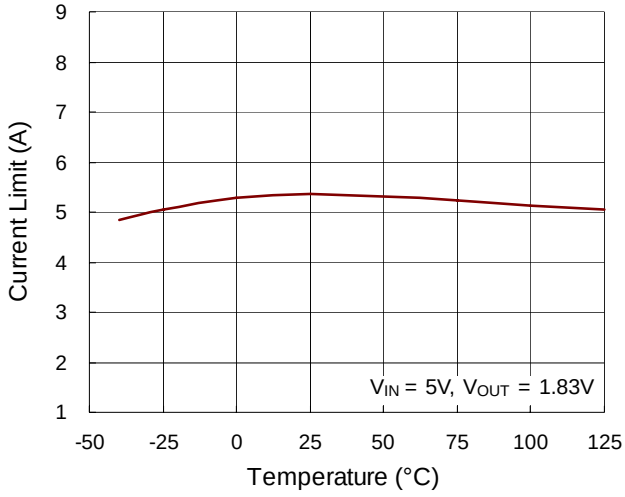

### Switching Frequency vs. Temperature



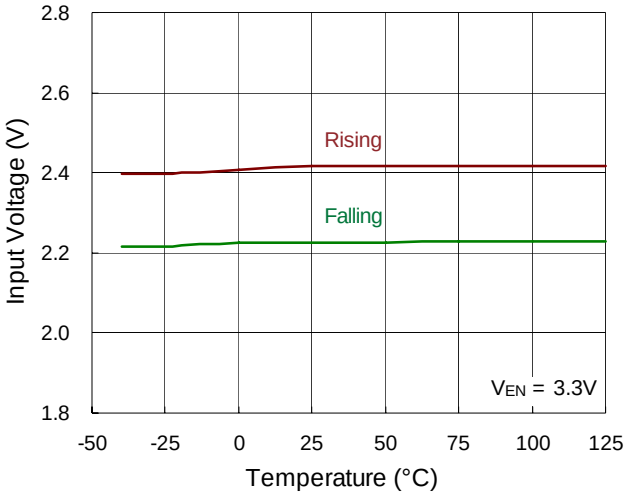

### Current Limit vs. Input Voltage



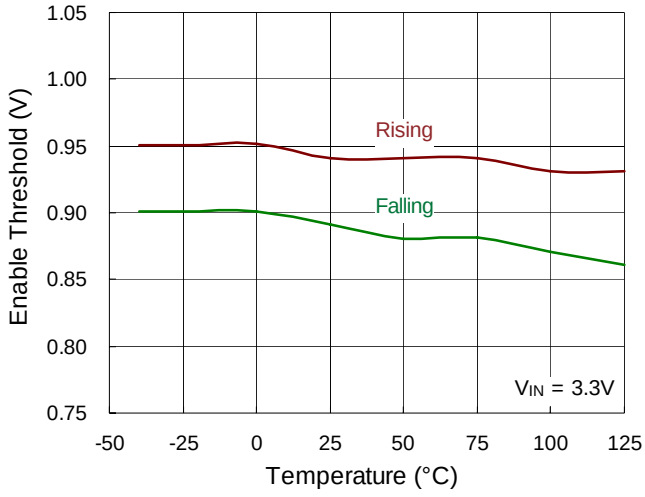

### Current Limit vs. Temperature



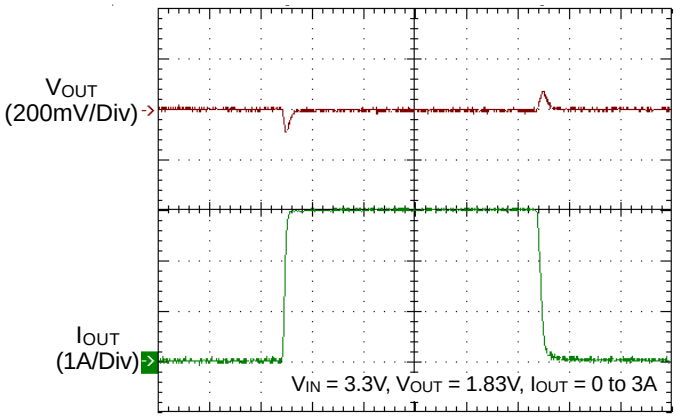

### UVLO Threshold vs. Temperature



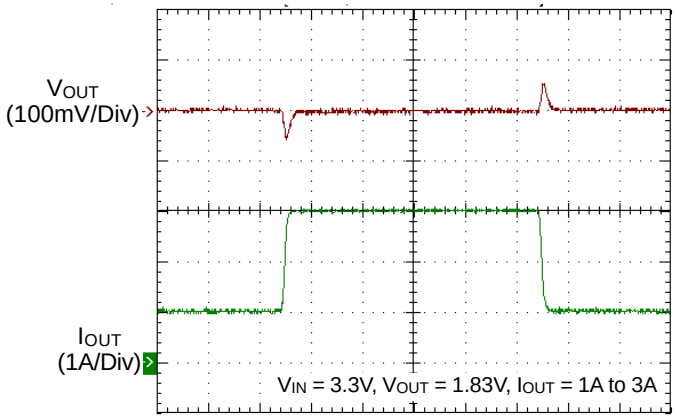

### Enable Threshold vs. Temperature



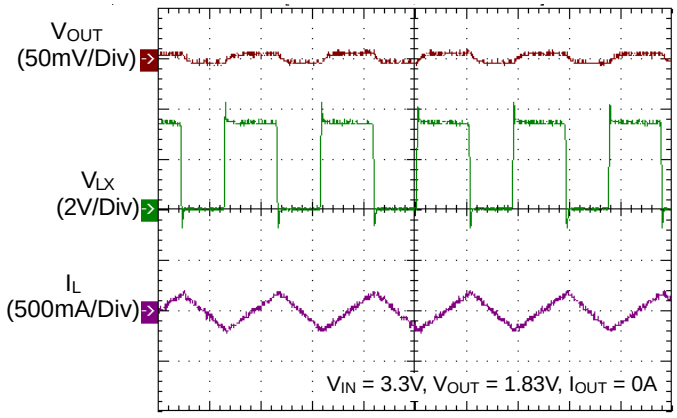
### Load Transient Response



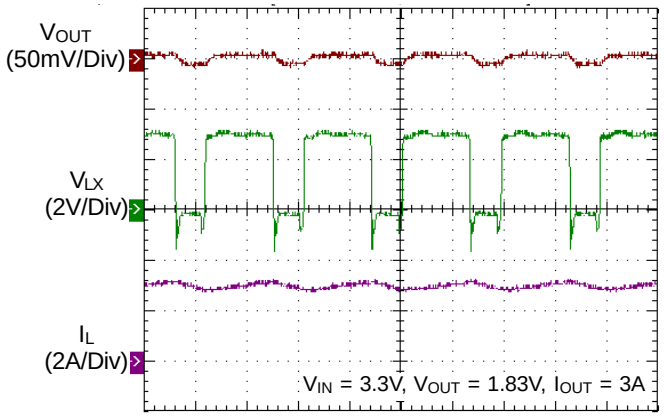

### Load Transient Response



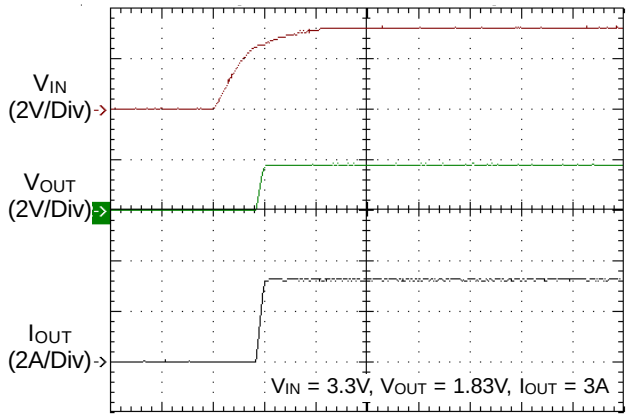

### Output Voltage Ripple



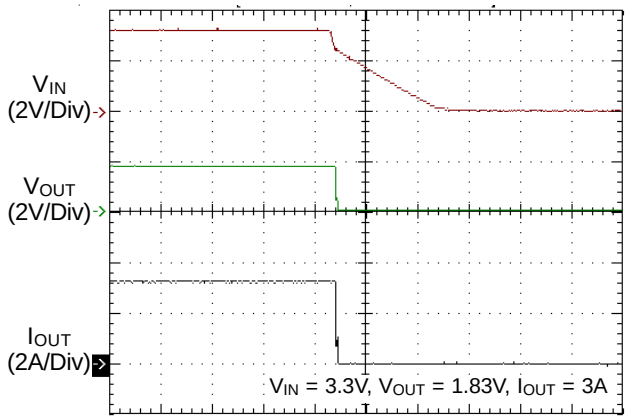

### Output Voltage Ripple



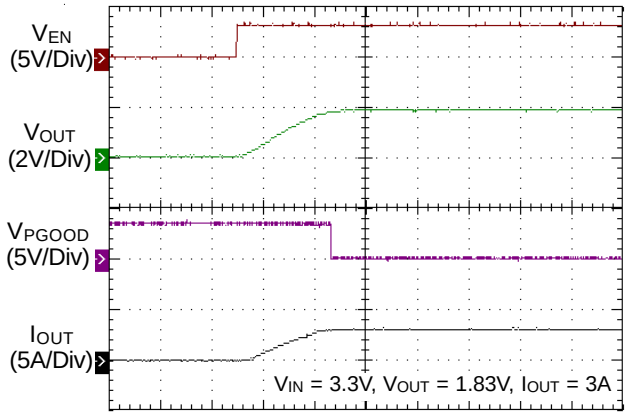

### Power On from VIN



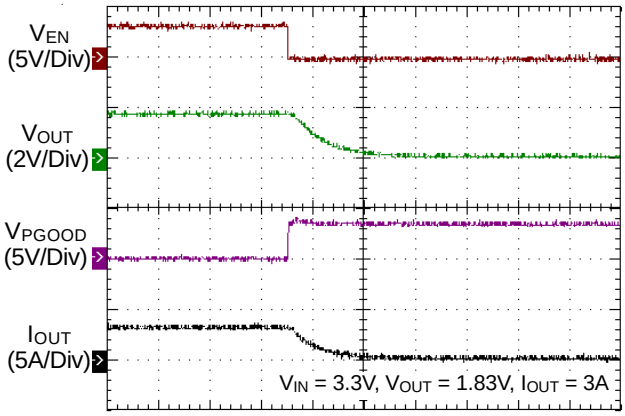

### Power Off from VIN



**Power On from EN**




**Power Off from EN**



## Application Information

This IC is a single phase Buck PWM converter. It provides single feedback loop, current mode control with fast transient response. An internal 1V reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed switching frequency (2MHz) oscillator and internal compensation are integrated to minimize external component count.

### Output Voltage Setting

The resistive voltage divider allows the FB pin to sense the output voltage as shown in Figure 1.

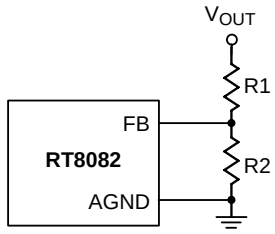



Figure 1. Setting the Output Voltage

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where $V_{REF}$ is the feedback reference voltage (1V typ.).

### Soft-Start

The IC contains an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter is turned on. Soft-start automatically begins once the chip's enable control is pulled to high. During soft-start, the internal soft-start capacitor is charged and generates a linear ramping-up voltage across the capacitor. The $V_{FB}$ voltage tracks the internal ramping-up voltage which will induce the duty pulse width to increase slowly and in turn reduce the output surge current. Finally, the internal 1V reference takes over the loop control once the internal ramping-up voltage becomes higher than 1V. The typical soft-start time is set at 1ms.

### Power Good Output

The power good output is an open-drain output and requires a pull up resistor. When the output voltage is 7% above or 7% below its set voltage, PGOOD will be pulled high. It is held high until the output voltage returns within the allowed tolerances once more. During soft-start, PGOOD is actively held high and is only allowed to be low when soft-start period is over and the output voltage reaches 93% of its set voltage.

### Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current, $\Delta I_L$, increases with higher $V_{IN}$ and decreases with higher inductance :

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High efficiency operation is achieved by reducing ripple current at low frequency, but it requires a large inductor to attain this goal.

For the ripple current selection, the value of $\Delta I_L = 0.4(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest $V_{IN}$. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

In this IC, 1μH is recommended for initial design. The inductor's current rating (cause a 40°C temperature rising from 25°C ambient) must be greater than the maximum load current and ensure that the peak current will not saturate the inductor during short circuit condition.

### Input and Output Capacitors Selection

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step change at the output can induce ringing

at the input, $V_{IN}$. This ringing can couple to the output and be mistaken. A sudden inrush of current through the long wires can potentially cause a voltage spike at $V_{IN}$ large enough to damage the part.

Two 10µF low ESR ceramic capacitors are recommended for bypassing input and an additional 0.1µF is recommended close to the IC input side for high frequency filtering. The selection of $C_{OUT}$ is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for $C_{OUT}$ selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response.

### Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub harmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, the maximum inductor peak current is reduced when slope compensation is added. For the RT8082, a separate inductor current signal is used to monitor over current condition, so this keeps the maximum output current relatively constant regardless of duty cycle.

### Under Output Voltage Protection (Hiccup Mode)

A Hiccup Mode of Under Voltage Protection (UVP) function is provided for the IC. When the FB voltage drops below half of the feedback reference voltage, $V_{REF}$, and the peak inductor current reaches the OCP threshold. The UVP function will be triggered to auto soft-start the power stage continuously until this event is cleared. The Hiccup Mode UVP reduces input current in short-circuit conditions and it will not be triggered during soft-start process.

### Under Voltage Lockout Threshold

The IC features input Under Voltage Lockout protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (2.45V typ.), the converter will reset and prepare the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage (2.25V typ.) during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis (0.2V typ.) to prevent noise from causing reset.

### Thermal Shutdown

The device implements an internal thermal shutdown function when the junction temperature exceeds 160°C. The thermal shutdown disables the device until the junction temperature drops below the hysteresis (20°C typ.). Then, the device is re-enabled and automatically reinstates the power up sequence.

### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, $\theta_{JA}$, is layout dependent. For WDFN-12E 3x3, the thermal resistance, $\theta_{JA}$, is 60°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (60°C/W) = 1.667W for WDFN-12E 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

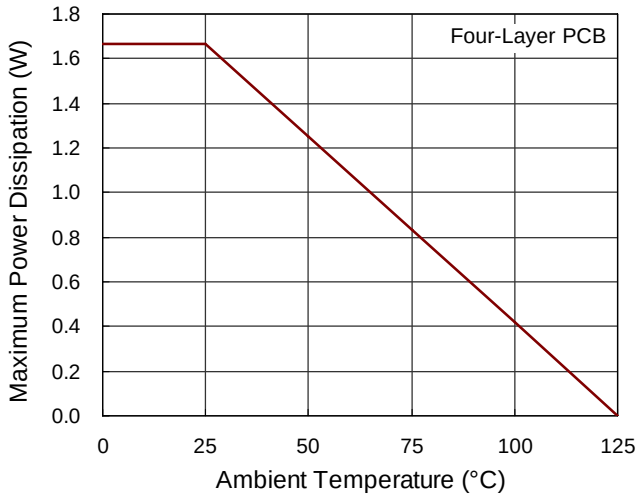



Figure 2. Derating Curve of Maximum Power Dissipation

**Layout Considerations**

Follow the PCB layout guidelines for optimal performance of the IC.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to VIN pin.
- LX node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the IC.
- Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.

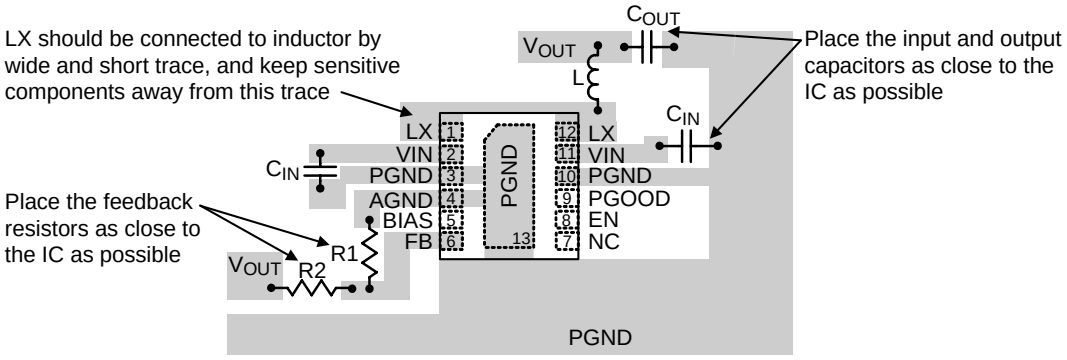
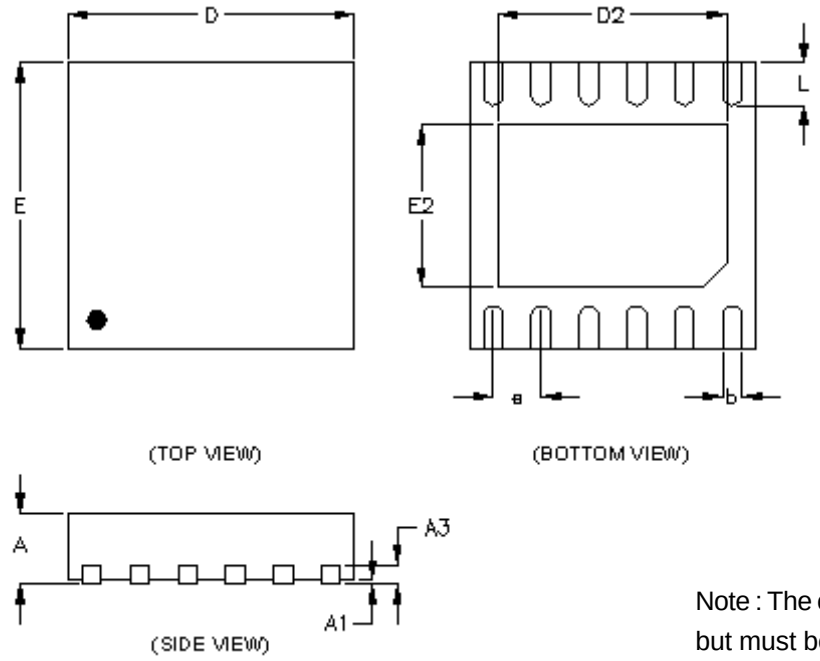
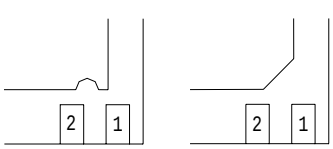



Figure 3. PCB Layout Guide

## Outline Dimension




**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.180 | 0.280 | 0.007 | 0.011 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D2 | 2.350 | 2.450 | 0.093 | 0.096 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E2 | 1.650 | 1.750 | 0.065 | 0.069 |
| e | 0.500 | | 0.020 | |
| L | 0.400 | 0.500 | 0.016 | 0.020 |

**W-Type 12E DFN 3x3 Package**

**Richtek Technology Corporation**

5F, No. 20, Taiyuen Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789