MR27V1641L

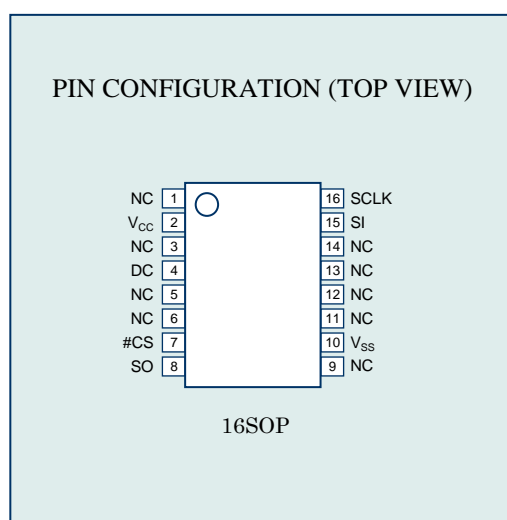**16M–Word × 1–Bit Serial Production Programmed ROM (P2ROM)**

GENERAL DESCRIPTION

The MR27V1641L is a 16 Mbit Production Programmed Read-Only Memory, which is configured as 16,777,216 word × 1-bit. The MR27V1641L supports a simple read operation using a single 3.3V power supply and a Serial Peripheral Interface (SPI) compatible serial bus.
The MR27V1641L have data programmed and have functions tested at LAPIS Semiconductor factory. (Using the DC pins for the programming function is NOT allowed.)

FEATURES

· 16,777,216-word × 1-bit configuration
· +3.0 V to 3.6 V power supply
· Access time   33 MHz serial clock (FAST-READ)
                   20 MHz serial clock (READ)
· Read Identification Instruction
· Active read current   25 mA MAX (FAST-READ)
                       20 mA MAX (READ)
· Standby current   50 µA MAX
· Serial Clock Input and Data Input/Output
· Input Data Format
       1-byte command code, 3-byte address, 1-byte dummy
          (FAST-READ)
       1-byte command code, 3-byte address
          (READ)

PIN CONFIGURATION (TOP VIEW)

Pin		Pin	
NC	1	16	SCLK
V_{CC}	2	15	SI
NC	3	14	NC
DC	4	13	NC
NC	5	12	NC
NC	6	11	NC
#CS	7	10	V_{SS}
SO	8	9	NC

16SOP

PACKAGES

· MR27V1641L-xxxMP
   16-pin plastic SOP (P-SOP16-375-1.27-K)

PIN DESCRIPTIONS

Pin name	Functions
#CS	Chip Select
SI	Serial Data Input
SO	Serial Data Output
SCLK	Clock Input
V_{CC}	Power supply voltage
V_{SS}	Ground
DC	Don't care (0v - Vcc) <for reference> Program power supply voltage Vpp under Programming operation
NC	No connection

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READ COMMAND DEFINITION

Command	Read Array (byte)	Note
1st	03[H]	1
2nd	AD1	2
3rd	AD2	2
4th	AD3	2
Action	N byte read out until #CS goes high	3

Note:
1. The 1st command 03[H] is a Read command
2. AD1 to AD3 are address input data
3. Data output

Details of Command are shown as follows.

1-byte command code								
READ:	0	0	0	0	0	0	1	1
3-byte address								
AD1:	X	X	X	A20	A19	A18	A17	A16
AD2:	A15	A14	A13	A12	A11	A10	A9	A8
AD3:	A7	A6	A5	A4	A3	A2	A1	A0

Note:
X: Dummy bit

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FAST-READ COMMAND DEFINITION

Command	Read Array (byte)	Note
1st	0B[H]	1
2nd	AD1	2
3rd	AD2	2
4th	AD3	2
5th	X	3
Action	N byte read out until #CS goes high	4

Note:
1. The 1st command 0B[H] is a Read command
2. AD1 to AD3 are address input data
3. X is a dummy cycle
4. Data output

Details of Command are shown as follows.

1-byte command code							
FAST-READ:	0	0	0	0	1	0	1	1
3-byte address							
AD1:	X	X	X	A20	A19	A18	A17	A16
AD2:	A15	A14	A13	A12	A11	A10	A9	A8
AD3:	A7	A6	A5	A4	A3	A2	A1	A0

Note:
X: Dummy bit

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READ IDENTIFICATION COMMAND DEFINITION

Command	Read Array (byte)	Note
1st	9F[H]	1
Action	3 byte read out	2

Note:
1. The 1st command 9F[H] is a Read Identification command
2. Identification output

Details of Command are shown as follows.

1-byte command code								
RDID	1	0	0	1	1	1	1	1

IDENTIFICATION DEFINITION

Manufacturer Identification	Device Identification	
	Type	Capacity
AE[H]	41[H]	13[H]

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DEVICE OPERATION

1. Command "03h" or "0Bh" makes this LSI become and keep active mode until next #CS High.
2. Incorrect command makes this LSI become and keep standby mode until next #CS Low. In standby mode, SO pin is High-Z.
3. At Power-up, the device must not be selected (that is #CS must follow the voltage applied on Vcc) until Vcc reaches the operating value.

COMMAND DESCRIPTION

1. Read Array
   This command consists of the 4-byte code. The 1st code is a command which decides if the device becomes standby or active mode. The 1st code "03h"activates the device. The 2nd code to the 4th code are address.

2. Fast-Read Array
   This command consists of the 5-byte code. The 1st code is a command which decides if the device becomes standby or active mode. The 1st code "0Bh"activates the device. The 2nd code to the 4th code are address. The 5th code is a dummy cycle.

3. Read Identification Array
   This command consists of the 1-byte code. The 1st code is a command which decides if the device becomes standby or active mode. The 1st code "9Fh"activates the device.

4. Standby
   When #CS is high , the device is put in standby mode at the next rising edge of SCLK. Maximum standby current is 50uA. When the above-mentioned 1st code is incorrect command , the device is put in standby mode at the next rising edge of SCLK.

DATA SEQUENCE

The data is serially sent out through SO pin, synchronized with the falling edge of SCLK. Meanwhile input data is also serially read in through SI pin, synchronized with the rising edge of SCLK. The bit sequence for both input and output data are bit7 (MSB) first, bit6, bit5, …, and bit0(LSB).

ADDRESS SEQUENCE

The address assignment is described at the COMMAND DEFINITION on page 2 or 3.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Storage temperature	Tstg	—	−55 to 125	°C
Input voltage	V_I		−0.5 to V_{CC}+0.5	V
Output voltage	V_O	relative to V_{SS}	−0.5 to V_{CC}+0.5	V
Power supply voltage	V_{CC}		−0.5 to 5	V
Power dissipation per package	P_D	Ta = 25°C	1.0	W
Output short circuit current	I_{OS}	—	10	mA

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating temperature under bias	Ta		0	—	70	°C
V_{CC} power supply voltage	V_{CC}	V_{CC} = 3.0 to 3.6 V	3.0	—	3.6	V
Input "H" level	V_{IH}		2.4	—	V_{CC}+0.5∗	V
Input "L" level	V_{IL}		−0.5∗∗	—	0.6	V

Voltage is relative to Vss.
∗ : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.
∗∗ : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE

(V_{CC} = 3.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C_{IN1}	V_I = 0 V	—	—	10	
Output	C_{OUT}	V_O = 0 V	—	—	10	pF
DC	C_{DC}	V_I = 0 V	—	—	200	

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ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	V_I = 0 to V_{CC}	—	—	10	µA
Output leakage current	I_{LO}	V_O = 0 to V_{CC}	—	—	10	µA
V_{CC} power supply current (Standby)	I_{CCSC}	#CS = V_{CC}	—	—	50	µA
	I_{CCST}	#CS = V_{IH}	—	—	1	mA

V_{CC} power supply current (Read)	I_{CC1}	#CS = V_{IL}
		f=20MHz
		SO=open
			—	—	20	mA

V_{CC} power supply current (Fast-Read)	I_{CC1F}	#CS = V_{IL}
		f=33MHz
		SO=open
			—	—	25	mA

Input "H" level	V_{IH}	—	2.4	—	Vcc+0.5∗	V
Input "L" level	V_{IL}	—	−0.5∗∗	—	0.6	V
Output "H" level	V_{OH}	I_{OH} = −100 µA	2.4	—	—	V
Output "L" level	V_{OL}	I_{OL} = 500 µA	—	—	0.4	V

Voltage is relative to Vss.

∗ : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

∗∗ : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

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AC CHARACTERISTICS

FAST-READ

(V$_{CC}$ = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock frequency	t$_{SCLK}$	—	—	33	MHz
Clock high time	t$_{SKH}$	—	14	—	ns
Clock low time	t$_{SKL}$	—	14	—	ns
Input signal Rise time	t$_R$	—	—	3	ns
Input signal Fall time	t$_F$	—	—	3	ns
#CS lead clock time	t$_{CSA}$	—	10	—	ns
#CS setup time	t$_{CS}$	—	5	—	ns
#CS lag clock time	t$_{CSB}$	—	5	—	ns
#CS hold time	t$_{CH}$	—	5	—	ns
#CS high time	t$_{CSH}$	—	80	—	ns
SI setup time	t$_{DS}$	—	2	—	ns
SI hold time	t$_{DH}$	—	10	—	ns
Access time	t$_{AA}$	—	—	14	ns
SO hold time	t$_{DOH}$	—	0	—	ns
SO floating time	t$_{DOZ}$	—	—	15	ns

READ

(V$_{CC}$ = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock frequency	t$_{SCLK}$	—	—	20	MHz
Clock high time	t$_{SKH}$	—	20	—	ns
Clock low time	t$_{SKL}$	—	20	—	ns
Input signal Rise time	t$_R$	—	—	3	ns
Input signal Fall time	t$_F$	—	—	3	ns
#CS lead clock time	t$_{CSA}$	—	10	—	ns
#CS setup time	t$_{CS}$	—	5	—	ns
#CS lag clock time	t$_{CSB}$	—	5	—	ns
#CS hold time	t$_{CH}$	—	5	—	ns
#CS high time	t$_{CSH}$	—	80	—	ns
SI setup time	t$_{DS}$	—	2	—	ns
SI hold time	t$_{DH}$	—	10	—	ns
Access time	t$_{AA}$	—	—	14	ns
SO hold time	t$_{DOH}$	—	0	—	ns
SO floating time	t$_{DOZ}$	—	—	15	ns

Measurement conditions   Output load

    Input signal level   0 V/Vcc
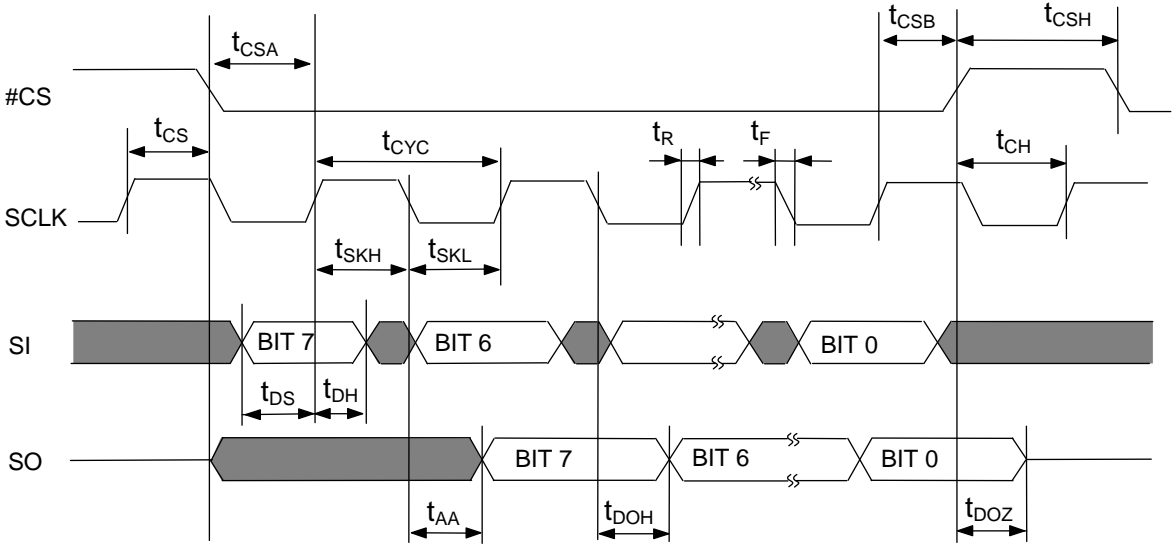
    Input timing reference level   0.3Vcc/0.7Vcc   Output

    Output load   30 pF

    Output timing reference level   0.5Vcc
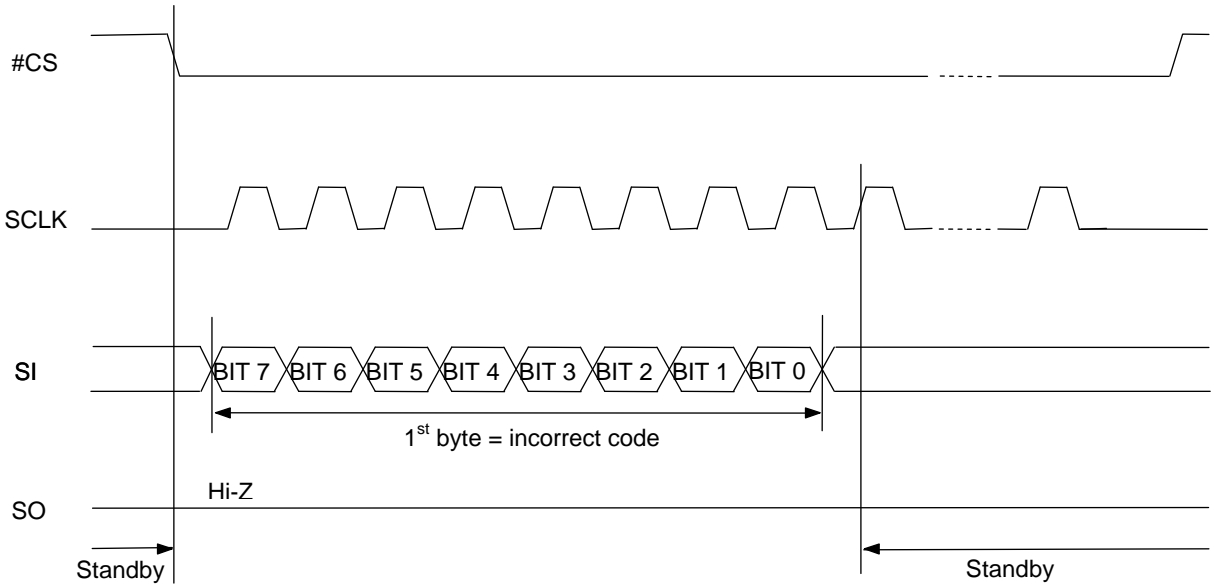
30 pF
(Including scope and jig)
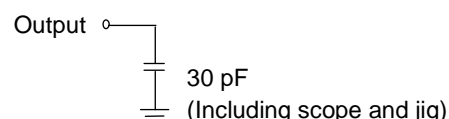
TIMING CHART (READ CYCLE)

Serial Data Input/Output Timing

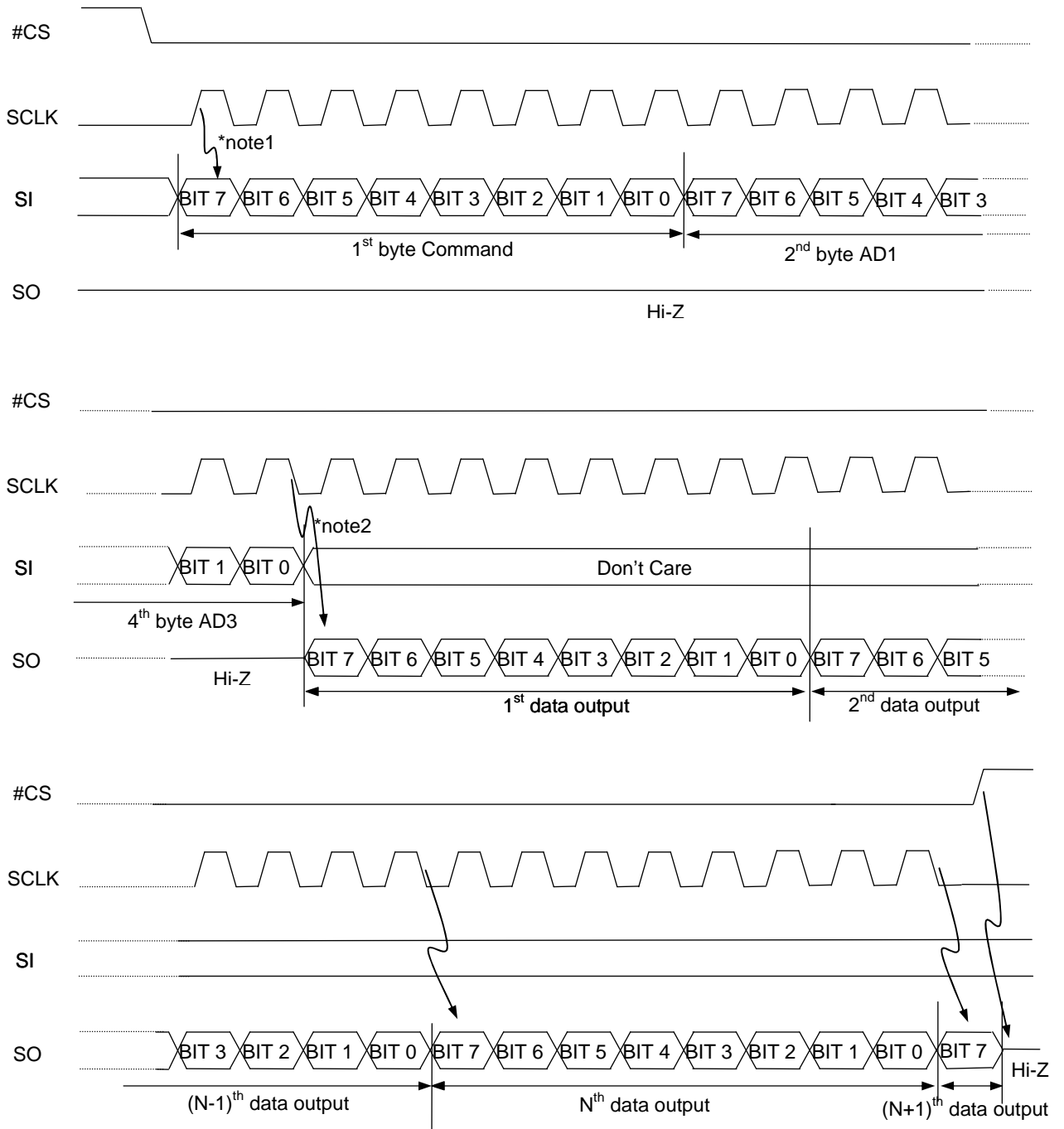### Standby Timing

Incorrect command makes this LSI become and keep standby mode until next #CS rising edge. In standby mode, SO pin is High-Z.
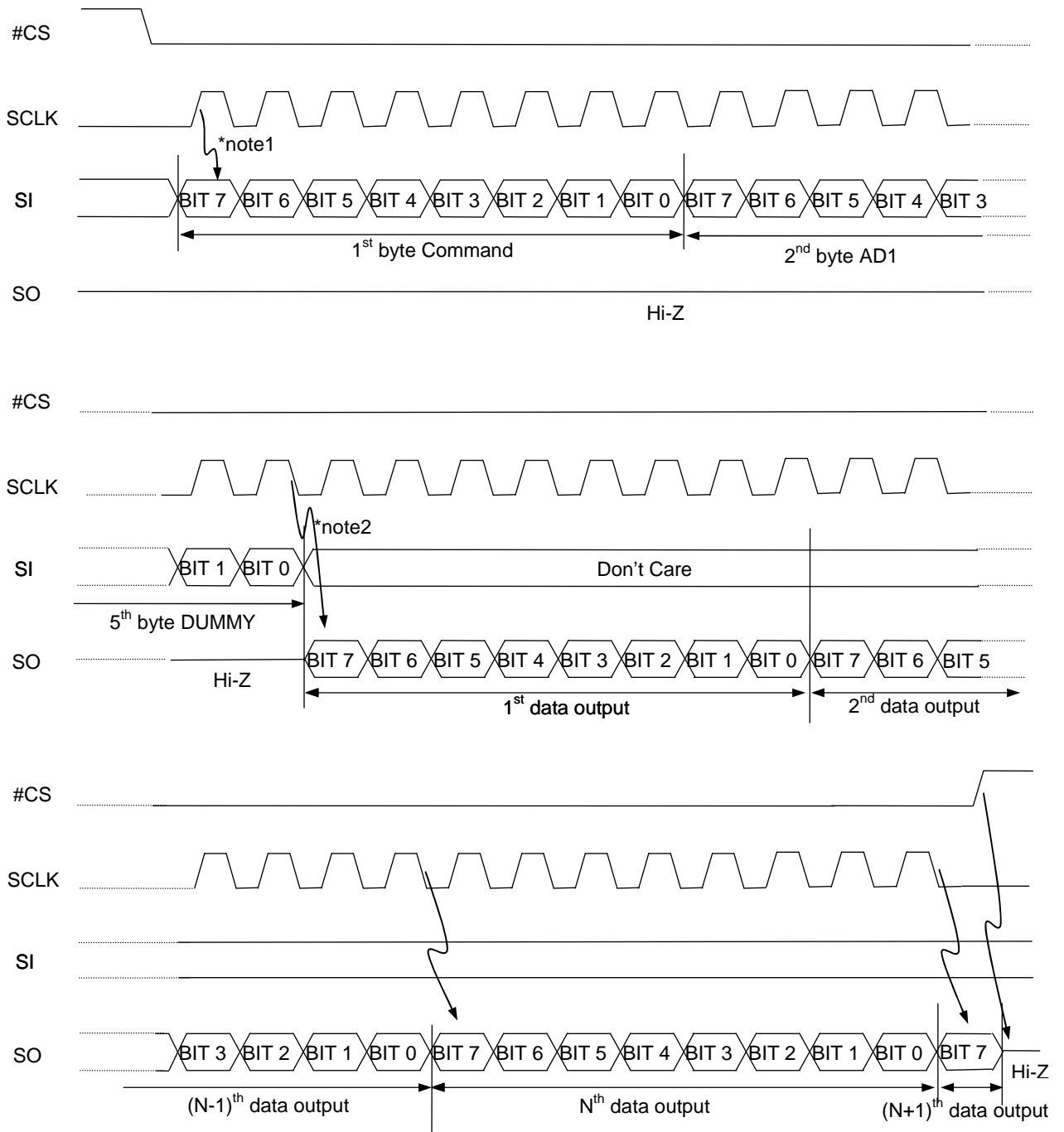
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Read Array Timing Waveform

#CS

SCLK

*note1

SI — BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3

1st byte Command   2nd byte AD1

SO — Hi-Z

#CS

SCLK

*note2

SI — BIT 1 | BIT 0 | Don't Care

4th byte AD3

SO — Hi-Z — BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | BIT 7 | BIT 6 | BIT 5

1st data output   2nd data output

#CS

SCLK

SI

SO — BIT 3 | BIT 2 | BIT 1 | BIT 0 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | BIT 7 — Hi-Z

$(N-1)^{th}$ data output N^{th} data output $(N+1)^{th}$ data output

Note:
1. Input data are latched at SCLK-rising edge.
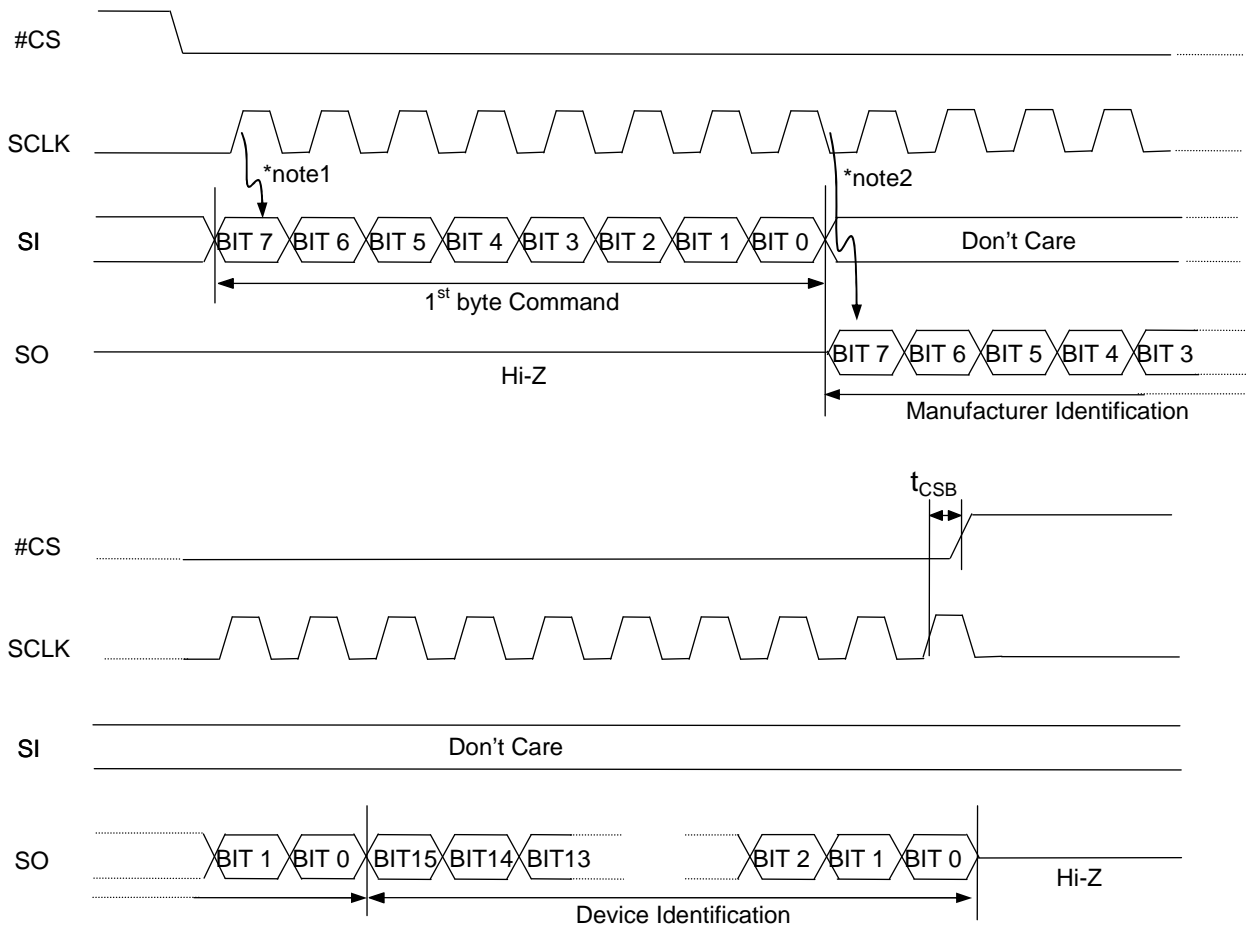2. Data-output starts at SCLK-falling edge in bit0 of the 4th byte.

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Fast Read Array Timing Waveform

#CS

SCLK

*note1

SI — BIT 7 X BIT 6 X BIT 5 X BIT 4 X BIT 3 X BIT 2 X BIT 1 X BIT 0 X BIT 7 X BIT 6 X BIT 5 X BIT 4 X BIT 3

1st byte Command   2nd byte AD1

SO

Hi-Z

#CS

SCLK

*note2

SI — BIT 1 X BIT 0   Don't Care

5th byte DUMMY

SO

Hi-Z   BIT 7 X BIT 6 X BIT 5 X BIT 4 X BIT 3 X BIT 2 X BIT 1 X BIT 0 X BIT 7 X BIT 6 X BIT 5

1st data output   2nd data output

#CS

SCLK

SI

SO — BIT 3 X BIT 2 X BIT 1 X BIT 0 X BIT 7 X BIT 6 X BIT 5 X BIT 4 X BIT 3 X BIT 2 X BIT 1 X BIT 0 X BIT 7   Hi-Z

(N-1)th data output   Nth data output   (N+1)th data output

Note:
1. Input data are latched at SCLK-rising edge.
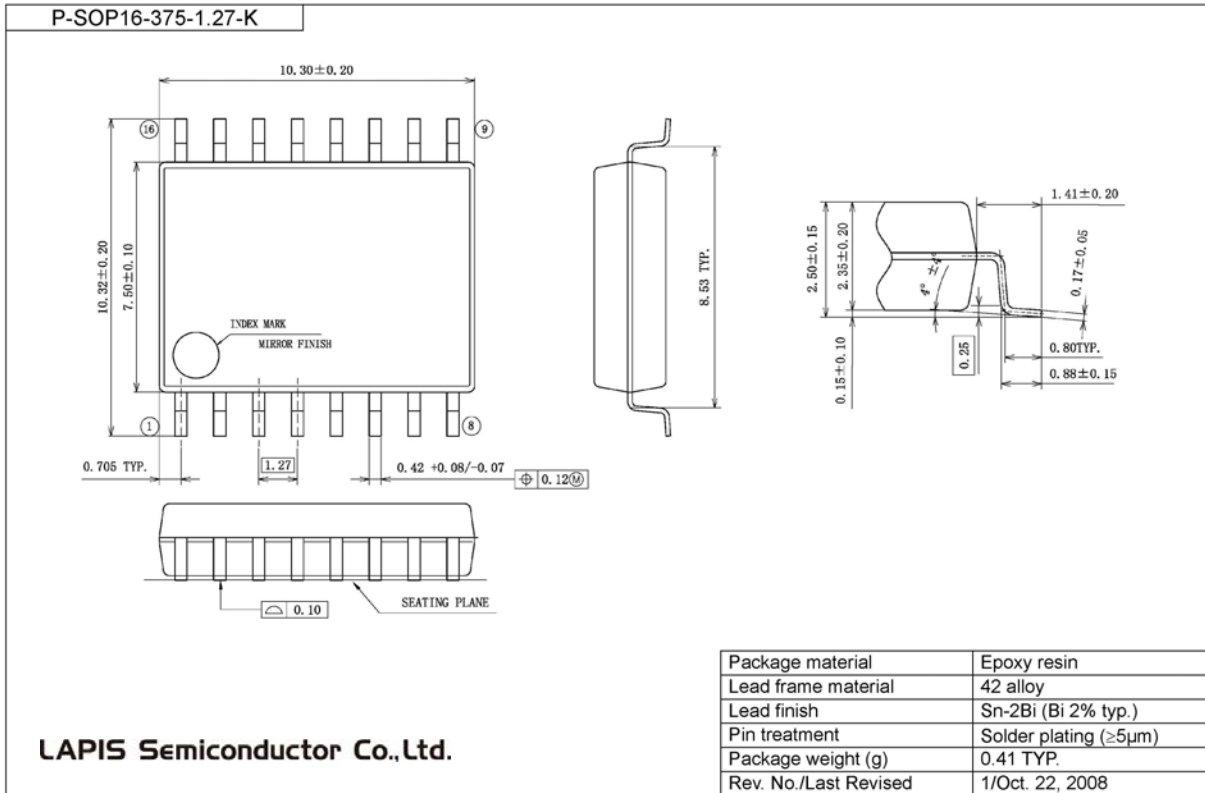2. Data-output starts at SCLK-falling edge in bit0 of the 5th byte.

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Read Identification Timing Waveform

Note:
1. Input data are latched at SCLK-rising edge.
2. Data-output starts at SCLK-falling edge in bit0 of the 1st byte.

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PACKAGE DIMENSIONS

(Unit: mm)

P-SOP16-375-1.27-K

Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.41 TYP.
Rev. No./Last Revised	1/Oct. 22, 2008

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Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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REVISION HISTORY

Document No.	Date	Page Previous Edition	Page Current Edition	Description
FEDR27V1641L-02-01	Oct. 28, 2005	–	–	Final edition 1
FEDR27V1641L-02-02	Oct. 31, 2006	1, 7, 8	1, 7, 8	serial clock (FAST-READ) 33MHz --> 30MHz
		1	1	Don't care (H or L or Open) --> Don't care (0v - Vcc)
		5	5	device operatioN added 3.
		6	6	Pin Capacitance C_{IN1} Max 12pF --> 10pF C_{OUT} Max 12pF --> 10pF
		8	8	FAST-READ t_{SKH} Min. 12ns --> 14ns t_{SKL} Min. 12ns --> 14ns FAST-READ & READ t_R Min. 0.1 V/ns --> Max. 3ns t_F Min. 0.1 V/ns --> Max. 3ns t_{AA} Max. 15ns --> 14ns t_{DOZ} Max. 8ns --> 15ns
FEDR27V1641L-02-03	Mar. 16, 2007	2	2	3-byte address (0 to 3FFF[H]) --> 3-byte address
		3	3	3-byte address (0 to 3FFF[H]) --> 3-byte address
		13	13	Replaced package diagram
FEDR27V1641L-002-03	Oct. 1, 2008	–	–	Changed company logo and name to OKI SEMICONDUCTOR
FEDR27V1641L-002-04	Apr. 1, 2009	1, 7, 8	1, 7, 8	serial clock (FAST-READ) 30MHz --> 33MHz

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