FAIRCHILD SEMICONDUCTOR®

July 2012

FDMC8878
N-Channel Power Trench® MOSFET
30V, 16.5A, 14mΩ

Features

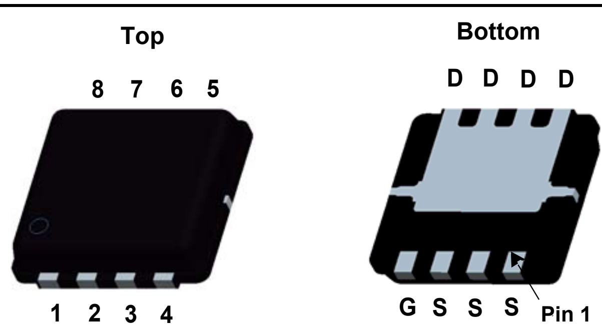
- Max $r_{DS(on)}$ = 14mΩ at V_{GS} = 10V, I_D = 9.6A
- Max $r_{DS(on)}$ = 17mΩ at V_{GS} = 4.5V, I_D = 8.7A
- Low Profile - 0.8 mm max in MLP 3.3X3.3
- RoHS Compliant

General Description

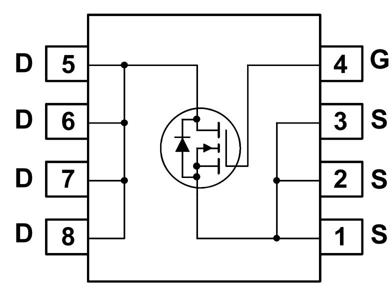
This N-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced Power Trench process. It has been optimized for power management applications.

Application

- DC - DC Conversion



MLP 3.3x3.3



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) T_C = 25°C	16.5	A
	-Continuous (Silicon limited) T_C = 25°C	38	
	-Continuous T_A = 25°C (Note 1a)	9.6	
	-Pulsed	60	
P_D	Power Dissipation T_C = 25°C	31	W
	Power Dissipation T_A = 25°C (Note 1a)	2.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8878	FDMC8878	MLP 3.3X3.3	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		20		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V			1	μA
		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C			100	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-5.7		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10V, I_D = 9.6A		9.6	14.0	mΩ
		V_{GS} = 4.5V, I_D = 8.7A		12.1	17.0	
		V_{GS} = 10V, I_D = 9.6A , T_J = 125°C		13.5	20.0	
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 9.6A		35		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		1000	1230	pF
C_{oss}	Output Capacitance			183	255	pF
C_{rss}	Reverse Transfer Capacitance			118	180	pF
R_g	Gate Resistance	f = 1MHz		1.1		Ω

Switching Characteristics

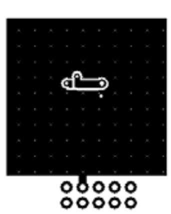
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, I_D = 9.6A V_{GS} = 10V, R_{GEN} = 6Ω		8	16	ns
t_r	Rise Time			4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			20	36	ns
t_f	Fall Time			3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 10V , V_{DD} = 15V , I_D = 9.6A		18	26	nC
Q_{gs}	Gate to Source Gate Charge			2.8		nC
Q_{gd}	Gate to Drain “Miller” Charge			3.9		nC

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 9.6A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 9.6A, di/dt = 100A/μs		23	35	ns
Q_{rr}	Reverse Recovery Charge			14	21	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 135°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted

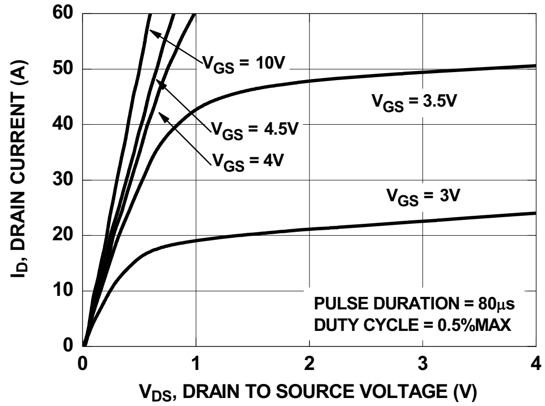


Figure 1. On-Region Characteristics

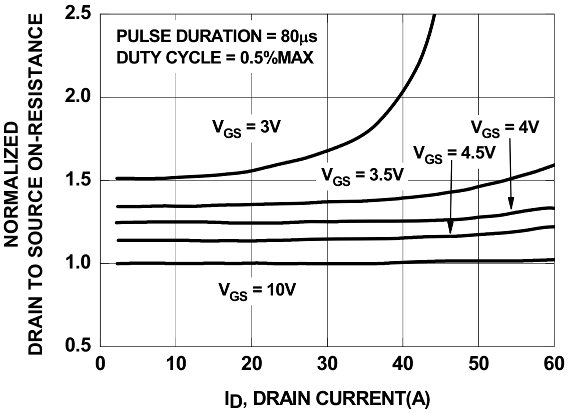


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

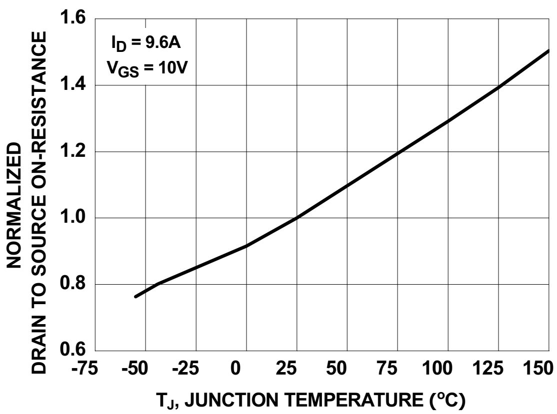


Figure 3. Normalized On-Resistance vs Junction Temperature

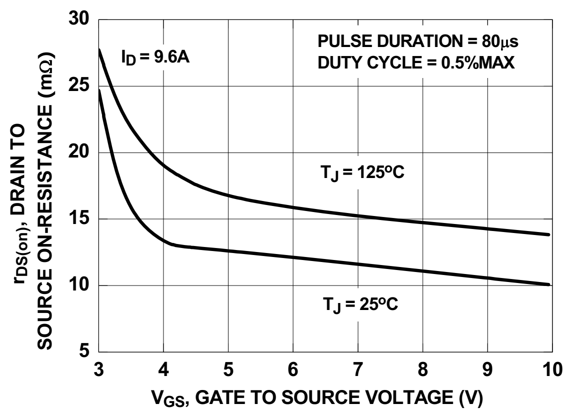


Figure 4. On-Resistance vs Gate to Source Voltage

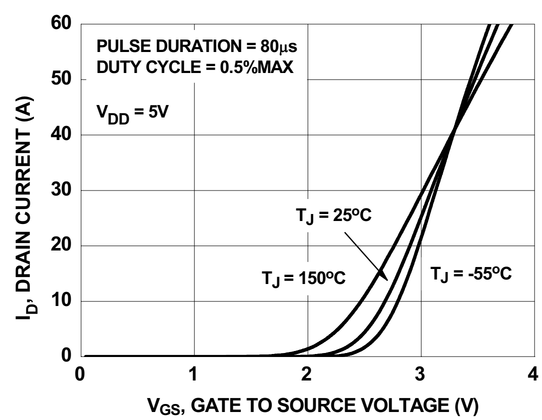


Figure 5. Transfer Characteristics

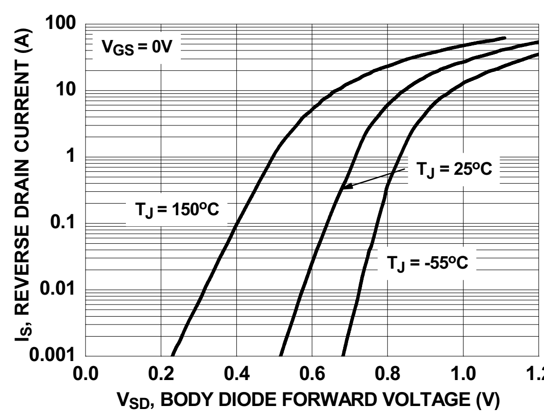


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

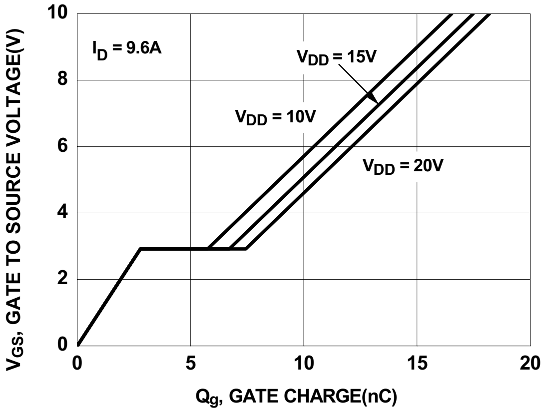


Figure 7. Gate Charge Characteristics

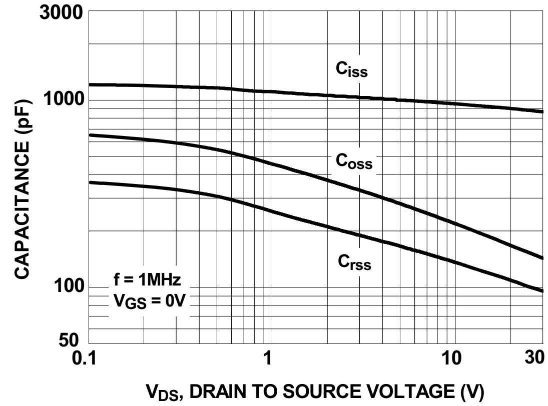


Figure 8. Capacitance vs Drain to Source Voltage

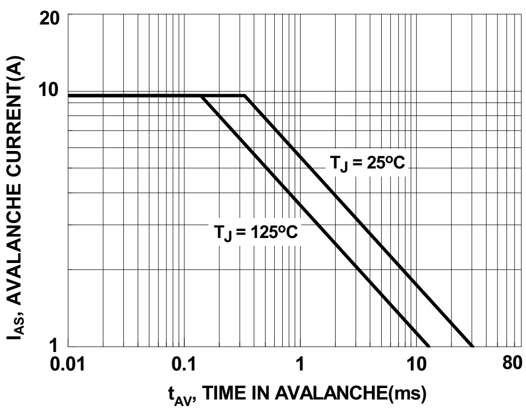


Figure 9. Unclamped Inductive Switching Capability

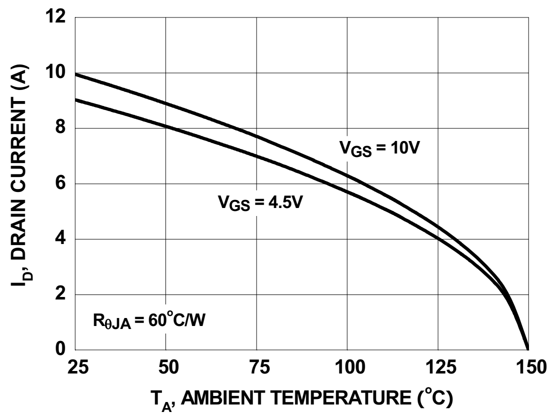


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

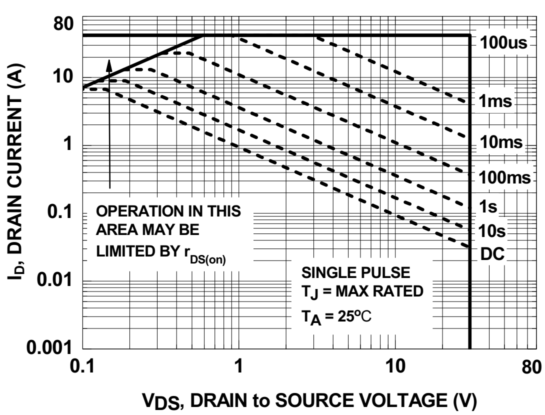


Figure 11. Forward Bias Safe Operating Area

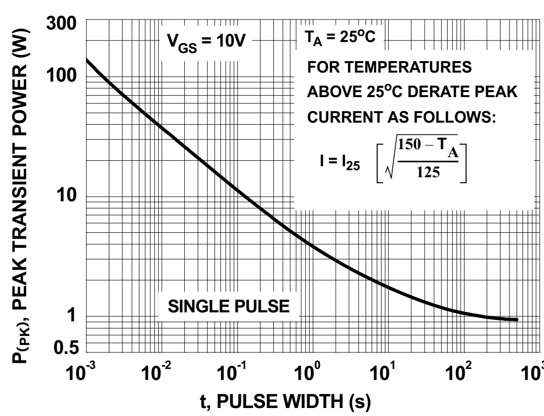


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

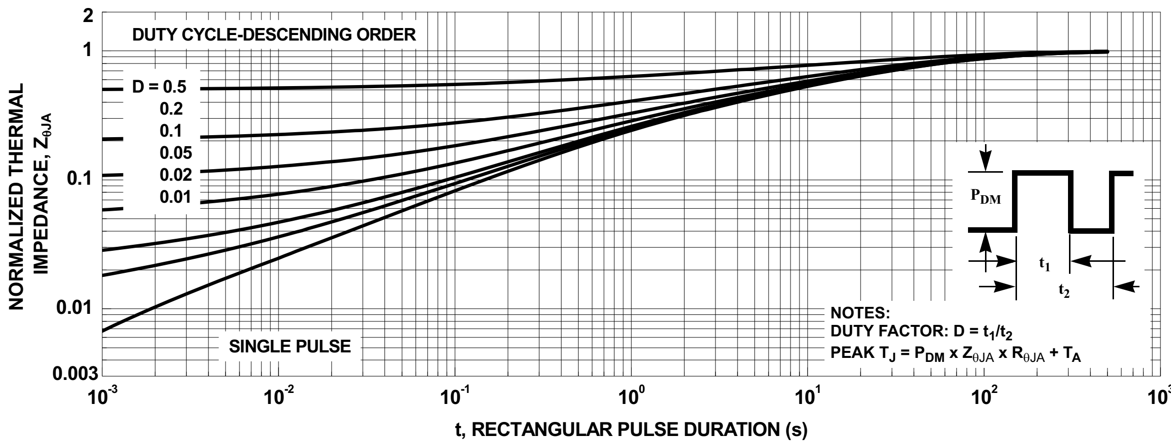
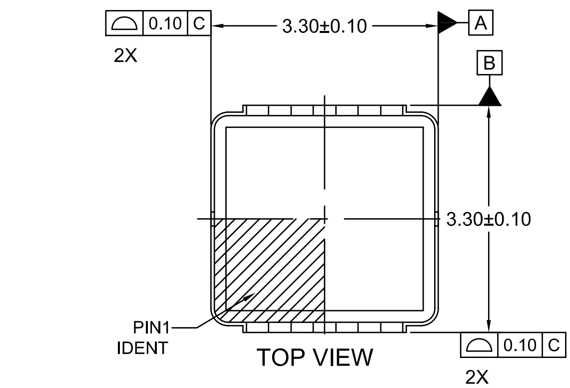
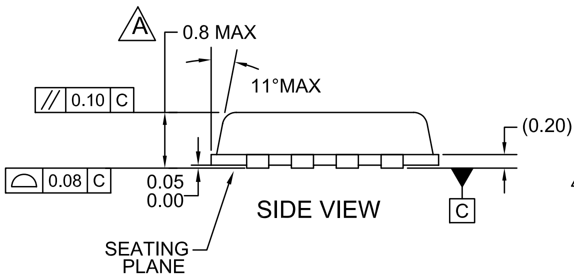
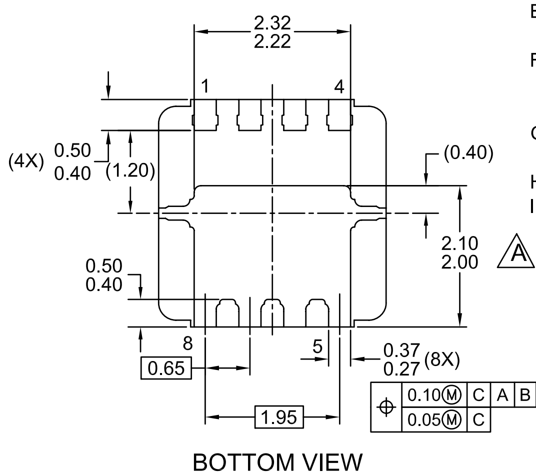


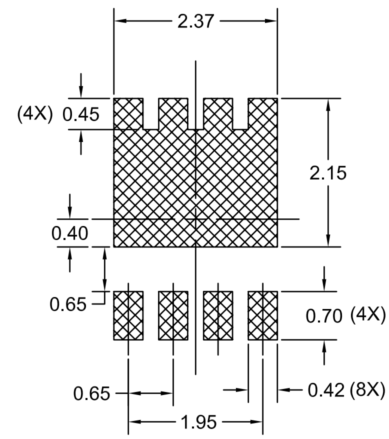
Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout









RECOMMENDED LAND PATTERN

NOTES:

A. EXCEPT AS NOTED, PACKAGE CONFORMS TO JEDEC REGISTRATION MO-240 VARIATION BA..

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY

E. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.

F. FLANGE DIMENSIONS INCLUDE INTERTERMINAL FLAS OR PROTRUSION. INTERTERMINAL FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.

G. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.

H. DRAWING FILENAME:

I. GENERAL RADII FOR ALL CORNERS SHALL BE 0.20MM MAX.

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