EPSON

S1C33L05

32-bit Single Chip Microcomputer

- 32-bit S1C33000 RISC Core
- Low Power
- Multiply Accumulation
- Built-in 16K-byte RAM
- 10-bit ADC
- Built-in LCD Controller
- Built-in USB1.1 Function Controller
- Built-in SDRAM Controller

■ DESCRIPTION

The S1C33L05 is a Seiko Epson original 32-bit microcomputer that features high speed, low power consumption, and low-voltage operation. The S1C33L05 consists of an S1C33000 32-bit RISC type CPU as its core, peripheral circuits including a bus control unit, DMA controller, interrupt controller, timers, serial interface with FIFO, A/D converter, a color STN LCD controller that supports 64K color display, SDRAM controller, USB1.1 function controller, sequential ROM interface, MMC (SPI mode) interface and NAND flash interface, and also an embedded RAM. Two oscillation circuits and a PLL are also included, supporting advanced operation, power-saving operation, and high-performance realtime clock functions. The S1C33L05 is ideal for portable products that require high-speed data processing. Especially it is suitable for the application processor embedded in PDAs, electronic dictionary and e-Book readers.

■ FEATURES

● Core CPU

Seiko Epson original 32-bit RISC CPU S1C33000 built-in

- Basic instruction set: 105 instructions (16-bit fixed size)
- Sixteen 32-bit general-purpose register
- 32-bit ALU and 8-bit shifter
- Multiplication/division instructions and MAC (multiplication and accumulation) instruction are available
- 20.83 ns of minimum instruction execution time at 48 MHz operation

● Internal memory

General-purpose RAM ..... 16K bytes (1-cycle-access)

Video-RAM ..... 40K bytes (usable for general-purpose RAM, 2-cycle-access)

● Internal peripheral circuits

OSC3 oscillation circuit/PLL ..... When PLL is disabled

Crystal oscillator	5 MHz min. to 48 MHz max.
Ceramic oscillator	48 MHz (fixed)
External clock input	2 MHz min. to 48 MHz max.

When PLL is enabled

Crystal oscillator	20 MHz min. to 48 MHz max.
Ceramic oscillator	48 MHz (fixed)
External clock input	20 MHz min. to 48 MHz max.

Generates the main clock for the bus and the CPU.
The software controllable PLL multiplies the high-speed (OSC3) oscillation clock frequency.

PLL input clock	10 MHz min. to 24 MHz max.
PLL output clock	10 MHz min. to 48 MHz max.

OSC1 oscillation circuit ..... Crystal oscillator or external clock input 32.768 kHz typ.
Generates the source clock for the realtime clock function, etc.

Timers ..... 8-bit timer 6 channels
16-bit timer 6 channels
Watchdog timer 1 channel (16-bit timer 0's function)
Clock timer 1 channel (with alarm function)

Serial interface ..... 4 channels
Clock-synchronous system, asynchronous system and IrDA 1.0 interface are selectable.
Ch.0 is selectable between a built-in buffer type (a 4-byte receive-data buffer and a 2-byte transmit-data buffer) and no buffer type.

A/D converter ..... 10 bits × 5 channels

LCD controller ..... 4 or 8-bit monochrome/color LCD interface

Panels supported
- Single-panel, single drive passive display
- 4/8-bit monochrome LCD interface
- 4/8-bit color LCD interface

Display modes
- 16-bpp mode: 64K colors or 64-level gray scale display
- 12-bpp mode: 4096 colors or 16-level gray scale display
- 8-bpp mode: 256 colors or 64-level gray scale display
- 4-bpp mode: 16 colors or 16-level gray scale display
- 2-bpp mode: 4 colors or 4-level gray scale display
- 1-bpp mode: 2 colors or 2-level gray scale display

∗ A 256 × 3 × 6-bit Look-Up Table (256K-color palette) is provided for displaying 256 colors simultaneously. The LUT can be bypassed to send display data from VRAM directly to the LCD.

∗ Gray scale display uses FRM (Frame Rate Modulation) and dithering.

Resolution (programmable)

Typical resolutions when only the internal VRAM is used:
- 320 × 240 pixels in 4-bpp mode
- 160 × 240 pixels in 8-bpp mode
- 160 × 160 pixels in 12-bpp mode

Typical resolutions when an external VRAM is used via the UMA:
- 320 × 240 pixels in 8-bpp mode
- 320 × 240 pixels in 16-bpp mode

SDRAM controller ..... 48 MHz synchronous clock max.
Supports up to 256M-bit (32MB) SDRAM with 16-bit data width.
16-stage IQB (32-byte Instruction Queue Buffer) and 2-stage DQB (4-byte Data Queue Buffer) are provided.
Allows LCDC DMA controller to access SDRAM directly as an external VRAM.

MMC (SPI mode) interface ..... 1 channel
Supports 1 to 16-bit serial data transfer in master mode.
Compatible with MMC.

NAND flash interface ..... Generates the #SMWE and #SMRE signals using the BCU signals to interface directly with SmartMedia cards or NAND flash memories.
Supports 8/16-bit Nand flash devices. Also the Nand flash booting function and the ECC function when a Nand flash is read/written are supported.

Sequential ROM interface ..... Supports MX23L12813 (manufactured by Macronix International Co., Ltd.).
Generates the SQUALE, SQLALE and #SQRD signals using the BCU signals to interface directly with the sequential mask ROM.

USB1.1 function controller ..... Endpoint: EP0, EPa, EPb, EPc, EPd (4 channels);
FIFO: 1,024 bytes

DMA controller ..... High-speed DMA 4 channels
High-speed DMA Ch. 3 has been reserved for the internal USB1.1 function controller.
Intelligent DMA 128 channels

Interrupt controller ..... Possible to invoke DMA

Input interrupt	10 types (programmable)
DMA controller interrupt	5 types
16-bit programmable timer interrupt	12 types
8-bit programmable timer interrupt	6 types
Serial interface interrupt	15 types
A/D converter interrupt	1 type
Clock timer interrupt	1 type
LCD controller interrupt	1 type
SPI interrupt	1 type
USB function controller interrupt	1 type

General-purpose input and output ports ... Shared with the I/O pins for internal peripheral circuits
Input port 9 bits (max.)
I/O port 69 bits (max.)

∗ The K54 and K65–K67 pins are not available in the S1C33L05.
∗ Two LED direct output (8 mA) ports (P27 and P26) are available.
∗ The number of the ports varies depending on the peripheral functions used.

● External bus interface

BCU (bus control unit) built-in

- 26-bit address bus (internal 28-bit processing)
- 16-bit data bus (Data size is selectable from 8 bits and 16 bits in each area.)
- Little/big-endian memory access; endian type may be set in each area.
- Memory mapped I/O
- Chip enable and wait control circuits built-in
- Supports burst ROM.

● Operating conditions and power consumption

Operating voltage	Core (V_{DD})	1.65 V to 1.95 V (1.8 V ±0.15 V) (when crystal oscillator is used) 1.70 V to 1.90 V (1.8 V ±0.10 V) (when ceramic oscillator is used)
	I/O (V_{DDE}, AV_{DDE})	2.70 V to 3.60 V (when USB is not used) 3.00 V to 3.60 V (when USB is used)
Operating clock frequency	CPU	48 MHz max. Note 1
	Bus (BCU)	40 MHz max.
	LCD controller	48 MHz max.
	USB function controller	48 MHz
	SDRAM	48 MHz
Operating temperature	-40 to 85°C (when crystal oscillator is used)	
	0 to 70°C (when ceramic oscillator is used)	
Power consumption	During SLEEP	12 µW typ.
	During HALT	18 mW typ. (48 MHz, LCDC and USB not included)
	During execution	42 mW typ. Note 2 (48 MHz, LCDC and USB not included)
	LCD controller - During display	1.8 mW typ. (LCDC clock = 8 MHz, 16 bpp, IVRAM mode, V_{DD}, LCDC block only)
	USB controller - Idle state	14 mW typ. (V_{DD}, USB block only)

● Supply form

Plastic package	QFP21-176pin (24 mm × 24 mm × 1.4 mm, 0.5-mm pitch)
Die form	167-PAD (5.25 mm × 4.85 mm, 100 µm pitch)

Notes: 1. Set the #X2SPD pin to "0" when running the CPU with a 40 MHz or more system clock. Also make sure that the internal bus operating clock frequency does not exceed 40 MHz.

2. The values of power consumption during execution were measured when a test program that consisted of 55% load instructions, 23% arithmetic operation instructions, 1% mac instruction, 12% branch instructions and 9% ext instruction was being continuously executed.

■ BLOCK DIAGRAM

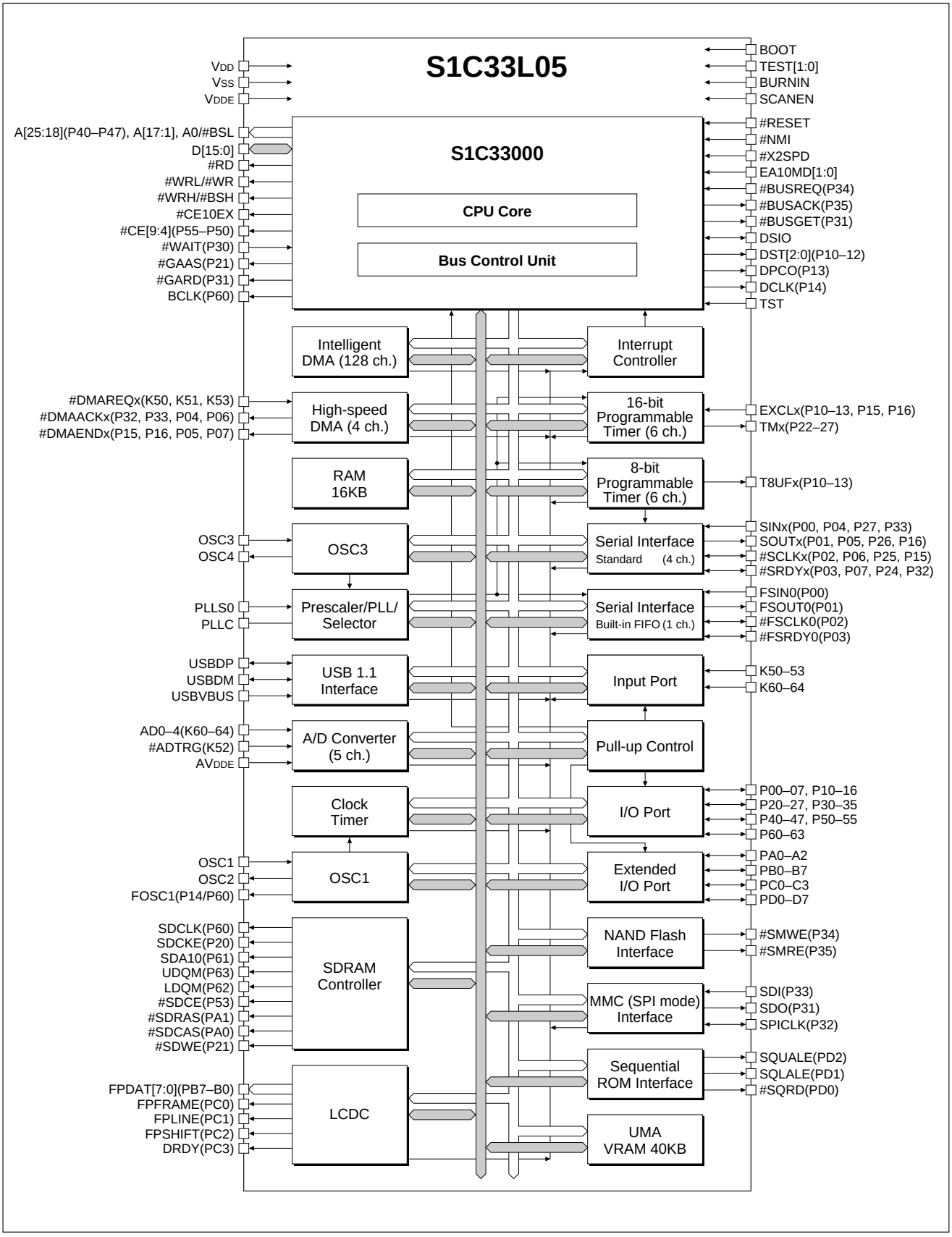
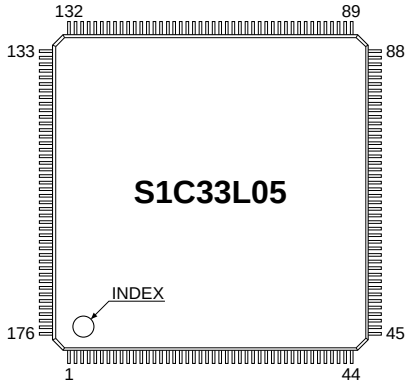


Fig. 1 S1C33L05 Functional Block Diagram

■ PIN LAYOUT

QFP21-176pin

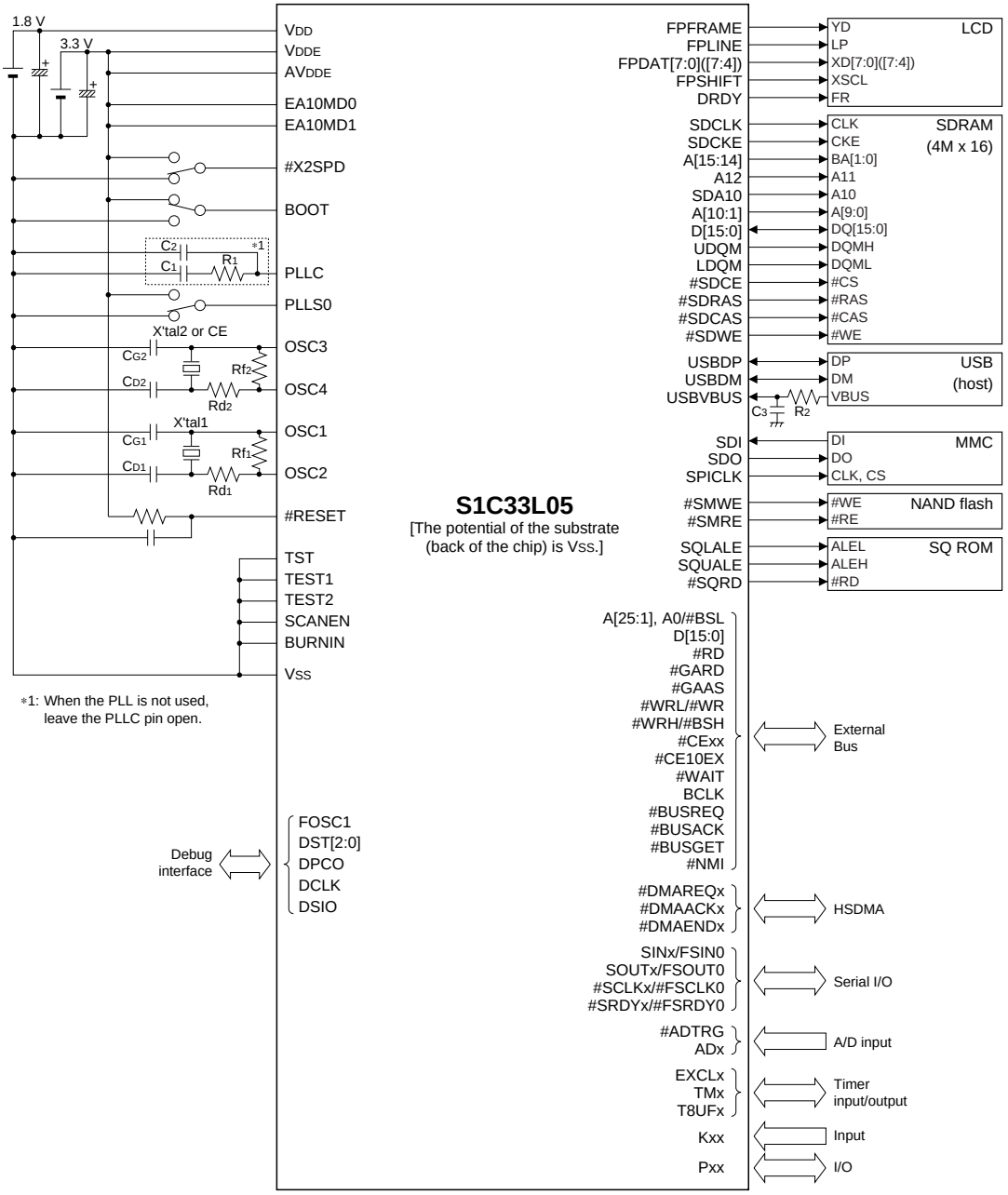


No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	**D9**	45	**P15**/EXCL4/#DMAEND0/#SCLK3	89	**P01**/SOUT0/FSOUT0	133	**A23**/P42
2	**D8**	46	N.C.	90	**P00**/SIN0/FSIN0	134	N.C.
3	**VDDE**	47	**DSIO**	91	**USBDP**	135	**A22**/P43
4	**D7**	48	**VDDE**	92	**USBDM**	136	**A21**/P44
5	**D6**	49	**DCLK**/P14/FOSC1	93	N.C.	137	**A20**/P45
6	**D5**	50	**DPCO**/P13/EXCL3/T8UF3	94	**USBVBUS**	138	**A19**/P46
7	**D4**	51	**DST2**/P12/EXCL2/T8UF2	95	**VDDE**	139	**A18**/P47
8	**D3**	52	**DST1**/P11/EXCL1/T8UF1	96	**P31**/#BUSGET/#GARD/SDO	140	**A17**
9	**D2**	53	**DST0**/P10/EXCL0/T8UF0	97	**P32**/#DMAACK0/#SRDY3/SPICLK	141	**A16**
10	**D1**	54	**VDD**	98	**VSS**	142	**VDDE**
11	**D0**	55	**#NMI**	99	**P33**/#DMAACK1/SIN3/SDI	143	**A15**
12	**VSS**	56	**#RESET**	100	**P34**/#BUSREQ/#CE6/#SMWE	144	**A14**
13	**P30**/#WAIT/#CE4&5/PA2	57	N.C.	101	**P35**/#BUSACK/#SMRE	145	N.C.
14	**PD0**/#SQRD	58	**VSS**	102	**VDD**	146	**A13**
15	**PD1**/SQLALE	59	**K60**/AD0	103	**#X2SPD**	147	**A12**
16	**PD2**/SQUALE	60	**K61**/AD1	104	**EA10MD0**	148	**VSS**
17	**PD3**	61	**K62**/AD2	105	**EA10MD1**	149	**A11**
18	**PD4**	62	**K63**/AD3	106	**VDDE**	150	**A10**
19	**PD5**	63	**K64**/AD4	107	**PLLC**	151	**VDD**
20	**PD6**	64	**TEST0**	108	**VSS**	152	**A9**
21	**PD7**	65	**AVDDE**	109	**PLLS0**	153	**A8**
22	**VDDE**	66	**K53**/#DMAREQ2	110	**TST**	154	**A7**
23	**P22**/TM0	67	**K52**/#ADTRG	111	**BOOT**	155	**A6**
24	**P23**/TM1	68	**K51**/#DMAREQ1	112	**#CE4**/#CE11/#CE11&12/P50	156	**A5**
25	**P24**/TM2/#SRDY2	69	**K50**/#DMAREQ0	113	**VSS**	157	**VSS**
26	**P25**/TM3/#SCLK2	70	**VSS**	114	**#CE5**/#CE15/#CE15&16/P51	158	**A4**
27	**P26**/TM4/SOUT2	71	**OSC1**	115	**#CE6**/#CE7&8/P52	159	**A3**
28	**P27**/TM5/SIN2	72	**OSC2**	116	#**CE7**/#RAS0/#CE13/#RAS2/P53/#SDCE	160	**VDDE**
29	**VSS**	73	**VDDE**	117	**#CE8**/#RAS1/#CE14/#RAS3/P54	161	**A2**
30	**PB7**/FPDAT7	74	**BURNIN**	118	**#CE9**/#CE17/#CE17&18/P55	162	**A1**
31	**PB6**/FPDAT6	75	**SCANEN**	119	**#CE10EX**/#CE9&10EX	163	**A0**/#BSL
32	**PB5**/FPDAT5	76	**TEST1**	120	**P61**/SDA10	164	**#WRH**/#BSH
33	**PB4**/FPDAT4	77	N.C.	121	**P62**/LDQM	165	N.C.
34	**VDD**	78	**VDD**	122	**P63**/UDQM	166	**#WRL**/#WR/#WE
35	**PB3**/FPDAT3	79	**OSC3**	123	**P21**/#DWE/#GAAS/#SDWE	167	**#RD**
36	**PB2**/FPDAT2	80	**OSC4**	124	**#LCAS**/PA0/#SDCAS	168	**VSS**
37	**PB1**/FPDAT1	81	**VSS**	125	**VDD**	169	**D15**
38	**PB0**/FPDAT0	82	**P07**/#SRDY1/#DMAEND3	126	**#HCAS**/PA1/#SDRAS	170	**D14**
39	**PC3**/DRDY	83	**P06**/#SCLK1/#DMAACK3	127	**P20**/#DRD/SDCKE	171	**D13**
40	**PC2**/FPSHIFT	84	**P05**/#SOUT1/#DMAEND2	128	**VDDE**	172	**D12**
41	**PC1**/FPLINE	85	**P04**/#SIN1/#DMAACK2	129	**BCLK**/P60/FOSC1/SDCLK	173	**D11**
42	**PC0**/FPFRAME	86	**P03**/#SRDY0/#FSRDY0	130	**A25**/P40	174	**VDD**
43	**VSS**	87	**P02**/#SCLK0/#FSCLK0	131	**VSS**	175	**D10**
44	**P16**/EXCL5/#DMAEND1/SOUT3	88	N.C.	132	**A24**/P41	176	N.C.

Bold: The pin (signal) name of a default setup.

Fig. 2 Pin Layout Diagram (QFP21-176pin)

■ BASIC EXTERNAL CONNECTION DIAGRAM



X'tal1	Crystal resonator	32.768 kHz
C_{G1}	Gate capacitor	12 pF
C_{D1}	Drain capacitor	12 pF
R_{f1}	Feedback resistor	10 MΩ
R_{d1}	Drain resistor	0 Ω
R_1	Resistor	4.7 kΩ
C_1	Capacitor	100 pF
C_2	Capacitor	3 pF
R_2	Resistor	10 Ω
C_3	Capacitor	1 µF

X'tal2 or CE	Resonator	Crystal	Ceramic (CSTCW48M0X11***)
C_{G2}	Gate capacitor	3 pF	(6 pF) *1, *2
C_{D2}	Drain capacitor	4 pF	(6 pF) *1, *2
R_{f2}	Feedback resistor	1 MΩ	22 kΩ *1
R_{d2}	Drain resistor	0 Ω	47 Ω *1

Note: *1 Oscillation characteristics vary depending on conditions (components used, board pattern, etc.). The values in the above table are shown only for reference and not guaranteed. In particular, ceramic oscillation is extremely sensitive to influence of external components and printed-circuit boards. Before using a ceramic resonator, please be sure to contact Murata Manufacturing Co., Ltd. for further information on conditions of use for ceramic resonators. Furthermore, this chip supports only 48-MHz ceramic resonators. Do not use ceramic resonators with any other frequency.

*2 Capacitance built into the ceramic resonator

Fig. 3 Basic External Connection Diagram

S1C33L05

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