

# TCP-3039H

## Advance Information

# 3.9 pF Passive Tunable Integrated Circuits (PTIC)

### Introduction

ON Semiconductor's PTICs have excellent RF performance and power consumption, making them suitable for any mobile handset or radio application. The fundamental building block of our PTIC product line is a tunable material called ParaScan™, based on Barium Strontium Titanate (BST). PTICs have the ability to change their capacitance from a supplied bias voltage generated by the Control IC. The 3.9 pF PTICs are available as wafer-level chip scale packages (WLCSP) and in QFN packages for easy mounting directly on printed circuit boards.

### Key Features

- High Tuning Range and Operation up to 20 V
- Usable Frequency Range: from 700 MHz to 2.7 GHz
- High Quality Factor (Q) for Low Loss
- High Power Handling Capability
- Compatible with PTIC Control IC TCC-103
- WLCSP Package: 0.722 x 1.029 x 0.611 mm (10 pillar)
- QFN Package: 1.200 x 1.600 x 0.950 mm
- QFN: MSL-2 Moisture Sensitivity Level (per J-STD-020)
- Pb-Free and RoHS Compliant

### Typical Applications

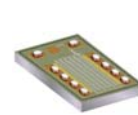
- Multi-band, Multi-standard, Advanced and Simple Mobile Phones
- Tunable Antenna Matching Networks
- Tunable RF Filters
- Active Antennas

This document contains information on a new product. Specifications and information herein are subject to change without notice.



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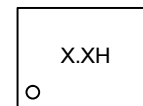


WLCSP  
10 pillar  
CASE TBD



QFN  
6 pin  
CASE TBD

### QFN MARKING DIAGRAM



X.X = 3.9

H = High Tuning

### FUNCTIONAL BLOCK DIAGRAM

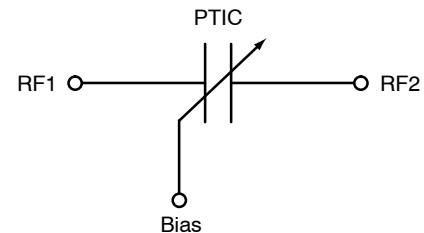


Figure 1. PTIC Functional Block Diagram

### ORDERING INFORMATION

| Device       | Package            | Shipping                 |
|--------------|--------------------|--------------------------|
| TCP-3039H-DT | WLCSP<br>(Pb-Free) | 4000 Units /<br>7" Reel  |
| TCP-3039H-QT | QFN<br>(Pb-Free)   | 8000 Units /<br>13" Reel |

For detailed ordering information, including part number definition and capacitance (pF) see the package dimensions section on page 7 of this datasheet.

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## TYPICAL SPECIFICATIONS

### Representative Performance Data at 25°C

**Table 1. PERFORMANCE DATA**

| Parameter                                       | Min  | Typ  | Max  | Units         |
|---|------|------|------|---------------|
| Operating Bias Voltage                          | 2.0  |      | 20   | V             |
| Capacitance ( $V_{bias} = 2\text{ V}$ )         | 3.51 | 3.90 | 4.29 | pF            |
| Capacitance ( $V_{bias} = 20\text{ V}$ )        | 0.98 | 1.03 | 1.08 | pF            |
| Tuning Range (2 V - 20 V)                       | 3.40 | 3.80 | 4.20 |               |
| Tuning Range (20 V - 2 V)                       |      | 3.60 |      |               |
| Leakage Current (WLCSP)                         |      |      | 2.0  | $\mu\text{A}$ |
| Operating Frequency                             | 700  |      | 2700 | MHz           |
| Quality Factor @ 700 MHz, 10 V                  |      | 90   |      |               |
| Quality Factor @ 2.4 GHz, 10 V                  |      | 60   |      |               |
| IP3 ( $V_{bias} = 2\text{ V}$ ) [1,3]           |      | 70   |      | dBm           |
| IP3 ( $V_{bias} = 20\text{ V}$ ) [1,3]          |      | 85   |      | dBm           |
| 2nd Harmonic ( $V_{bias} = 2\text{ V}$ ) [2,3]  |      | -65  |      | dBm           |
| 2nd Harmonic ( $V_{bias} = 20\text{ V}$ ) [2,3] |      | -80  |      | dBm           |
| 3rd Harmonic ( $V_{bias} = 2\text{ V}$ ) [2,3]  |      | -40  |      | dBm           |
| 3rd Harmonic ( $V_{bias} = 20\text{ V}$ ) [2,3] |      | -70  |      | dBm           |
| Transition Time (Cmin $\rightarrow$ Cmax) [4]   |      | 80   |      | $\mu\text{s}$ |
| Transition Time (Cmax $\rightarrow$ Cmin) [4]   |      | 70   |      | $\mu\text{s}$ |

1.  $f_1 = 850\text{ MHz}$ ,  $f_2 = 860\text{ MHz}$ , Pin 25 dBm/Tone
2. 850 MHz, Pin +34 dBm
3. IP3 and Harmonics are measured in the shunt configuration in a 50  $\Omega$  environment
4. RF<sub>IN</sub> and RF<sub>OUT</sub> are both connected to DC ground

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## Representative performance data at 25°C for 3.9 pF WLCSP Package

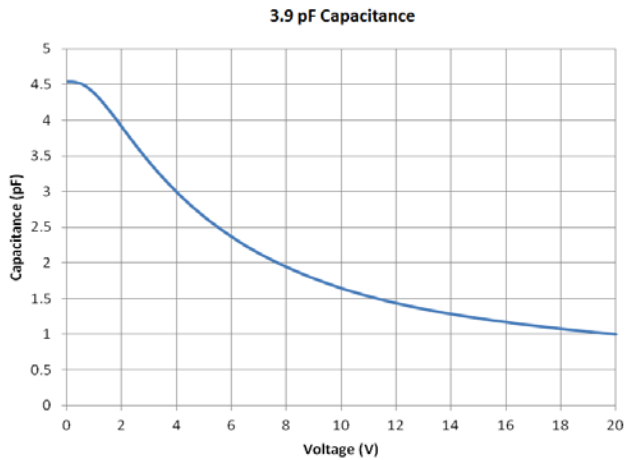


Figure 2. Capacitance

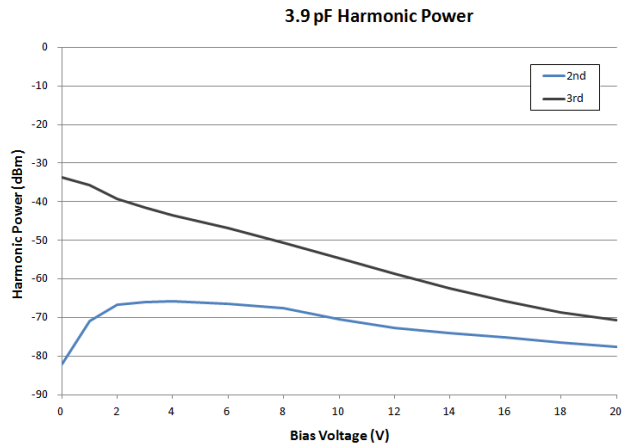


Figure 3. Harmonic Power\*

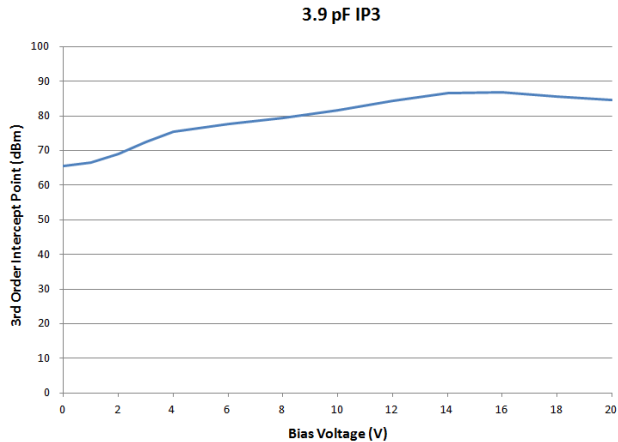


Figure 4. IP3\*

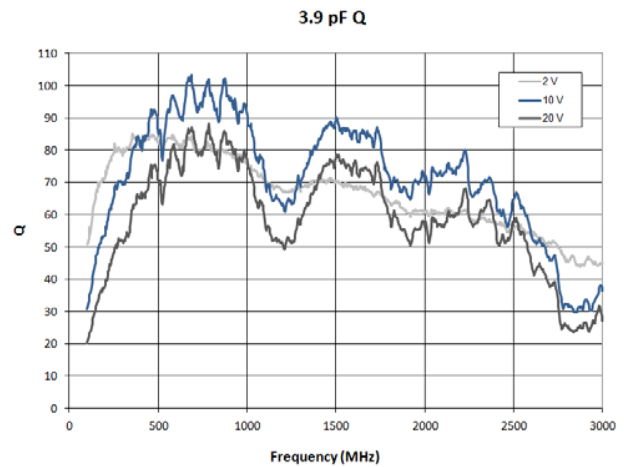


Figure 5. Q\*

\*The data shown is based on the TCP-1039N device performance, for reference only. The TCP-3039H performance data will be available in the Production Datasheet.

Table 2. ABSOLUTE MAXIMUM RATINGS

| Parameter                   | Rating                               | Units |
|-----------------------------|--------------------------------------|-------|
| Input Power                 | +40                                  | dBm   |
| Bias Voltage                | +25 (Note 5)                         | V     |
| Operating Temperature Range | -30 to +85                           | °C    |
| Storage Temperature Range   | -55 to +125                          | °C    |
| ESD – Human Body Model      | Class 1A JEDEC HBM Standard (Note 6) |       |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

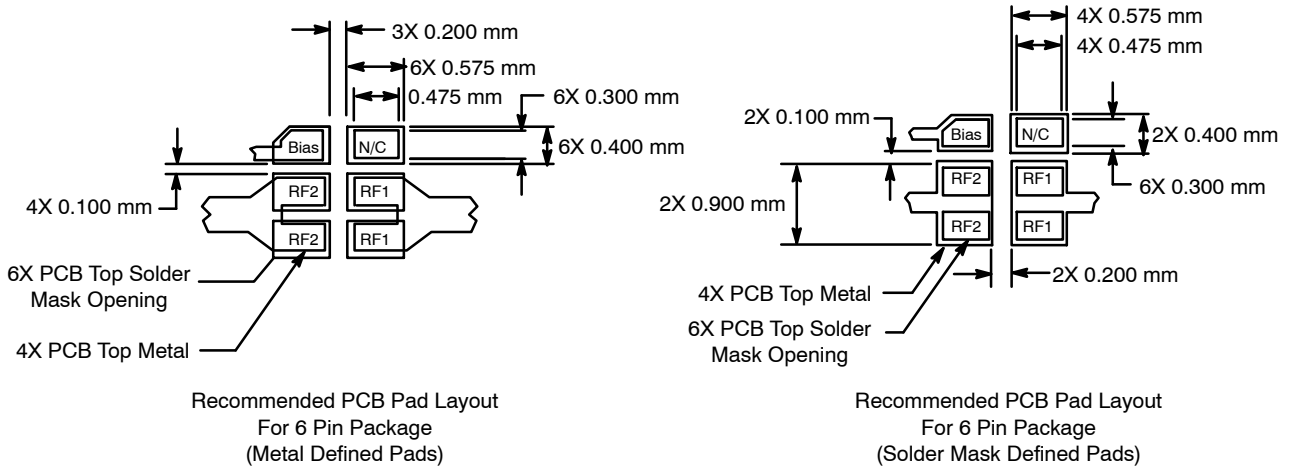
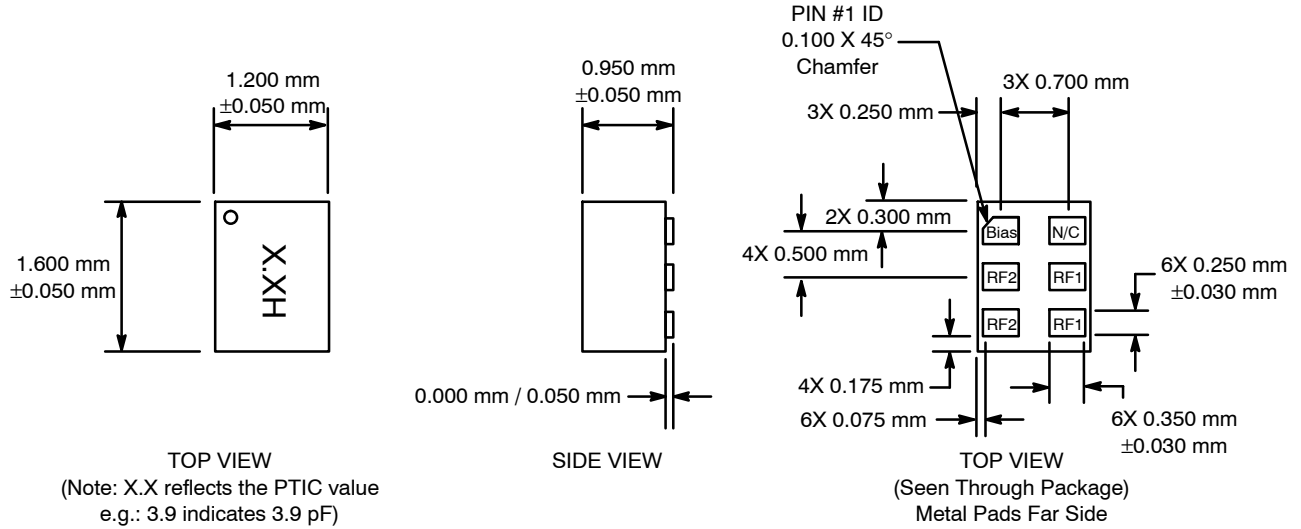
5. WLCSP: Recommended Bias Voltage not to exceed 20 V

6. Class 1A defined as passing 250 V, but may fail after exposure to 500 V ESD pulse

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## PACKAGE INFORMATION

### QFN Package Layout and Dimensional Information



**Note:**

2X means 2 sites with the specific value

3X means 3 sites with the specific value

4X means 4 sites with the specific value

0.9 mm pad layout is standard for all products. Shorter pad layouts can be considered for smaller products.

**Figure 6. QFN Package Dimensions**

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## Wafer Level Chip Scale Package (WLCSP) Layout and Dimensional Information

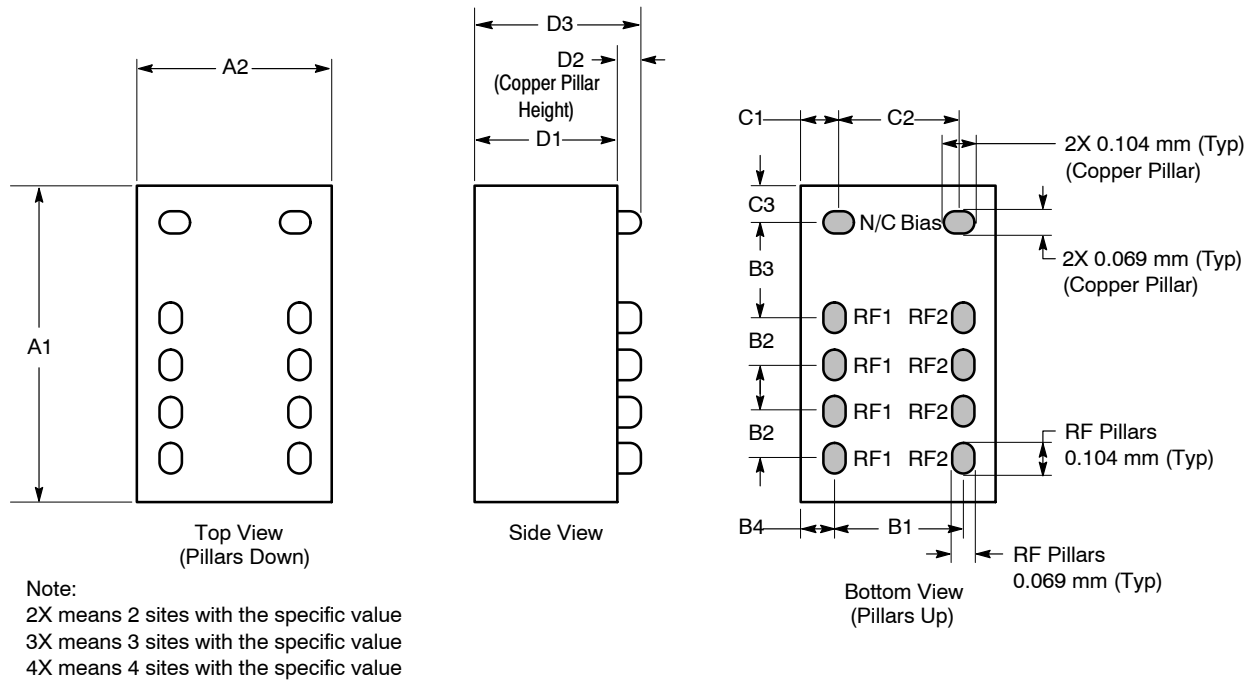


Figure 7. WLCSP Package Dimensions

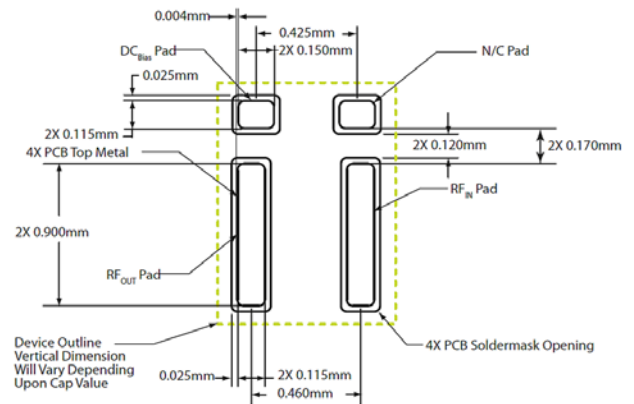
Table 3. PACKAGE DIMENSIONS

(All dimensions are in millimeters)

| WLCSP* | DIM | Nominal | Max | Device                |
|--------|-----|---------|-----|-----------------------|
| 8P     | A1  | 0.879   |     | 1.2, 2.7 pF           |
| 10P    | A1  | 1.029   |     | 3.3, 3.9 pF           |
| 12P    | A1  | 1.179   |     | 4.7, 5.6, 6.8, 8.2 pF |
| 14P    | A1  | 1.329   |     |                       |
| ALL    | A2  | 0.722   |     |                       |
| ALL    | B1  | 0.460   |     |                       |
| ALL    | B2  | 0.150   |     |                       |
| ALL    | B3  | 0.300   |     |                       |
| ALL    | B4  | 0.131   |     |                       |
| ALL    | C1  | 0.1485  |     |                       |
| ALL    | C2  | 0.425   |     |                       |
| ALL    | C3  | 0.130   |     |                       |
| ALL    | D1  | 0.530   |     |                       |
| ALL    | D2  | 0.081   |     |                       |
| ALL    | D3  | 0.611   |     |                       |

\*Total number of pillars

Top View Recommended PCB Pad Layout (Metal Defined Pad)



Note:  
 0.9 mm pad layout is standard for all products. Shorter pad layouts can be considered for smaller products.

Figure 8. Recommended Pad Layout

**ASSEMBLY CONSIDERATIONS AND REFLOW PROFILE**

The following assembly considerations should be observed:

**Cleanliness**

These chips should be handled in a clean environment.

**Electro-static Sensitivity**

ON Semiconductor’s PTICs are ESD Class 1A sensitive. The proper ESD handling procedures should be used.

**Mounting**

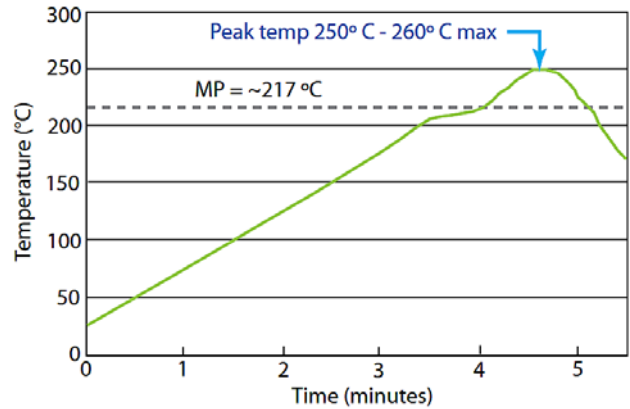
The WLCSP PTIC is fabricated for Flip Chip solder mounting. Connectivity to the RF and Bias terminations on the PTIC die is established through copper pillar posts (53 μm nominal height) topped with lead-free SAC351 solder caps (28 μm nominal height). The PTIC die is RoHS-compliant and compatible with lead-free soldering profile.

**Post-reflow Cleaning**

Use of ultrasonic cleaning is not recommended for pillared devices as it may lead to premature fatigue failure of the pillars.

**Molding**

The PTIC die is compatible for over-molding or under-fill.

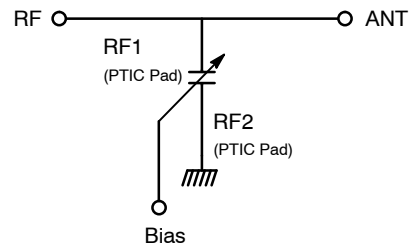


*This reflow profile is a guideline for Pb-free solder materials. Adjustments to this profile are necessary based on specific process requirements and board size, thickness and density. Not to exceed 260° C for 5 seconds.*

**Figure 9. Reflow Profile**

**ORIENTATION OF THE PTIC FOR OPTIMUM LOSSES**

When configuring the PTIC in your specific circuit design, at least one of the RF terminals must be connected to DC ground. If minimum transition times are required, DC ground on both RF terminals is recommended. To minimize losses, the PTIC should be oriented such that RF2 is at the lower RF impedance of the two RF nodes. A shunt PTIC, for example, should have RF2 connected to RF ground.



**Figure 10. PTIC Orientation Functional Block Diagram**

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## PART NUMBER DEFINITION

Example: TCP-3039H-DT

|                       |   |                              |  |                        |   |                         |                |
|-----------------------|---|------------------------------|--|------------------------|---|-------------------------|----------------|
| <b>TCP</b>            | - | <b>30</b>                    | <b>39</b>  | <b>H</b>               | - | <b>D</b>                | <b>T</b>       |
| <u>Product Family</u> |   | <u>Process Generation</u>    | <u>Capacitor Value</u>   | <u>Tuning</u>          |   | <u>Package / Format</u> | <u>Packing</u> |
| TCP                   |   | 10 = Gen 1.0<br>30 = Gen 3.0 | 12 = 1.2 pF<br>27 = 2.7 pF<br>33 = 3.3 pF<br>39 = 3.9 pF<br>47 = 4.7 pF<br>56 = 5.6 pF<br>68 = 6.8 pF<br>82 = 8.2 pF | N = Normal<br>H = High |   | D = WLCSP<br>Q = QFN    | T = T&R        |

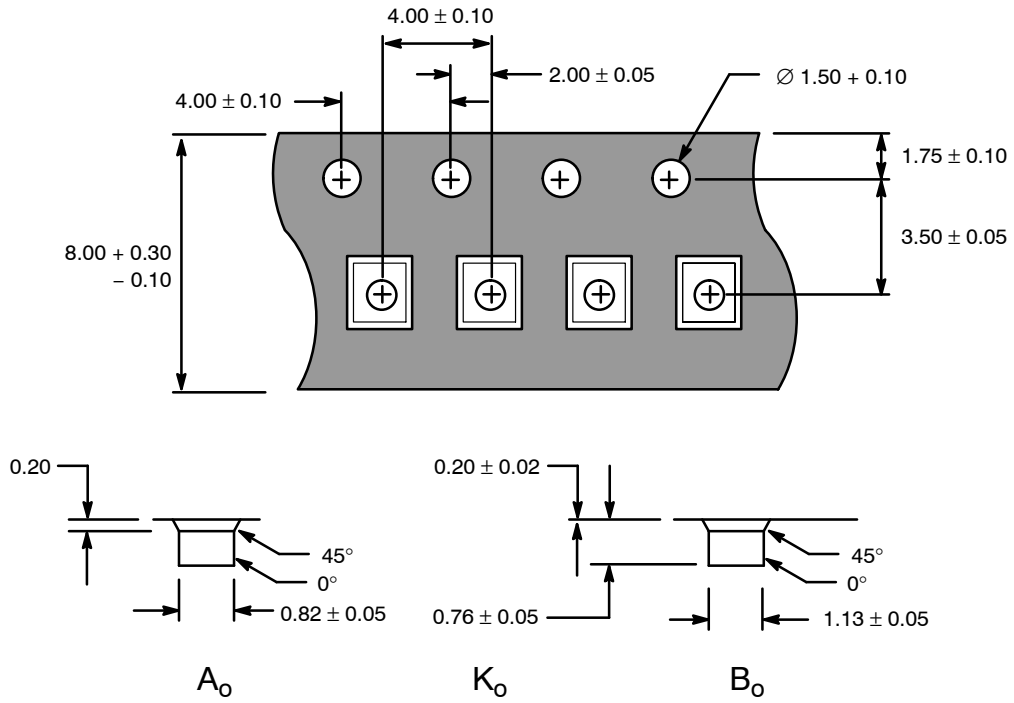
**Table 4. PART NUMBERS**

| Part Number  | Capacitance |      | Package*        |
|--------------|-------------|------|-----------------|
|              | 2 V         | 20 V |                 |
| TCP-3039H-DT | 3.90        | 1    | 10-Pillar WLCSP |
| TCP-3039H-QT | 3.90        | 1    | 6-Pin QFN       |

\*See PTIC package dimensions on page 5

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## TAPE & REEL DIMENSIONS



Note: The reel size is 7"  
Pocket may have a hole 0.2 mm to 0.4 mm  $\pm 0.05$  mm

Figure 11. 10 Pillar WLCSP Carrier Tape Drawing



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## TAPE & REEL DIMENSIONS (Cont'd)

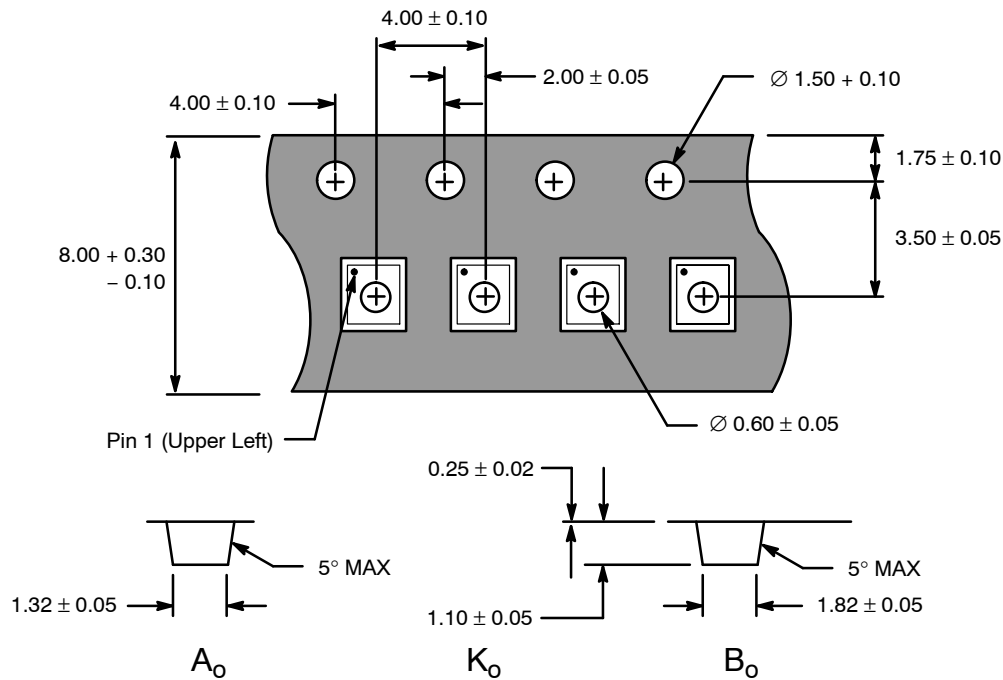


Figure 12. QFN Carrier Tape Drawing

Table 5. POCKET DIMENSION

| Pocket Dimension (mm) |             |      |      | Unit Dimension (mm) |             |      |      |
|-----------------------|-------------|------|------|---------------------|-------------|------|------|
|                       | Spec        | Max  | Min  |                     | Spec        | Max  | Min  |
| Ao                    | 1.32 ± 0.05 | 1.37 | 1.27 | A                   | 1.2 ± 0.05  | 1.25 | 1.15 |
| Bo                    | 1.82 ± 0.05 | 1.87 | 1.77 | B                   | 1.6 ± 0.05  | 1.65 | 1.55 |
| Ko                    | 1.1 ± 0.05  | 1.15 | 1.05 | K                   | 0.95 ± 0.05 | 1.00 | 0.90 |

NOTE: The reel size is 13"

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