

# FOD3150

## High Noise Immunity, 1.0A Output Current, Gate Drive Optocoupler

### Features

- High noise immunity characterized by 20kV/μs minimum common mode rejection
- Use of P-channel MOSFETs at output stage enables output voltage swing close to the supply rail
- Wide supply voltage range from 15V to 30V
- Fast switching speed
  - 500ns max. propagation delay
  - 300ns max. pulse width distortion
- Under Voltage LockOut (UVLO) with hysteresis
- Extended industrial temperature range, -40°C to 100°C temperature range
- Safety and regulatory approvals
  - UL1577, 5000 V<sub>RMS</sub> for 1 min.
  - IEC60747-5-2
- >8.0mm clearance and creepage distance (option 'T')

### Applications

- Industrial inverter
- Uninterruptible power supply
- Induction heating
- Isolated IGBT/Power MOSFET gate drive

### Description

The FOD3150 is a 1.0A Output Current Gate Drive Optocoupler, capable of driving most 800V/20A IGBT/MOSFET. It is ideally suited for fast switching driving of power IGBT and MOSFETs used in motor control inverter applications, and high performance power system.

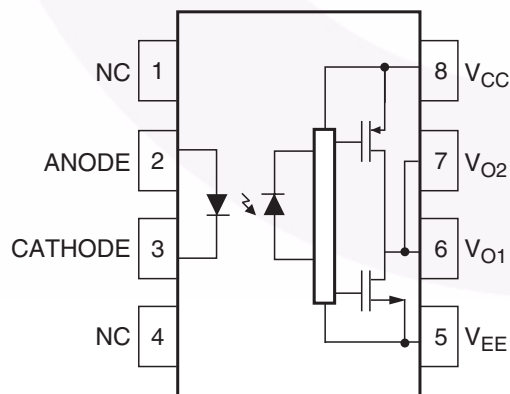
It utilizes Fairchild's patented coplanar packaging technology, Optoplanar<sup>®</sup>, and optimized IC design to achieve high noise immunity, characterized by high common mode rejection.

It consists of a gallium aluminum arsenide (AlGaAs) light emitting diode optically coupled to an integrated circuit with a high-speed driver for push-pull MOSFET output stage.

### Related Resources

- FOD3120, 2.5A Output Current, Gate Drive Optocoupler Datasheet
- [www.fairchildsemi.com/products/opto/](http://www.fairchildsemi.com/products/opto/)

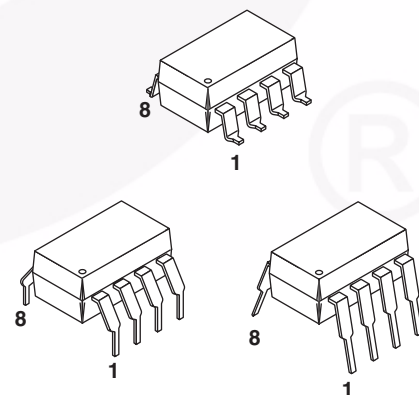
### Functional Block Diagram



**Note:**

A 0.1μF bypass capacitor must be connected between pins 5 and 8.

### Package Outlines



**Truth Table**

LED	$V_{CC}-V_{EE}$ "Positive Going" (Turn-on)	$V_{CC}-V_{EE}$ "Negative Going" (Turn-off)	$V_O$
Off	0V to 30V	0V to 30V	Low
On	0V to 11V	0V to 9.5V	Low
On	11V to 13.5V	9.5V to 12V	Transition
On	13.5V to 30V	12V to 30V	High

**Pin Definitions**

Pin #	Name	Description
1	NC	Not Connected
2	Anode	LED Anode
3	Cathode	LED Cathode
4	NC	Not Connected
5	$V_{EE}$	Negative Supply Voltage
6	$V_{O2}$	Output Voltage 2 (internally connected to $V_{O1}$ )
7	$V_{O1}$	Output Voltage 1
8	$V_{CC}$	Positive Supply Voltage

## Safety and Insulation Ratings

As per IEC 60747-5-2. This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For Rated Main Voltage < 150Vrms		I-IV		
	For Rated Main Voltage < 300Vrms		I-IV		
	For Rated Main Voltage < 450Vrms		I-III		
	For Rated Main Voltage < 600Vrms		I-III		
	Climatic Classification		55/100/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V <sub>PR</sub>	Input to Output Test Voltage, Method b, V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Test with t <sub>m</sub> = 1 sec., Partial Discharge < 5pC	1669			
	Input to Output Test Voltage, Method a, V <sub>IORM</sub> × 1.5 = V <sub>PR</sub> , Type and Sample Test with t <sub>m</sub> = 60 sec., Partial Discharge < 5 pC	1335			
V <sub>IORM</sub>	Max Working Insulation Voltage	890			V <sub>peak</sub>
V <sub>IOTM</sub>	Highest Allowable Over Voltage	6000			V <sub>peak</sub>
	External Creepage	8			mm
	External Clearance	7.4			mm
	External Clearance (for Option T-0.4" Lead Spacing)	10.16			mm
	Insulation Thickness	0.5			mm
T <sub>Case</sub>	Safety Limit Values – Maximum Values Allowed in the Event of a Failure				
	Case Temperature	150			°C
I <sub>S,INPUT</sub>	Input Current	25			mA
P <sub>S,OUTPUT</sub>	Output Power (Duty Factor ≤ 2.7%)	250			mW
R <sub>IO</sub>	Insulation Resistance at T <sub>S</sub> , V <sub>IO</sub> = 500V	10 <sup>9</sup>			Ω

**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
$T_{STG}$	Storage Temperature	-55 to +125	$^\circ\text{C}$
$T_{OPR}$	Operating Temperature	-40 to +100	$^\circ\text{C}$
$T_J$	Junction Temperature	-40 to +125	$^\circ\text{C}$
$T_{SOL}$	Lead Wave Solder Temperature (refer to page 19 for reflow solder profile)	260 for 10sec	$^\circ\text{C}$
$I_{F(AVG)}$	Average Input Current	25	mA
$V_R$	Reverse Input Voltage	5	V
$I_{O(PEAK)}$	Peak Output Current <sup>(1)</sup>	1.5	A
$V_{CC} - V_{EE}$	Supply Voltage	0 to 35	V
$V_{O(PEAK)}$	Peak Output Voltage	0 to $V_{CC}$	V
$t_{R(IN)}, t_{F(IN)}$	Input Signal Rise and Fall Time	500	ns
$PD_I$	Input Power Dissipation <sup>(2)(4)</sup>	45	mW
$PD_O$	Output Power Dissipation <sup>(3)(4)</sup>	250	mW

**Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Value	Units
$T_A$	Ambient Operating Temperature	-40 to +100	$^\circ\text{C}$
$V_{CC} - V_{EE}$	Power Supply	15 to 30	V
$I_{F(ON)}$	Input Current (ON)	7 to 16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	0 to 0.8	V

**Isolation Characteristics**

Apply over all recommended conditions, typical value is measured at  $T_A = 25^\circ\text{C}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{ISO}$	Input-Output Isolation Voltage	$T_A = 25^\circ\text{C}$ , R.H. < 50%, $t = 1.0\text{min}$ , $I_{I-O} \leq 10\mu\text{A}$ , 50Hz <sup>(5)(6)</sup>	5000			$V_{RMS}$
$R_{ISO}$	Isolation Resistance	$V_{I-O} = 500\text{V}^{(5)}$		$10^{11}$		$\Omega$
$C_{ISO}$	Isolation Capacitance	$V_{I-O} = 0\text{V}$ , Freq = 1.0MHz <sup>(5)</sup>		1		pF

## Electrical Characteristics

Apply over all recommended conditions, typical value is measured at  $V_{CC} = 30V$ ,  $V_{EE} = \text{Ground}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_F$	Input Forward Voltage	$I_F = 10\text{mA}$	1.2	1.5	1.8	V
$\Delta(V_F / T_A)$	Temperature Coefficient of Forward Voltage			-1.8		mV/°C
$BV_R$	Input Reverse Breakdown Voltage	$I_R = 10\mu\text{A}$	5			V
$C_{IN}$	Input Capacitance	$f = 1\text{MHz}$ , $V_F = 0V$		60		pF
$I_{OH}$	High Level Output Current <sup>(1)</sup>	$V_O = V_{CC} - 0.75V$	0.2			A
		$V_O = V_{CC} - 4V$	1.0			
$I_{OL}$	Low Level Output Current <sup>(1)</sup>	$V_O = V_{CC} + 0.75V$	0.2			A
		$V_O = V_{CC} + 4V$	1.0			
$V_{OH}$	High Level Output Voltage	$I_F = 10\text{mA}$ , $I_O = -1A$	$V_{CC} - 4V$	$V_{CC} - 6V$		V
		$I_F = 10\text{mA}$ , $I_O = -100\text{mA}$	$V_{CC} - 0.5V$	$V_{CC} - 0.1V$		
$V_{OL}$	Low Level Output Voltage	$I_F = 0\text{mA}$ , $I_O = 1A$		$V_{EE} + 6V$	$V_{EE} + 4V$	V
		$I_F = 0\text{mA}$ , $I_O = 100\text{mA}$		$V_{EE} + 0.1V$	$V_{EE} + 0.5V$	
$I_{CCH}$	High Level Supply Current	$V_O = \text{Open}$ , $I_F = 7$ to $16\text{mA}$		2.8	5	mA
$I_{CCL}$	Low Level Supply Current	$V_O = \text{Open}$ , $V_F = 0$ to $0.8V$		2.8	5	mA
$I_{FLH}$	Threshold Input Current Low to High	$I_O = 0\text{mA}$ , $V_O > 5V$		2.3	5.0	mA
$V_{FHL}$	Threshold Input Voltage High to Low	$I_O = 0\text{mA}$ , $V_O < 5V$	0.8			V
$V_{UVLO+}$	Under Voltage Lockout Threshold	$I_F = 10\text{mA}$ , $V_O > 5V$	11	12.7	13.5	V
$V_{UVLO-}$		$I_F = 10\text{mA}$ , $V_O < 5V$	9.5	11.2	12.0	V
$UVLO_{HYS}$	Under Voltage Lockout Threshold Hysteresis			1.5		V

## Switching Characteristics

Apply over all recommended conditions, typical value is measured at  $V_{CC} = 30V$ ,  $V_{EE} = \text{Ground}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise specified.

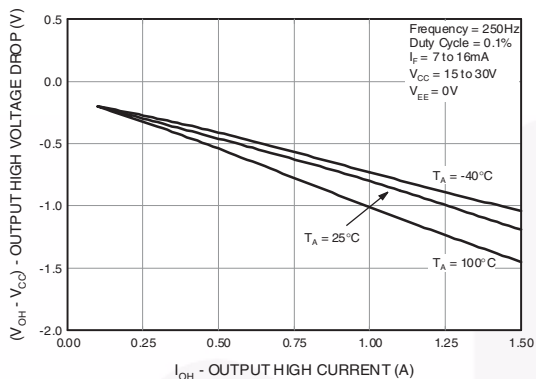
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{PHL}$	Propagation Delay Time to Logic Low Output	$I_F = 7\text{mA to } 16\text{mA}$ , $R_G = 20\Omega$ , $C_G = 10\text{nF}$ , $f = 10\text{kHz}$ , Duty Cycle = 50%	100	275	500	ns
$t_{PLH}$	Propagation Delay Time to Logic High Output		100	255	500	ns
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $			20	300	ns
PDD (Skew)	Propagation Delay Difference Between Any Two Parts or Channels, $(t_{PHL} - t_{PLH})^{(7)}$			-350	350	ns
$t_r$	Output Rise Time (10% – 90%)				60	ns
$t_f$	Output Fall Time (90% – 10%)				60	ns
$t_{UVLO\ ON}$	UVLO Turn On Delay		$I_F = 10\text{mA}$ , $V_O > 5V$		1.6	
$t_{UVLO\ OFF}$	UVLO Turn Off Delay	$I_F = 10\text{mA}$ , $V_O < 5V$		0.4		$\mu\text{s}$
$ CM_H $	Common Mode Transient Immunity at Output High	$T_A = 25^\circ\text{C}$ , $V_{CC} = 30V$ , $I_F = 7 \text{ to } 16\text{mA}$ , $V_{CM} = 2000V^{(8)}$	20	50		$\text{kV}/\mu\text{s}$
$ CM_L $	Common Mode Transient Immunity at Output Low	$T_A = 25^\circ\text{C}$ , $V_{CC} = 30V$ , $V_F = 0V$ , $V_{CM} = 2000V^{(9)}$	20	50		$\text{kV}/\mu\text{s}$

### Notes:

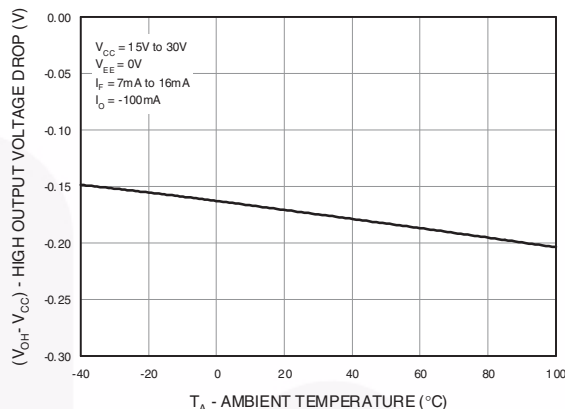
- Maximum pulse width =  $10\mu\text{s}$ , maximum duty cycle = 0.2%
- Derate linearly above  $87^\circ\text{C}$ , free air temperature at a rate of  $0.77\text{mW}/^\circ\text{C}$
- No derating required across temperature range.
- Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.
- Device is considered a two terminal device: Pins 2 and 3 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
- $5,000 V_{RMS}$  for 1 minute duration is equivalent to  $6,000 V_{AC\ RMS}$  for 1 second duration.
- The difference between  $t_{PHL}$  and  $t_{PLH}$  between any two FOD3150 parts under same test conditions.
- Common mode transient immunity at output high is the maximum tolerable negative  $dV_{cm}/dt$  on the trailing edge of the common mode impulse signal,  $V_{cm}$ , to assure that the output will remain high (i.e.  $V_O > 15.0V$ ).
- Common mode transient immunity at output low is the maximum tolerable positive  $dV_{cm}/dt$  on the leading edge of the common pulse signal,  $V_{cm}$ , to assure that the output will remain low (i.e.  $V_O < 1.0V$ ).

## Typical Performance Curves

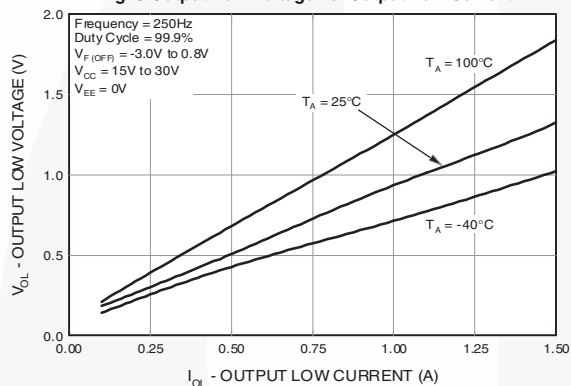
**Fig. 1 Output High Voltage Drop vs. Output High Current**



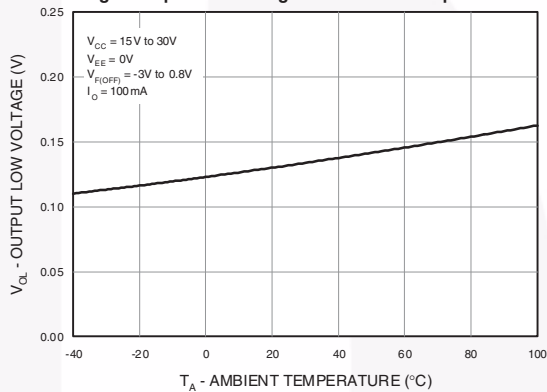
**Fig. 2 Output High Voltage Drop vs. Ambient Temperature**



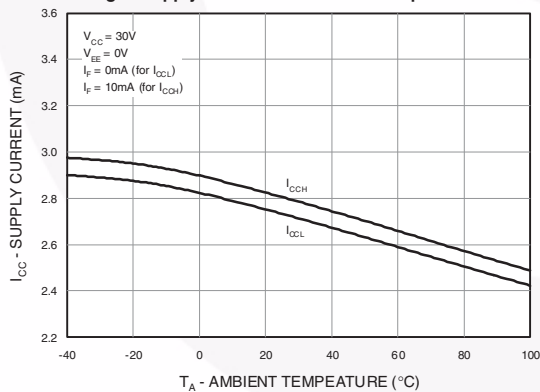
**Fig. 3 Output Low Voltage vs. Output Low Current**



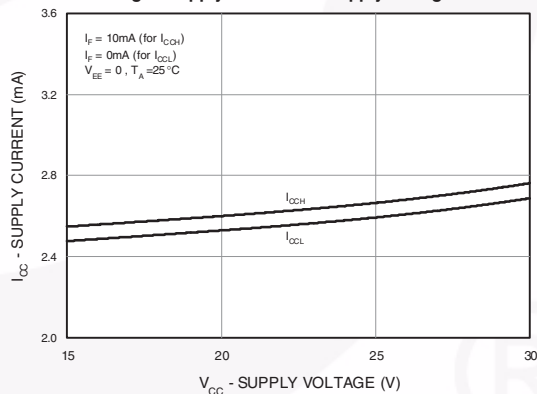
**Fig. 4 Output Low Voltage vs. Ambient Temperature**



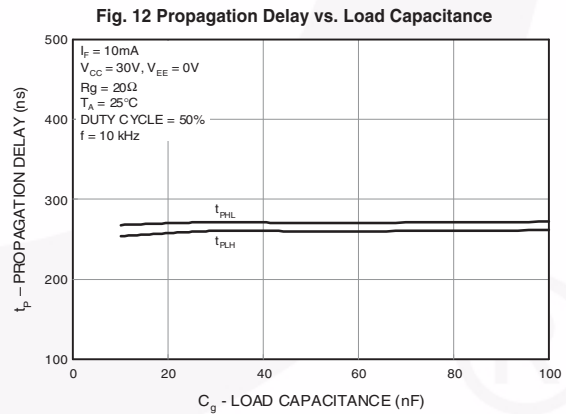
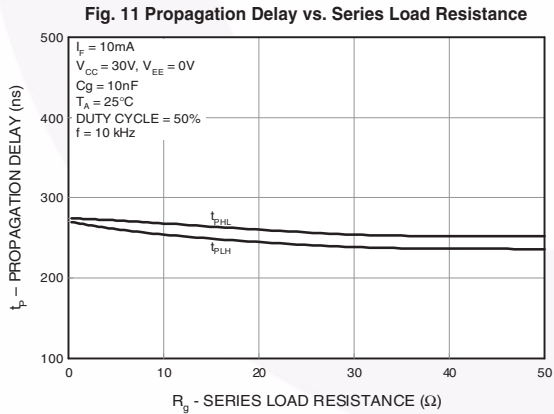
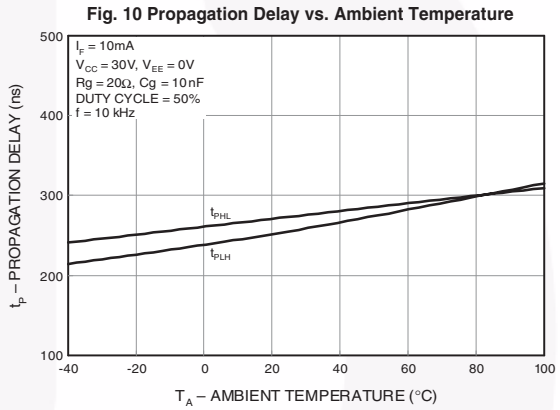
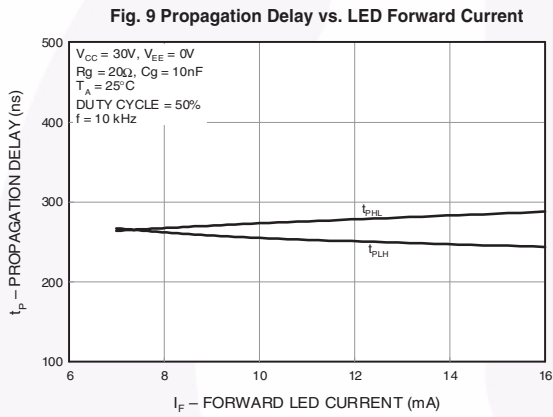
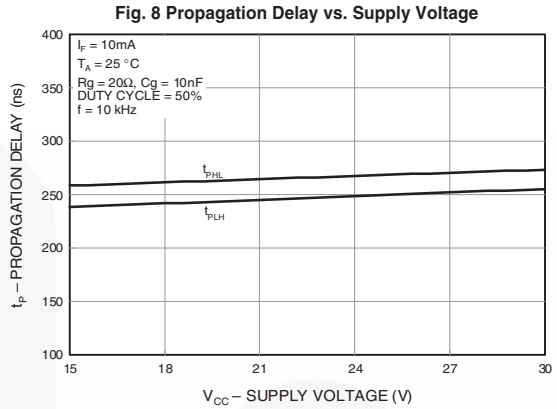
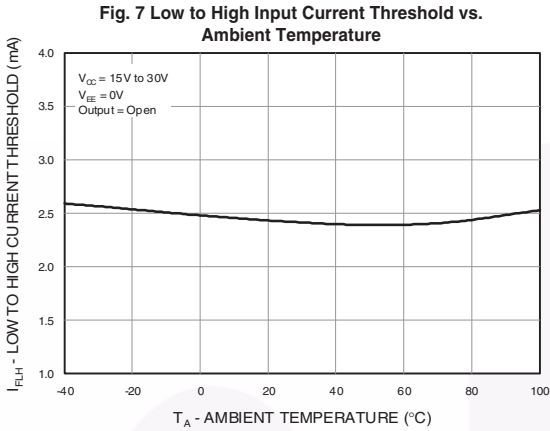
**Fig. 5 Supply Current vs. Ambient Temperature**



**Fig. 6 Supply Current vs. Supply Voltage**



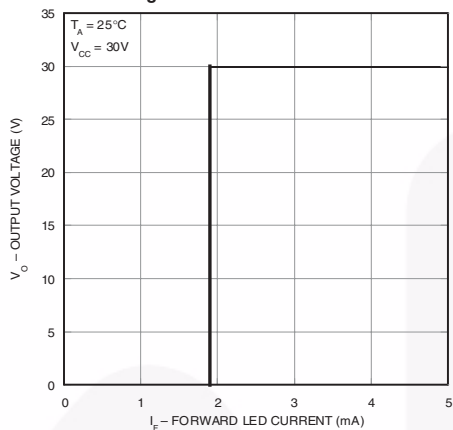
**Typical Performance Curves (Continued)**



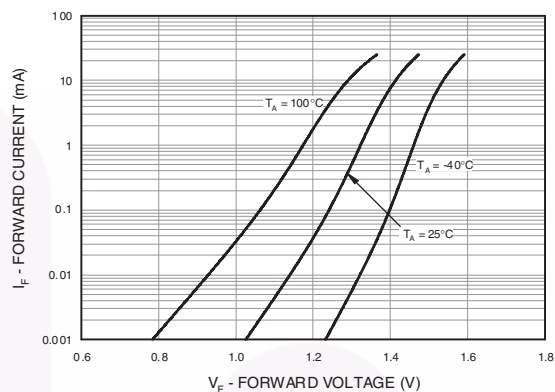


## Typical Performance Curves (Continued)

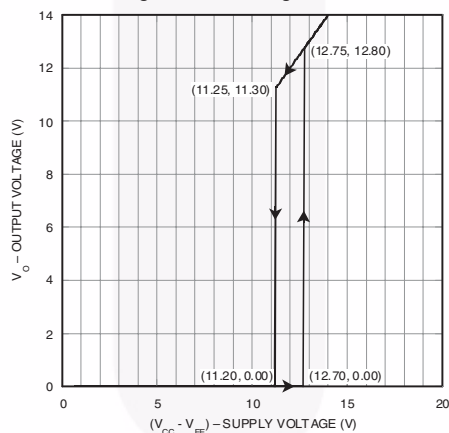
**Fig. 13 Transfer Characteristics**



**Fig. 14 Input Forward Current vs. Forward Voltage**



**Fig. 15 Under Voltage Lockout**



### Test Circuit

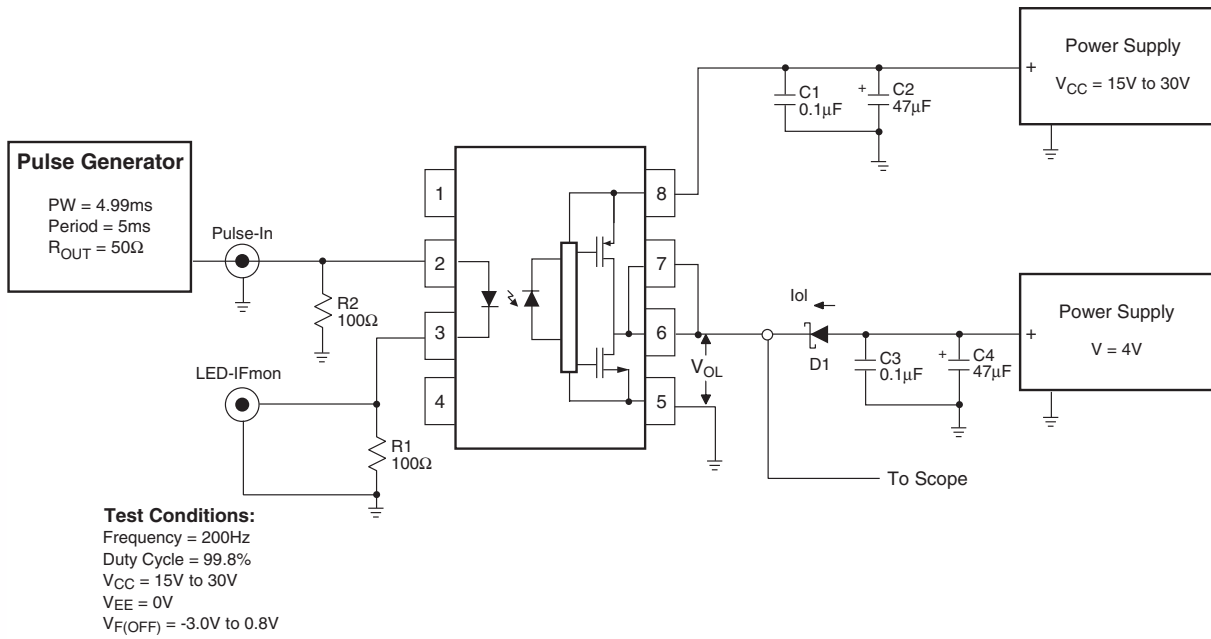


Figure 20.  $I_{OL}$  Test Circuit

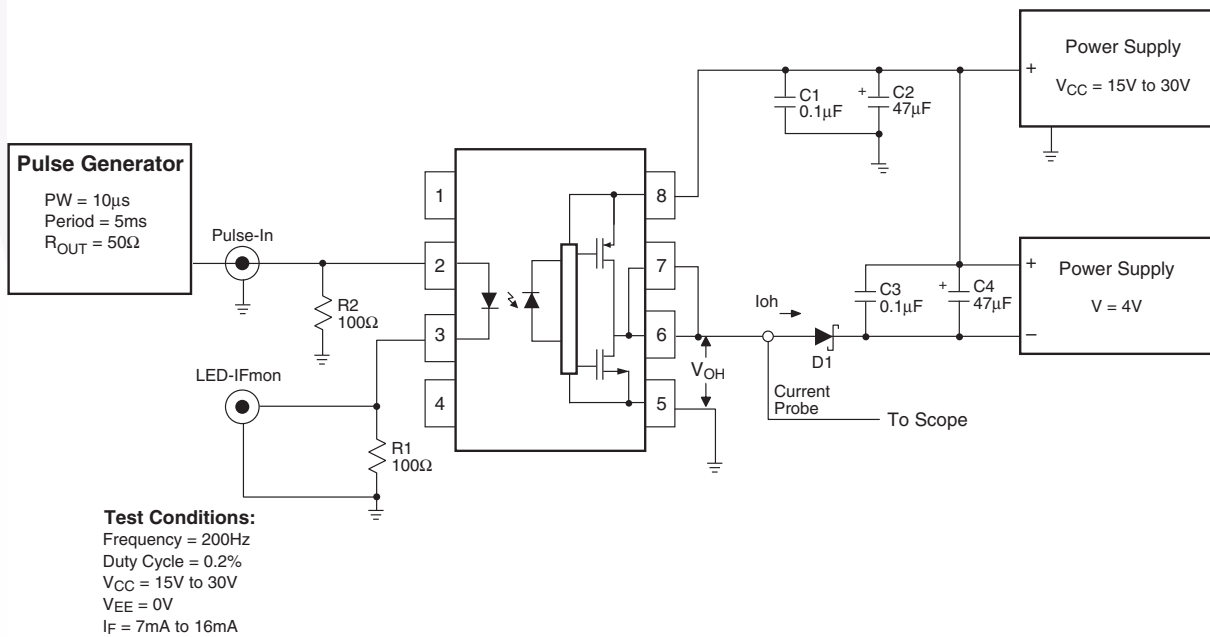


Figure 21.  $I_{OH}$  Test Circuit

Test Circuit (Continued)

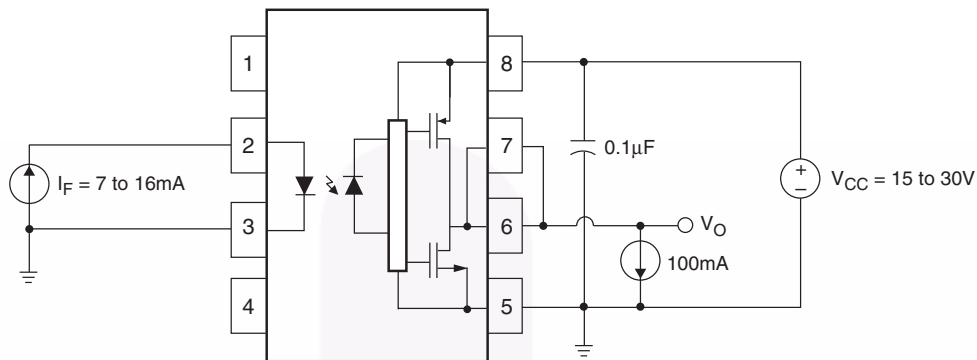


Figure 22.  $V_{OH}$  Test Circuit

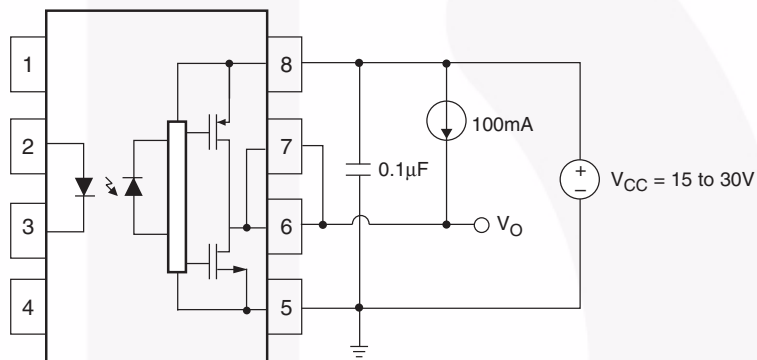
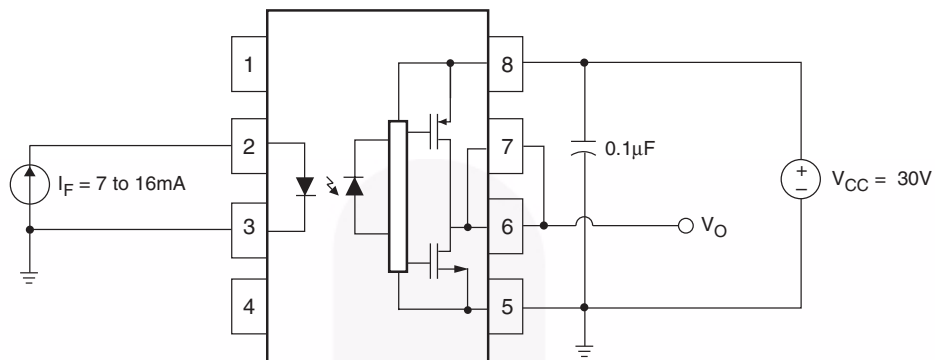


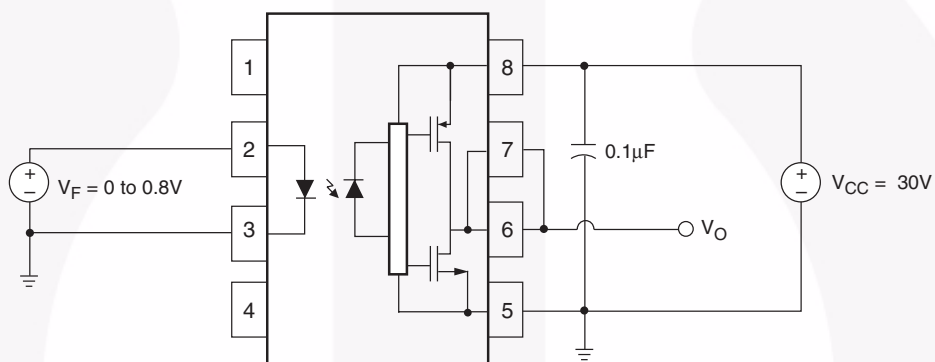
Figure 23.  $V_{OL}$  Test Circuit



**Test Circuit** (Continued)



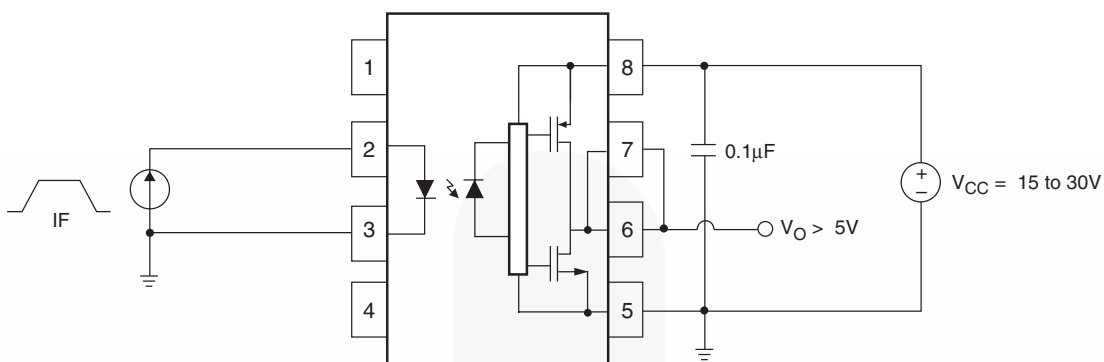
**Figure 24.  $I_{CCH}$  Test Circuit**



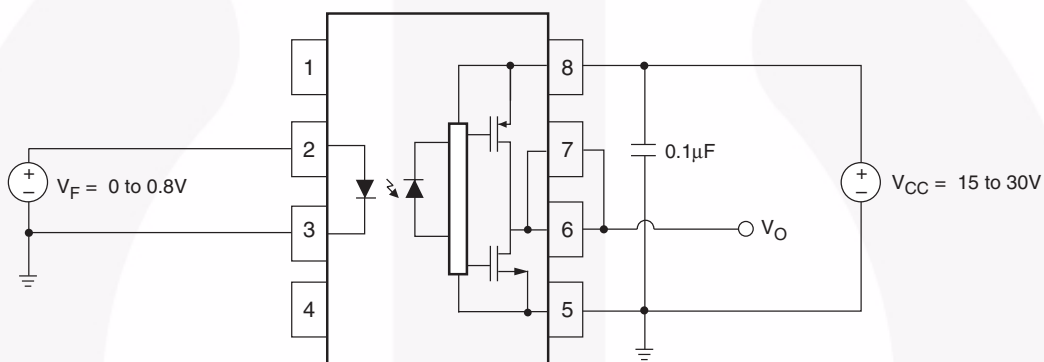
**Figure 25.  $I_{CCL}$  Test Circuit**



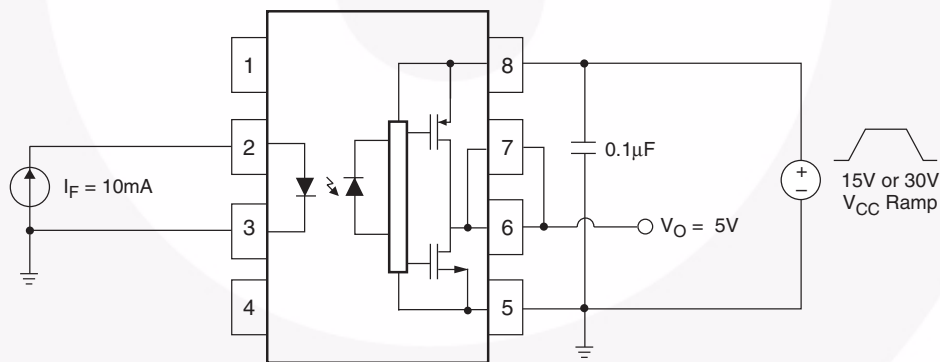
**Test Circuit** (Continued)



**Figure 26.  $I_{FLH}$  Test Circuit**

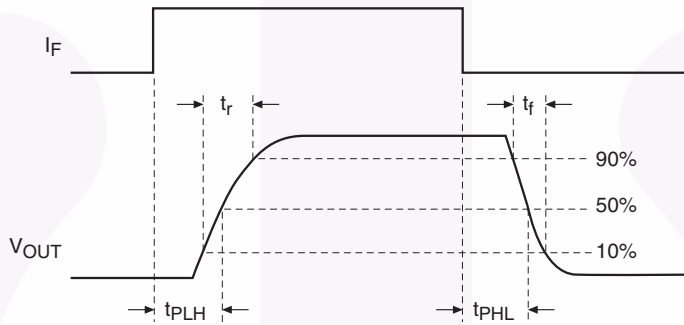
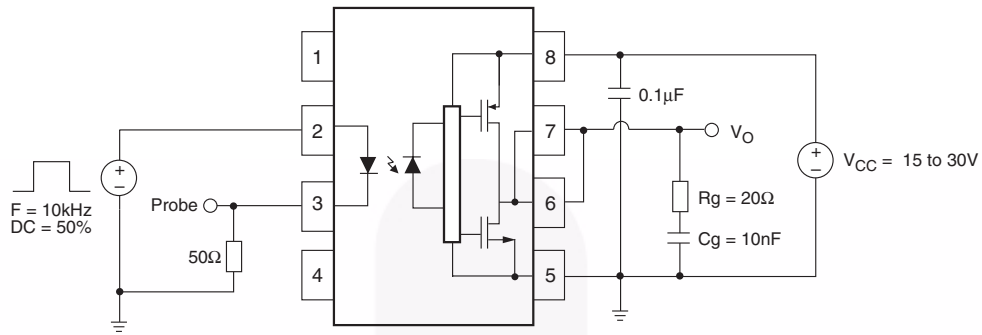


**Figure 27.  $V_{FHL}$  Test Circuit**

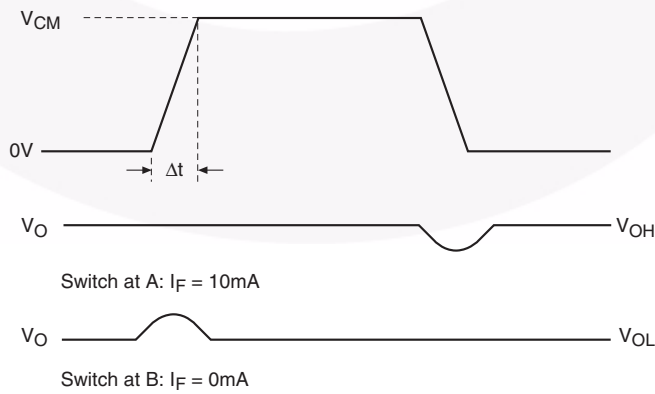
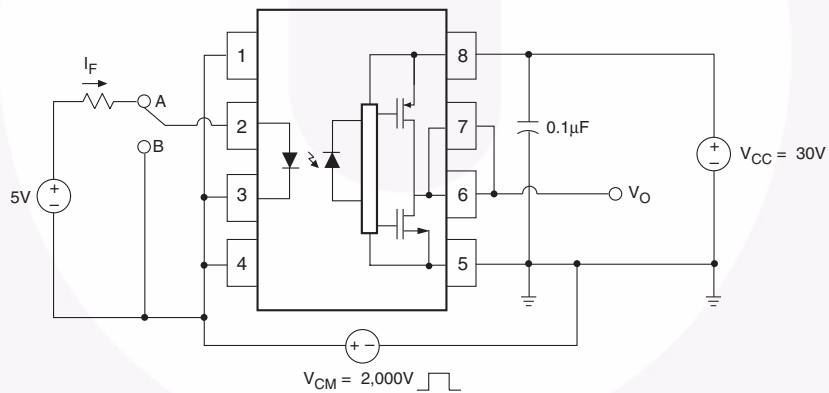


**Figure 28. UVLO Test Circuit**

**Test Circuit (Continued)**



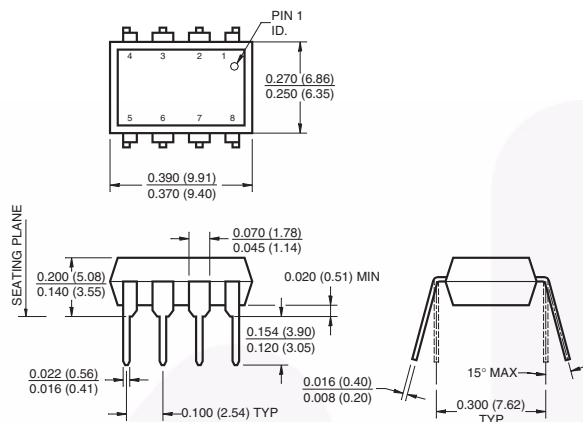
**Figure 29.  $t_{pHL}$ ,  $t_{pLH}$ ,  $t_R$  and  $t_F$  Test Circuit and Waveforms**



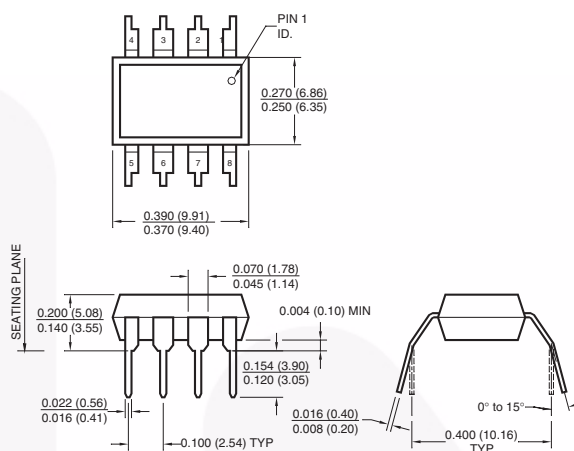
**Figure 30. CMR Test Circuit and Waveforms**

## Package Dimensions

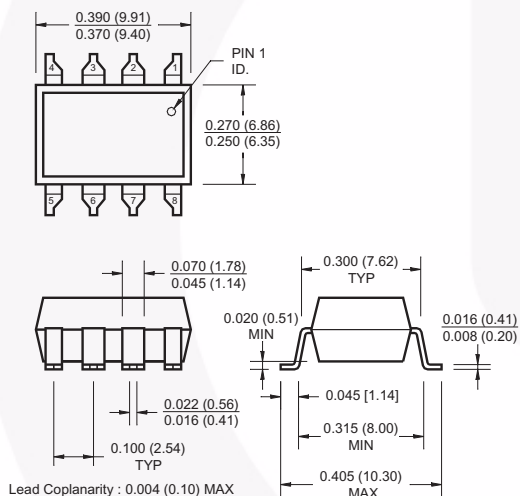
### Through Hole



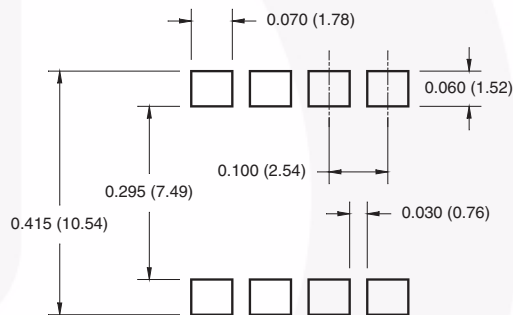
### 0.4" Lead Spacing



### Surface Mount



### 8-Pin DIP – Land Pattern



#### Note:

All dimensions are in inches (millimeters)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

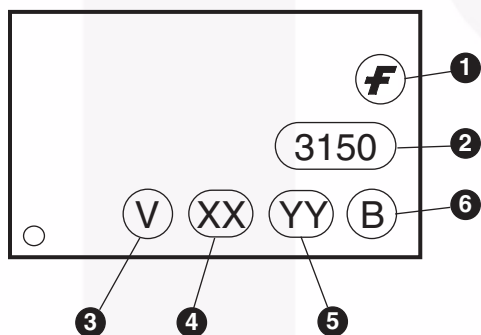
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

## Ordering Information

Part Number	Package	Packing Method
FOD3150	DIP 8-Pin	Tube (50 units per tube)
FOD3150S	SMT 8-Pin (Lead Bend)	Tube (50 units per tube)
FOD3150SD	SMT 8-Pin (Lead Bend)	Tape and Reel (1,000 units per reel)
FOD3150V	DIP 8-Pin, IEC60747-5-2 option	Tube (50 units per tube)
FOD3150SV	SMT 8-Pin (Lead Bend), IEC60747-5-2 option	Tube (50 units per tube)
FOD3150SDV	SMT 8-Pin (Lead Bend), IEC60747-5-2 option	Tape and Reel (1,000 units per reel)
FOD3150T	DIP 8-Pin, 0.4" Lead Spacing	Tube (50 units per tube)
FOD3150TV	DIP 8-Pin, 0.4" Lead Spacing , IEC60747-5-2 option	Tube (50 units per tube)

## Marking Information

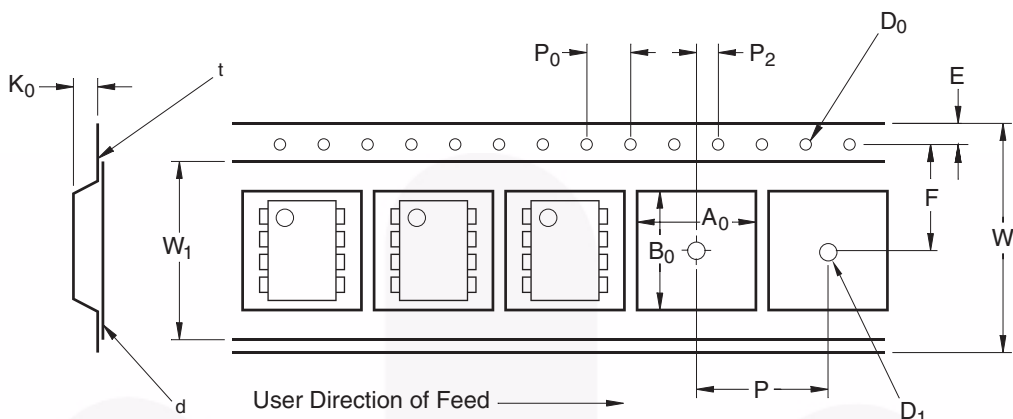


### Definitions

1	Fairchild logo
2	Device number
3	IEC60747-5-2 Option (only appears on component ordered with this option)
4	Two digit year code, e.g., '08'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

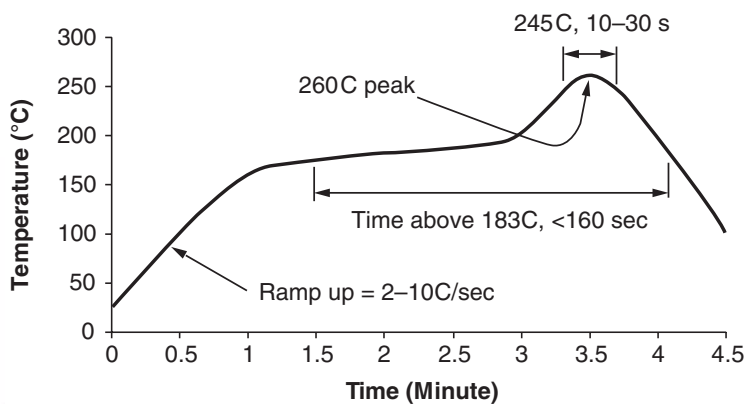


## Carrier Tape Specifications



Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P <sub>0</sub>	Sprocket Hole Pitch	4.0 ± 0.1
D <sub>0</sub>	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P <sub>2</sub>		2.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A <sub>0</sub>	Pocket Dimensions	10.30 ± 0.20
B <sub>0</sub>		10.30 ± 0.20
K <sub>0</sub>		4.90 ± 0.20
W <sub>1</sub>	Cover Tape Width	13.2 ± 0.2
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

## Reflow Profile








- Peak reflow temperature: 260C (package surface temperature)
- Time of temperature higher than 183C for 160 seconds or less
- One time soldering reflow is recommended





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