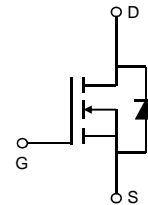
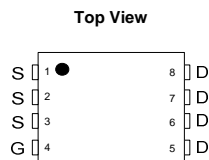


General Description

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Very Low RDS(on) at 4.5V_{GS}
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

Features

V _{DS}	30V
I _D (at V _{GS} =10V)	85A
R _{DS(ON)} (at V _{GS} =10V)	< 2.2mΩ
R _{DS(ON)} (at V _{GS} = 4.5V)	< 2.7mΩ



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current ^G	I _D	T _C =25°C	85
		T _C =100°C	66
Pulsed Drain Current ^C	I _{DM}	334	A
Continuous Drain Current	I _{DSM}	T _A =25°C	49
		T _A =70°C	39
Avalanche Current ^C	I _{AS}	70	A
Avalanche energy L=0.05mH ^C	E _{AS}	123	mJ
V _{DS} Spike	V _{SPIKE}	36	V
Power Dissipation ^B	P _D	T _C =25°C	83
		T _C =100°C	33
Power Dissipation ^A	P _{DSM}	T _A =25°C	7.4
		T _A =70°C	4.7
Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	R _{θJA}	14	17	°C/W
Maximum Junction-to-Ambient ^{A D}		Steady-State	40	55
Maximum Junction-to-Case	R _{θJC}	1.1	1.5	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	1.5	2	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		1.7	2.2	mΩ
		V _{GS} =4.5V, I _D =20A		2.2	2.7	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		85		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current ^G				85	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance			3430		pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		1327		pF
C _{rss}	Reverse Transfer Capacitance			175		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.3	0.7	1.1	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		53	64	nC
Q _{g(4.5V)}	Total Gate Charge			25	30	nC
Q _{gs}	Gate Source Charge			7.8		nC
Q _{gd}	Gate Drain Charge			10.3		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		7.5		ns
t _r	Turn-On Rise Time			5.0		ns
t _{D(off)}	Turn-Off DelayTime			33.8		ns
t _f	Turn-Off Fall Time			9.8		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs		22		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs		58		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

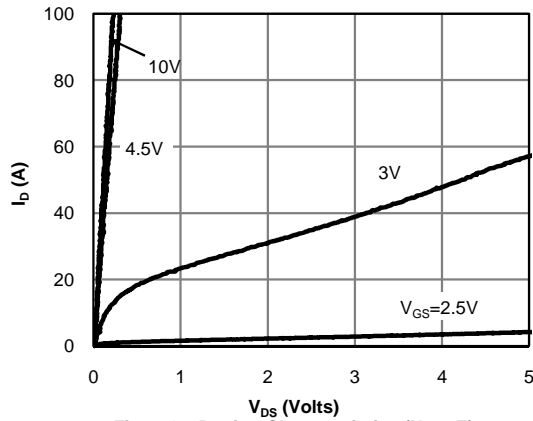


Fig 1: On-Region Characteristics (Note E)

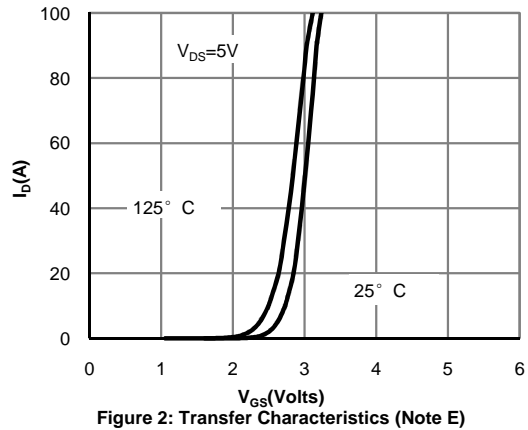


Figure 2: Transfer Characteristics (Note E)

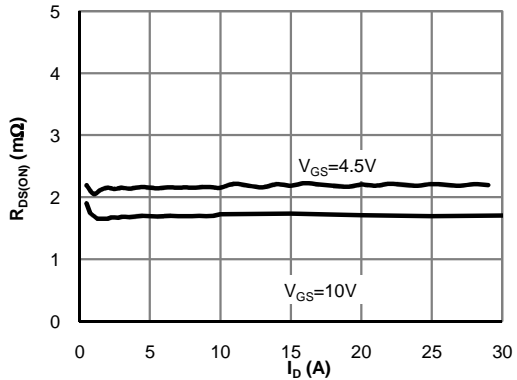


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

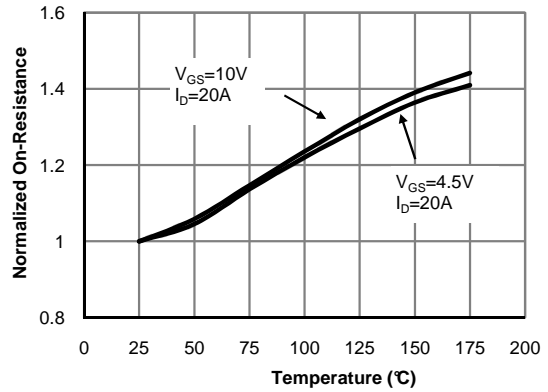


Figure 4: On-Resistance vs. Junction Temperature (Note E)

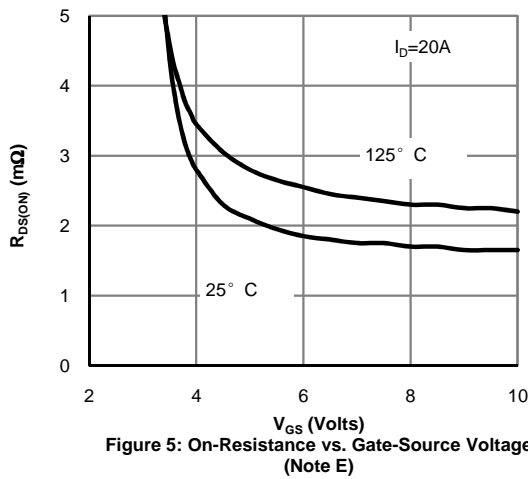


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

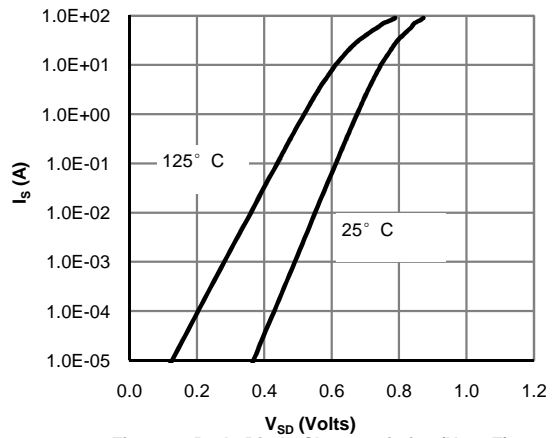


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

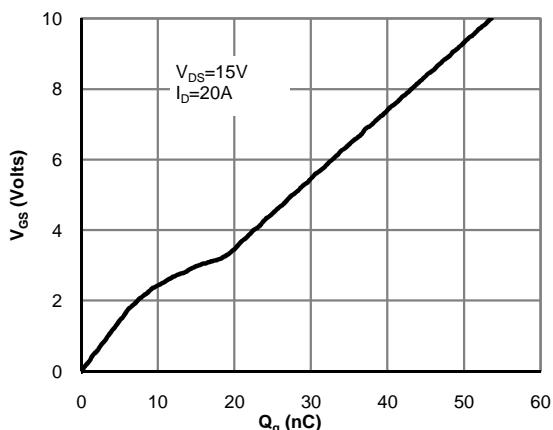


Figure 7: Gate-Charge Characteristics

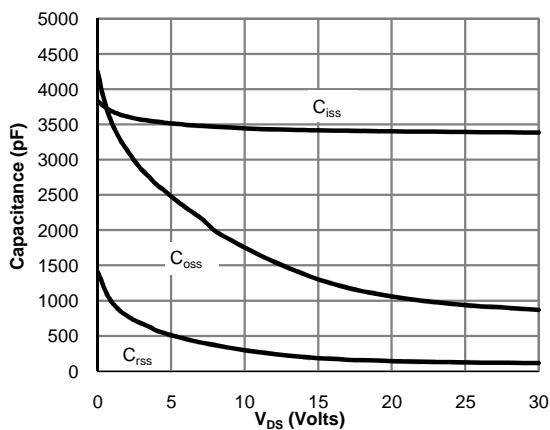


Figure 8: Capacitance Characteristics

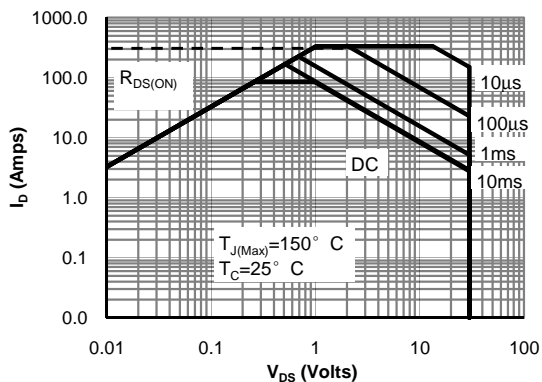


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

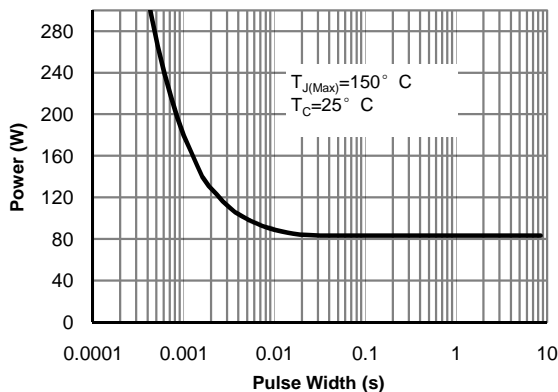


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

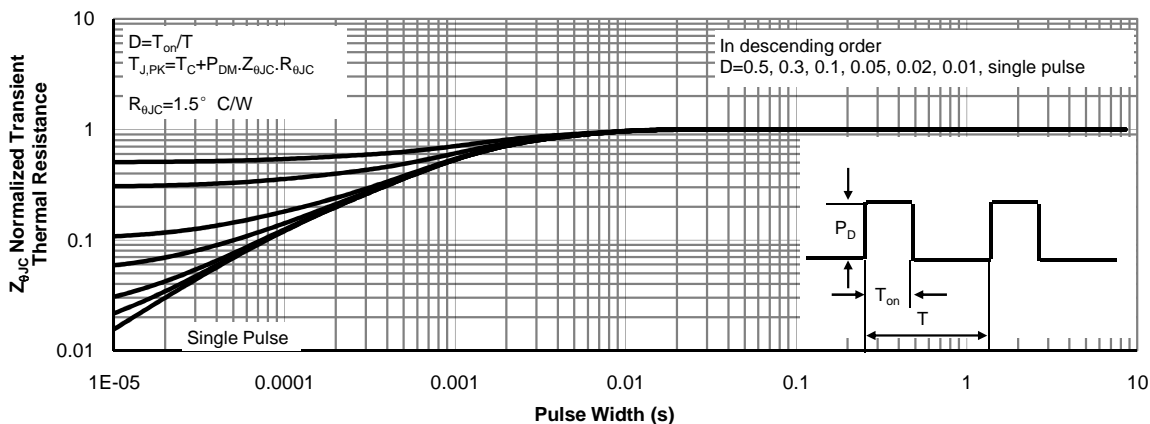


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

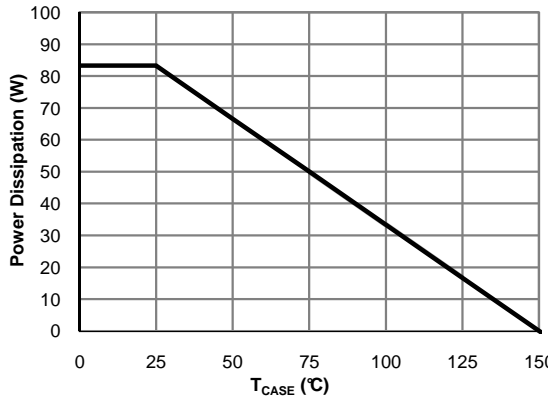


Figure 12: Power De-rating (Note F)

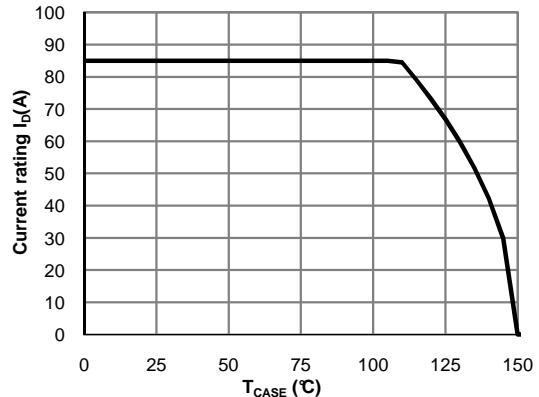


Figure 13: Current De-rating (Note F)

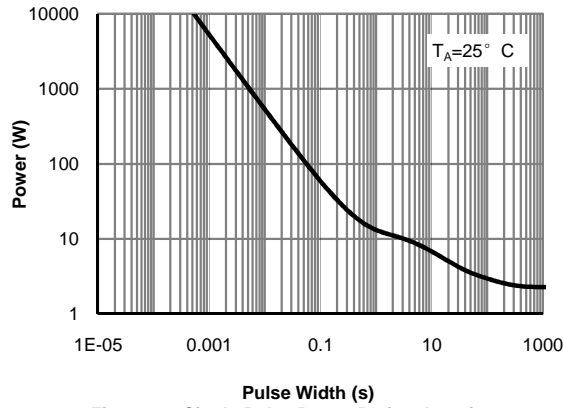


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

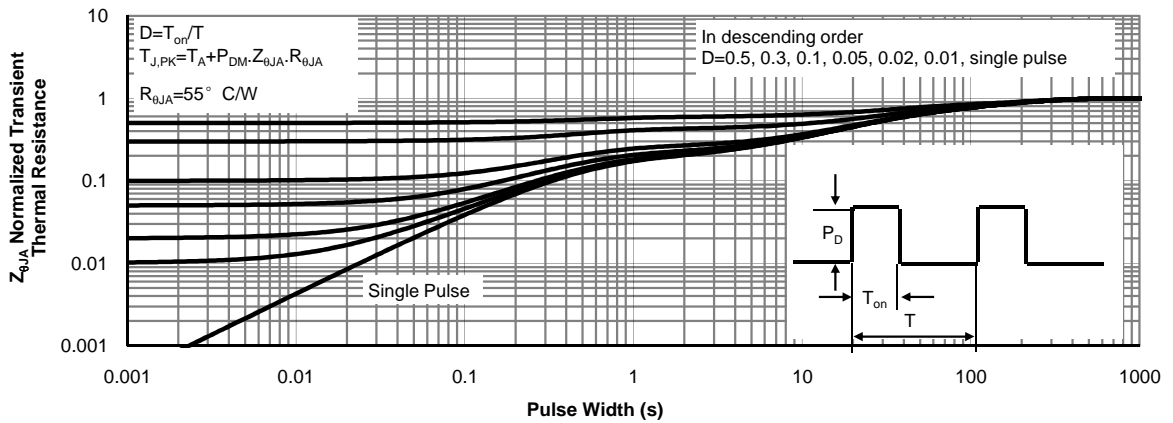
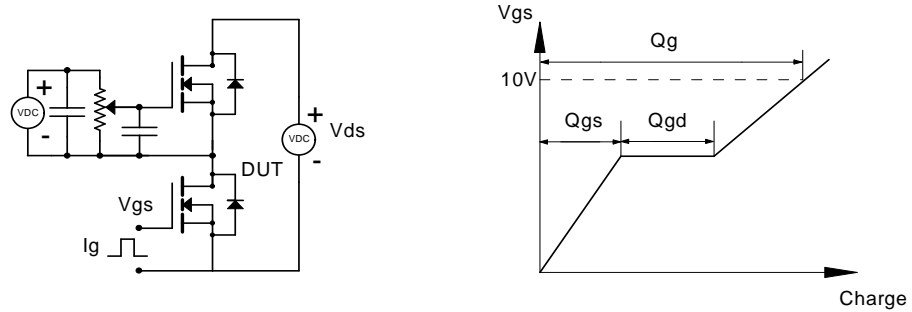
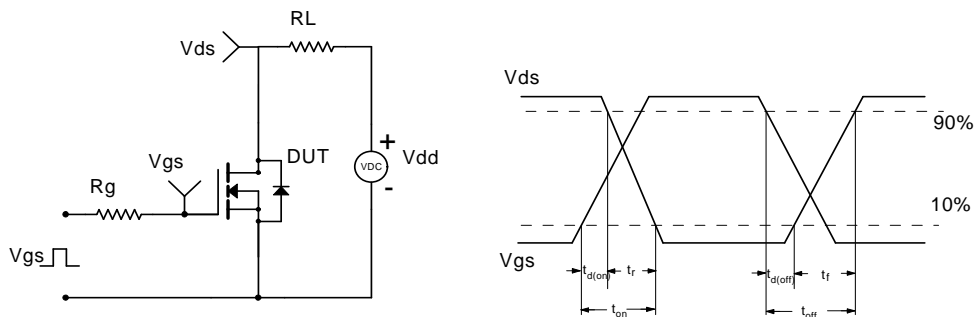


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

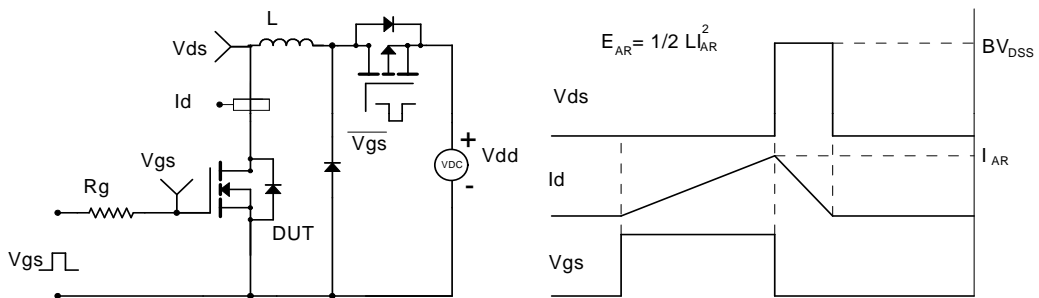
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

