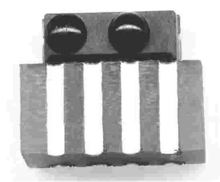
Integrated Low Profile Transceiver Module for Telecom Applications – IrDA Standard

Description

The miniaturized TFDU4201 is an ideal transceiver for applications in telecommunications like mobile phones and pagers. The infrared transceiver is compatible to the IrDA Low Power physical layer specification up to a data rate of 115 kbit/s. TFDU4201A is a TFDU4201 attached to a 4.75 mm spacer.

TFDU4201A is electrically identical with TFDU4201. The only difference is that these devices are soldered to a PCB as spacer to be compliant with a customer demand for centering the optical axis to a given window.

Package



Features

- Package Dimension: L 9.9 mm x W 6.1 mm x H 7.6 mm
- Compatible to IrDA Low Power Standard
- SMD Side View
- Lowest Power Consumption 55 µA Receive Mode, 1 µA Shutdown
- Only 30 mA IRED Peak Current During Transmission
- Wide Supply Voltage Range (2.4 V to 3.6 V)
- Operational down to 2.0 V
- Fewest External Components
- Internal Current Control
- Tri–State Output (Rxd)
- High EMI Immunity
- **SD Pin**

Applications

Mobile Phones, Pagers, Personal Digital Assistants (PDA), Handheld Battery Operated Equipment

Ordering Information

Part Number	Qty / Reel	Description
TFDU4201A–TR3	600	Oriented in carrier tape for side view mounting, TFDU4201 on a 4.75 mm thick spacer

Functional Block Diagram

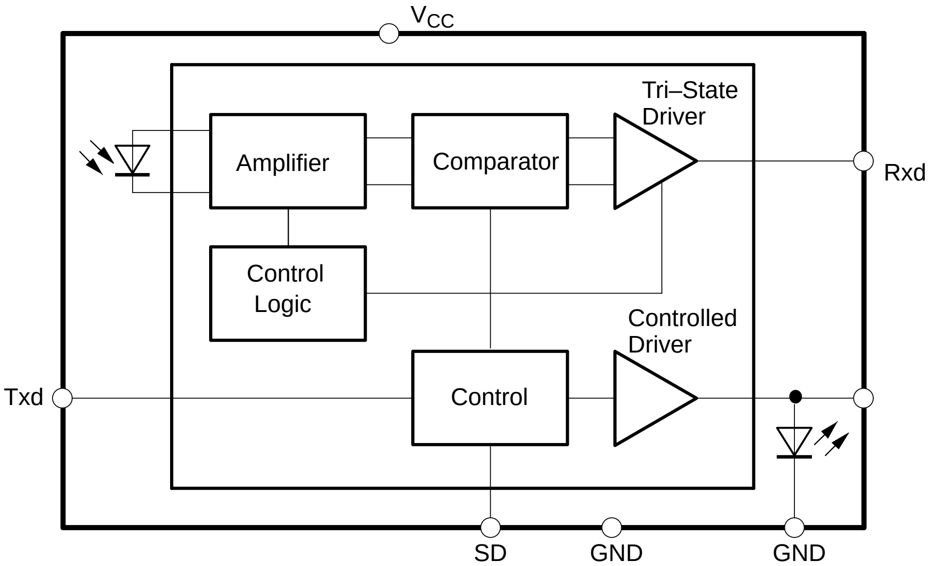


Figure 1. Functional Block Diagram

Pin Description

Pin	Symbol	Description	I/O	Active
1	V_{CC}	Supply Voltage		
2	IRED GND	IRED Cathode Ground, Ground		
3	IRED GND	IRED Cathode Ground, Ground		
4	Rxd	Output, Received Data, Tri-state, Floating in Shutdown Mode (V_{CC}/SD = Low)	O	LOW
5	Txd	Input Transmit Data	I	HIGH
6	SD	Shutdown	I	HIGH
7	GND	IRED Cathode Ground, Ground		
8	NC			

Absolute Maximum Ratings

Reference Point Pin 8, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply Voltage Range		V_{CC}	–0.5		6	V	
Input Current					10	mA	All Input Pins
Output Sink Current					25	mA	
Power Dissipation		P_{tot}			200	mW	See Figure 3
Junction Temperature		T_J			125	°C	
Ambient Temperature Range (Operating)		T_{amb}	–25		85	°C	
Storage Temperature Range		T_{stg}	–40		100	°C	
Soldering Temperature	t = 20 s @215°C			215	240	°C	See Vishay IrDA Design Guide
Average IRED Current*)		I_{IRED}(DC)			125	mA	
Repetitive Pulsed IRED*) Current		I_{IRED}(RP)			500	mA	<90 µs, t_{on}<20%
Transmitter Data Input Voltage		V_{Txd}	–0.5		V_{CC}+0.5	V	
Receiver Data Output Voltage		V_{Rxd}	–0.5		V_{CC}+0.5	V	
Virtual source size	Method: (1–1/e) encircled energy	d		2		mm	
Compatible to Class 1 operation of IEC 60825 or EN60825 with worst case IrDA SIR pulse pattern, 115.2 kbit/s							

*) Note: Maximum values of IRED. Cannot be reached due to implemented current source.

Electrical Characteristics

Tested for the following parameters (V_{CC} = 2.4 V to 3.6 V, 25°C, unless otherwise stated)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Remarks
Transceiver							
Supported Data Rates	Base band		9.6		115.2	kbit/s	
Supply Voltage Range		V_{CC}	2.4		3.6	V	Operational Down to 2.0 V
Supply Current	V_{CC} = 2.4 V to 5.5 V, E_e = 0	I_S		50	80	µA	Receive Mode, full Temperature Range
	V_{CC} = 2.4 V to 5.5 V, 10 klx Sunlight	I_S		70	90	µA	
	Shutdown Mode	$I_{Sshdown}$		10 5	100 10	nA nA	Entire Temperature Range Room Temperature 25°C
IRED Peak Current Transmitting	V_{CC} = 5.5 V V_{CC} = 2.4 V	I_{Str}		38 35	45 40	mA mA	SIR Transmit
Transceiver “Power On“ Settling Time					50	µs	Time from Switching on V_{CC} to Established Specified Operation

Optoelectronic Characteristics

Tested for the following parameters (V_{CC} = 2.4 V to 3.6 V, 25°C, unless otherwise stated)

Parameter	Test Conditions	Symbol	Min.	Typ	Max.	Unit	Remarks
Receiver							
Minimum Detection Threshold Irradiance	$\lvert\alpha\rvert \le \pm15°$ V_{CC} = 2.4 V to 5.5 V	$E_{e, min}$		25	40	mW/m^2	
Maximum Detection Threshold Irradiance	$\lvert\alpha\rvert \le \pm90°$ V_{CC} = 5 V	$E_{e, max}$	3300	5000		W/m^2	
	$\lvert\alpha\rvert \le \pm90°$ V_{CC} = 3 V	$E_{e, max}$	8000	15000		W/m^2	
Logic Low Receiver Input Irradiance		$E_{e,max,low}$			4	mW/m^2	
Output Voltage Rxd	Active	V_{OL}		0.5	0.8	V	C = 15 pF, R = 2.2 kΩ
	Non Active	V_{OH}	V_{CC}–0.5			V	C = 15 pF, R = 2.2 kΩ
Output Current Rxd V_{OL} < 0.8 V					4	mA	
Rise Time @Load: C = 15 pF, R = 2.2k		t_r	20		200	ns	
Fall Time @Load: C = 15 pF, R = 2.2k		t_f	20		200	ns	
Rxd Signal Electrical Output Pulse Width	2.4 kbit/s, Input Pulse Width 1.41 µs to 3/16 of bit Duration	t_p	1.4		20	µs	
Rxd Signal Electrical Output Pulse Width	115.2 kbit/s, Input Pulse Width 1.41 µs to 3/16 of bit Duration	t_p	1.4		4.5	µs	
Output Delay Time (Rxd), Leading Edge Optical Input to Electrical Output	Output Level = 0.5· V_{CC} @ 40 mW/m^2	t_{dl}		1	2	µs	
Jitter, Leading Edge of Output Signal	Over a Period of 10 bit, 115.2 kbit/s	t_j			300	ns	
Output Delay Time (Rxd), Trailing Edge Optical Input to Electrical Output	Output Level = 0.5· V_{CC} 40 mW/m^2	t_{dt}			6.5	µs	
Latency		t_L		100	200	µs	

Optoelectronic Characteristics (continued)

Tested for the following parameters (V_{CC} = 2.4 V to 3.6 V, 25°C, unless otherwise stated)

Parameter	Test Conditions	Symbol	Min.	Typ	Max.	Unit	Remarks
Transmitter							
Logic Low Transmitter Input Voltage		V_{IL}(Txd)	0		0.8	V	
Logic High Transmitter Input Voltage		V_{IH}(Txd)	2.4		V_{CC}	V	
Controlled Current	I_e = 4 mW/sr to 28 mW/sr in |α| ≤ ±15°	I_{F1}	25	30	35	mA	Voltage Range 2.4 V to 5.5 V
Output Radiant Intensity, |α| ≤ ±15°	I_{F1} = 25 mA to 35 mA	I_e	4	8	28	mW/sr	Current Controlled, 20% duty cycle.
Peak Emission Wavelength		λ_p	850		900	nm	
Spectral Emission Bandwidth				60		nm	
Optical Rise/Falltime	115.2 kHz Square Wave Signal (duty cycle 1:1)				200	ns	
Optical Output Pulse Duration	Input Pulse Duration 1.6 µs			1.6	2.2	µs	
Output Radiant Intensity	Logic Low Level				0.04	µW/sr	
Overshoot, Optical					25	%	
Rising Edge Peak to Peak Jitter	Over a Period of 10 bits, Independent of Information Content	t_j			0.2	µs	

Recommended SMD Pad Layout

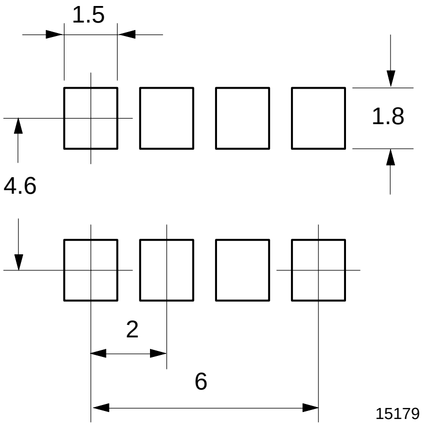


Figure 2. Pad Layout

Current Derating Diagram

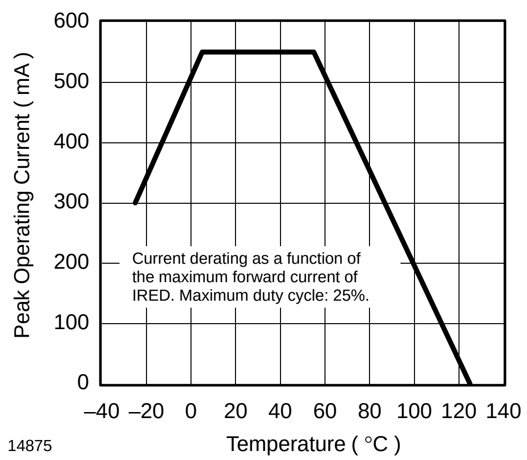
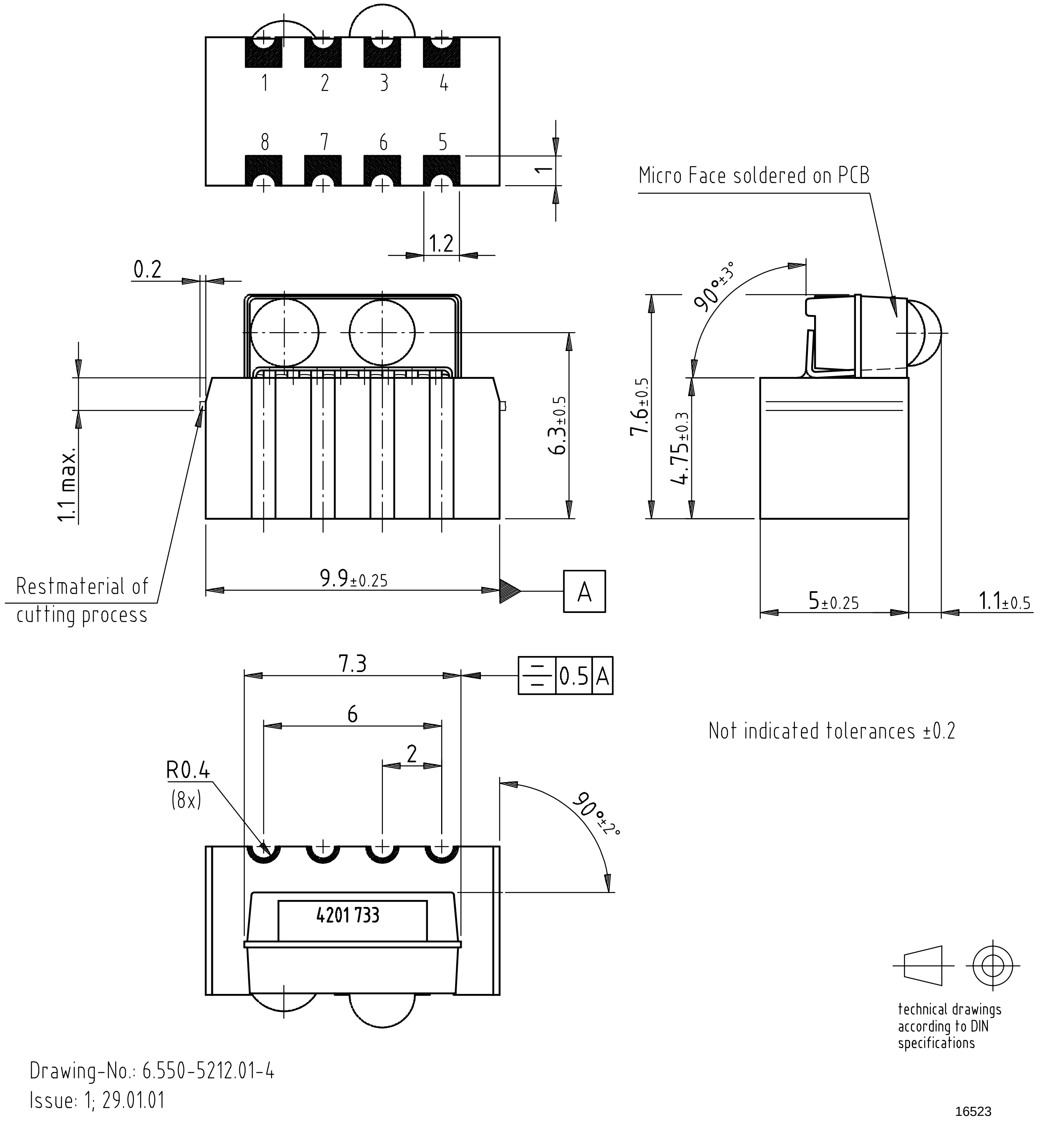
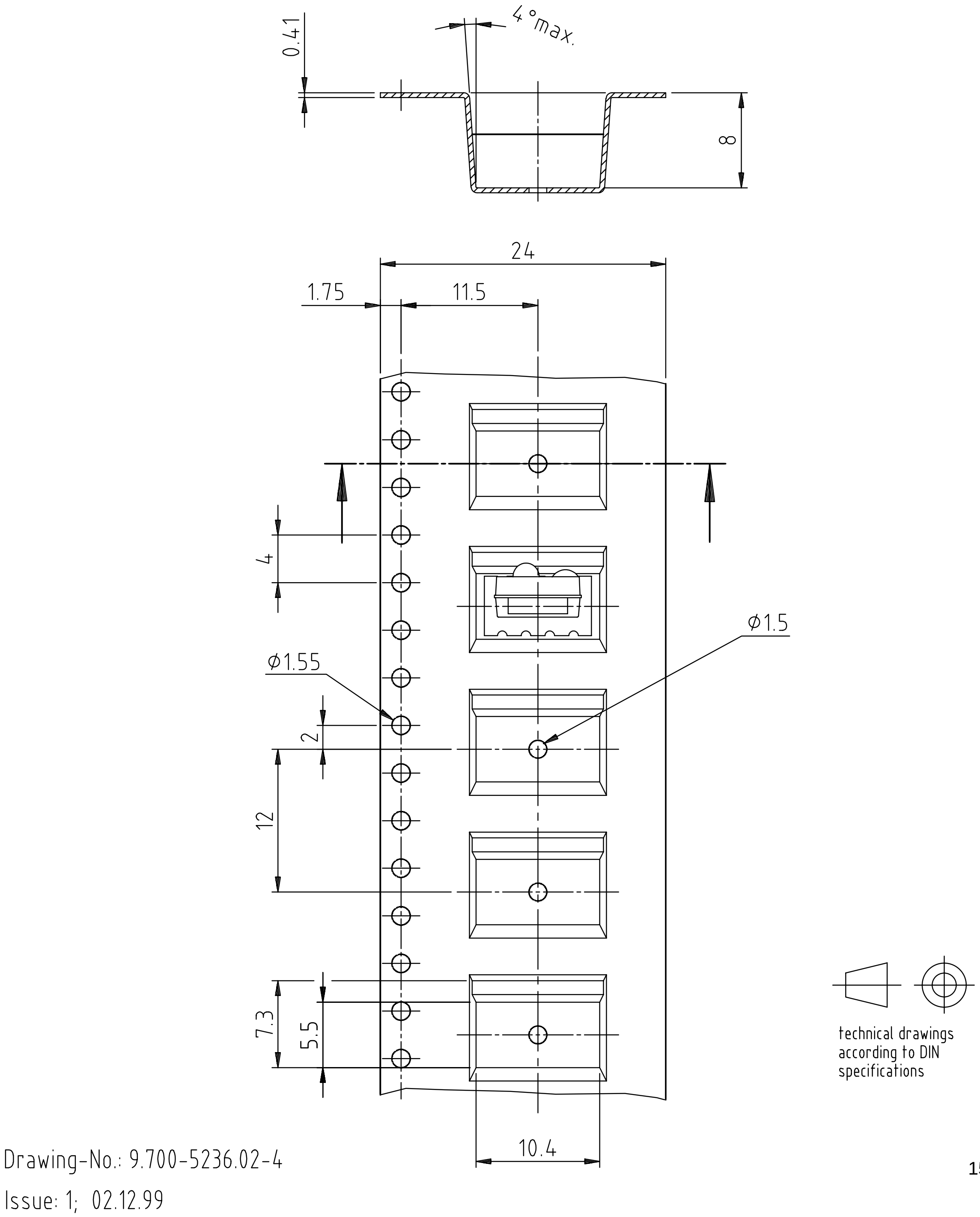


Figure 3. Shows the current derating of the emitter chip as a function of ambient temperature and duty cycle, see absolute maximum ratings. This is for information only. The TFDU4201 has an internal current control. Therefore, most of this curve is not relevant for this device because the higher currents are not intended to be used.

TFDU4201A–(Mechanical Dimensions)




0.41
4°max.
8
24
1.75
11.5
4
Ø1.5
Ø1.55
2
12
7.3
5.5
10.4
technical drawings
according to DIN
specifications
Drawing-No.: 9.700-5236.02-4
Issue: 1; 02.12.99

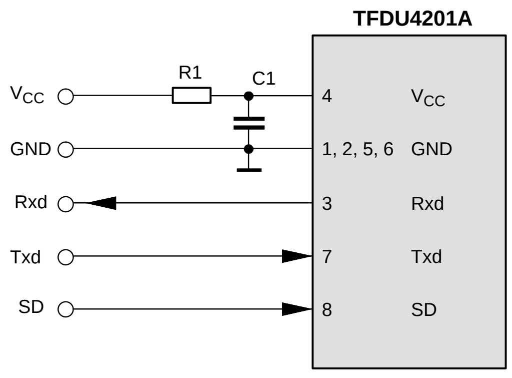
15181

Appendix

Application Hints

The TFDU4201 does not need any external components when operated at a “clean“ power supply. In a more noisy ambient it is recommended to add a capacitor and a resistor for noise suppression. A combination of a tantalum with a ceramics capacitor will be most efficient.

Recommended Circuit Diagram



Shut down

To shut down the TFDU4201 into a standby mode the SD pin has to be set active. For minimizing the shutdown current it is recommended to use a logic high level of >0.9 x V_{CC}

Latency

The receiver is in specified conditions after the defined latency. In a UART related application after that time (typically 50 µs) the receiver buffer of the UART must be cleared. Therefore the transceiver has to wait at least the specified latency after receiving the last bit before starting the transmission to be sure that the corresponding receiver is in a defined state.

Table 1. Recommended Application Circuit Components *)

Component	Recommended Value	Vishay Part Number
C1	4.7 µF	293D 475X9 016B 2T
R1	5 Ω max	

*) This is a recommendation for a combination to start with to exclude power supply effects. Optimum, from a costs point of view, to work without both.

Revision History:

A1.2, 07/04/1999: New edition

A1.2, 08/07/1999: Correction of typos: 2.4 V instead of 2.7 V in the full context, and missing measurement conditions added.

A1.3, 13/10/2000: First public release

A1.4, 29/01/2001: Typos corrected, storage temperature increased, IRED peak current increased, minimum detection threshold improved, latency increased, output radiation intensity, improved.

Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

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The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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