January 1994
Edition 2.0

FUJITSU

DATA SHEET

MB85285A-60/-70/-80

CMOS 4M x 9 Fast Page Mode DRAM Module

CMOS 4,194,304 x 9 Bit Fast Page Mode DRAM Module

The Fujitsu MB85285A is a fully decoded CMOS Dinamic Random Access Memory (DRAM) Module consisting of nine MB814100A devices.

The MB85285A organized as 4,194,304 x 9–bit words is optimized for those applications requiring high speed, high performance, large memory storage, and high density memory organizations.

The operation and electrical characteristics of the MB85285A are the same as the MB814100A devices which feature Fast Page operation. For ease of memory expansion, the MB85285A is offered in a 30–pad Single In–line Memory Module (SIMM).

See page 8

MSS–30P–P03

See page 9

MSP–30P–P04

PRODUCT LINE & FEATURES

Parameter	MB85285A–60	MB85285A–70	MB85285A–80
$\overline{RAS}$ Access Time	60ns max.	70ns max.	80ns max.
Random Cycle Time	110ns max.	125ns max.	140ns max.
Address Access Time	30ns max.	35ns max.	40ns max.
$\overline{CAS}$ Access Time	15ns max.	20ns max.	20ns max.
Fast Page Mode Cycle Time	40ns max.	45ns max.	45ns max.
Power Dissipation • Operating mode	5445mW max.	4950mW max.	4455mW max.
• Standby mode	99mW max.(TTL level) / 49.5mW max.(CMOS level)		

- Organization:
  4,194,304 words x 9 bits
- Memory:
  MB814100A, 9 pcs
- Decoupling Capacitor:
  0.22 µF, 9 pcs
- Package and Ordering Information:
  30–pad SIMM, order as
  MB85285A–xxPJPB
  (PJPB = Solder pad)
  30–pad SIP, order as
  MB85285A–xxPJPS

PIN ASSIGNMENT
(TOP VIEW)

$\overline{VCC}$	1
$\overline{CAS}$	2
DQ0	3
A0	4
A1	5
DQ1	6
A2	7
A3	8
VSS	9
DQ2	10
A4	11
A5	12
DQ3	13
A6	14
A7	15
DQ4	16
A8	17
A9	18
A10	19
DQ5	20
$\overline{WE}$	21
VSS	22
DQ6	23
NC	24
DQ7	25
Q8	26
$\overline{RAS}$	27
$\overline{CAS}$8	28
D8	29
VCC	30

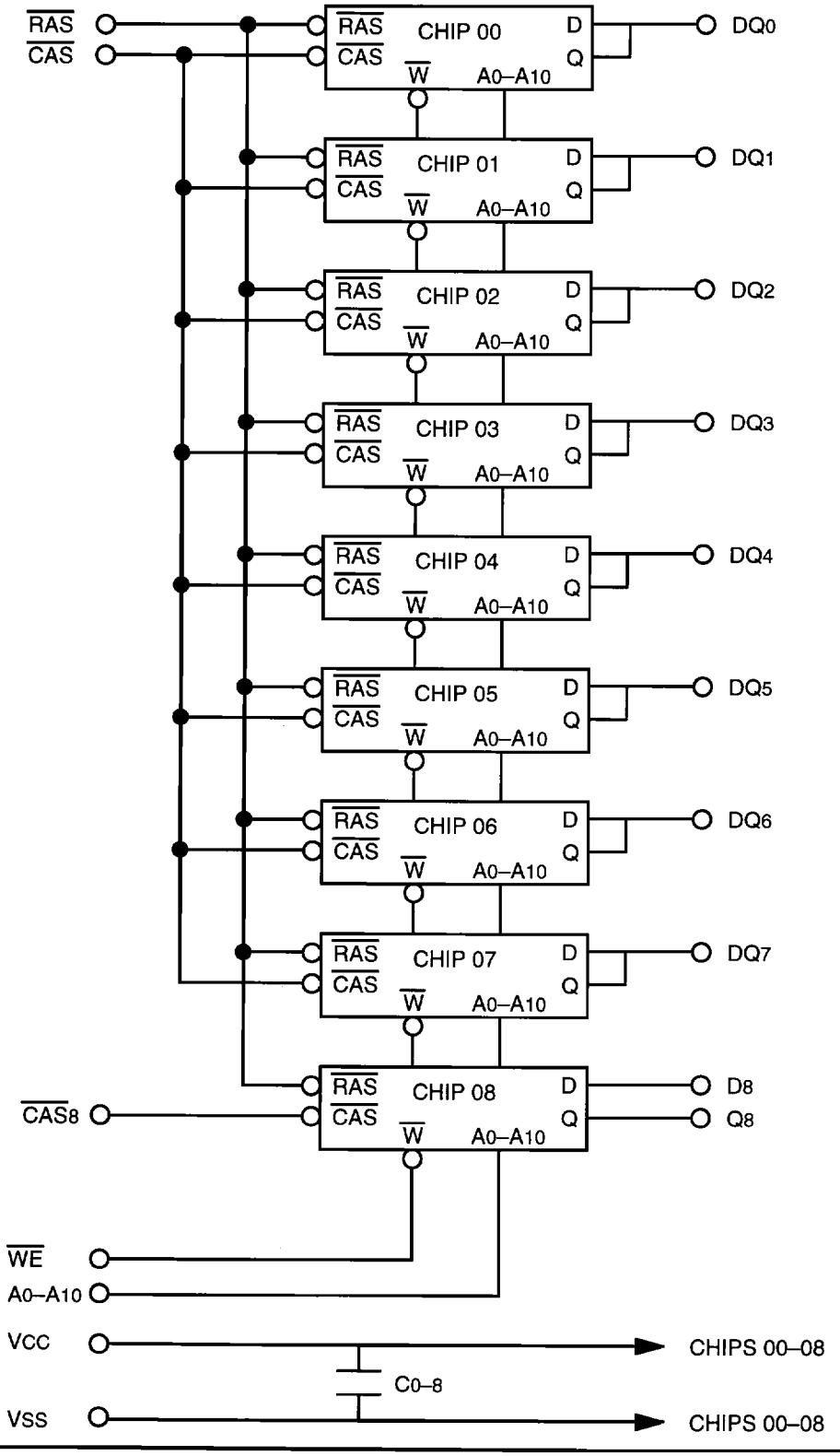
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Supply Voltage	VCC	–1.0 to +7.0	V
Input Voltage	VIN	–1.0 to +7.0	V
Output Voltage	VOUT	–1.0 to +7.0	V
Short Circuit Output Current	IOUT	±50	mA
Power Dissipation	PD	9.0	W
Storage Temperature	TSTG	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A11	CIN1	—	53	pF
Input Capacitance, $\overline{RAS}$	CIN2	—	42	pF
Input Capacitance, $\overline{CAS}$	CIN3	—	39	pF
Input Capacitance, $\overline{CAS}$8	CIN4	—	6	pF
Input Capacitance, $\overline{WE}$	CIN5	—	44	pF
Input Capacitance, D8	CIN6	—	6	pF
I/O Capacitance, DQ0 to DQ7	CDQ	—	11	pF
Output Capacitance, Q8	COUT	—	8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced VSS)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
	VSS	0	0	0	V
Input High Voltage, all inputs	VIH	2.4	—	6.5	V
Input Low Voltage, all inputs	VIL1	–2.0	—	0.8	V
all DQs	VIL2	–1.0 *1	—	0.8	V
Operating Temperature	TA	0	25	70 *2	°C

Note: *1 The device will withstand undershoots to the –2.0V level with a maximum pulse width of 20ns.
*2 Maximum ambient temperature is permissible under certain conditions. See Fig. 2&3.

Fig. 2 – DERATING CURVE (Normal Cycle)

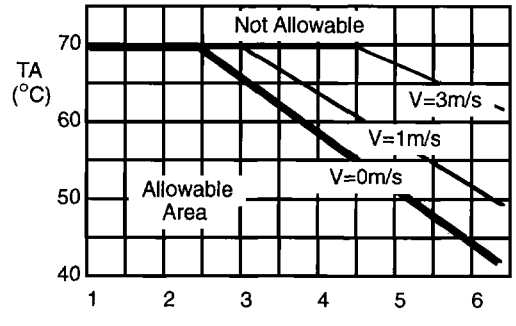
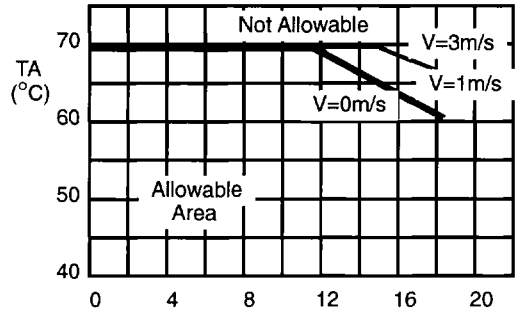


Fig. 3 – DERATING CURVE (Fast Page Cycle)



Return to the DRAM Menu

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Paramter		Notes	Symbol	Conditions	Values			Unit
					Min	Typ	Max	
Output High Voltage		1	VOH	IOH = –5 mA	2.4	—	—	V
Output Low Voltage		1	VOL	IOL = 4.2 mA	—	—	0.4	
Input Leakage Current			IIL	0 V ≤ VIN ≤ 5.5V; 4.5 V ≤ VCC ≤ 5.5 V VSS = 0 V; All other pins not under test = 0 V	–30	—	30	µA
Output Leakage Current			IOL	0 V ≤ VOUT ≤ 5.5 V; Data out disabled	–10	—	10	µA
Operating Current (Average Power Supply Current)	MB85285A-60	2	ICC1	$\overline{RAS}$ & $\overline{CAS}$ cycling; tRC = min	—	—	990	mA
	MB85285A-70						900	
	MB85285A-80						810	
Standby Current (Power Supply Current)	TTL level		ICC2	$\overline{RAS}$ = $\overline{CAS}$ = VIH	—	—	18	mA
	CMOS level			$\overline{RAS}$ = $\overline{CAS}$ ≥ VCC–0.2V			9	
Refresh Current #1 (Average Power Supply Current)	MB85285A-60	2	ICC3	$\overline{CAS}$ = VIH, $\overline{RAS}$ cycling; tRC = min	—	—	990	mA
	MB85285A-70						900	
	MB85285A-80						810	
Fast Page Mode Current	MB85285A-60	2	ICC4	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; tPC = min	—	—	495	mA
	MB85285A-70						450	
	MB85285A-80						405	
Refresh Current #2 (Average Power Supply Current)	MB85285A-60	2	ICC5	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; tRC = min	—	—	810	mA
	MB85285A-70						720	
	MB85285A-80						630	

Notes:

1. Referenced to VSS.
2. ICC depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   ICC depends on the number of address change as $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   ICC1, ICC3 and ICC5 are specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   ICC4 is specified at one time of address change during one Page cycle.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Notes	Symbol	MB85285A-60		MB85285A-70		MB85285A-80		Unit
			Min	Max	Min	Max	Min	Max	
Time Between Refresh		tREF	—	16.4	—	16.4	—	16.4	ms
Random Read/Write Cycle Time		tRC	110	—	125	—	140	—	ns
Read–Modify–Write Cycle Time		tRWC	130	—	150	—	165	—	ns
Access Time from $\overline{RAS}$	4,7	tRAC	—	60	—	70	—	80	ns
Access Time from $\overline{CAS}$	5,7	tCAC	—	15	—	20	—	20	ns
Column Address Access Time	6,7	tAA	—	30	—	35	—	40	ns
Output Hold Time		tOH	0	—	0	—	0	—	ns
Output Buffer Turn On Delay Time		tON	0	—	0	—	0	—	ns
Output Buffer Turn Off Delay Time	8	tOFF	—	15	—	15	—	20	ns
Transition Time		tT	2	50	2	50	2	50	ns
$\overline{RAS}$ Precharge Time		tRP	40	—	45	—	50	—	ns
$\overline{RAS}$ Pulse Width		tRAS	60	100000	70	100000	80	100000	ns
$\overline{RAS}$ Hold Time		tRSH	15	—	20	—	20	—	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		tCRP	5	—	5	—	5	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	9,10	tRCD	20	45	20	50	20	60	ns
$\overline{CAS}$ Pulse Width		tCAS	15	—	20	—	20	—	ns
$\overline{CAS}$ Hold Time		tCSH	60	—	70	—	80	—	ns
$\overline{CAS}$ Precharge Time (Normal)	15	tCPN	10	—	10	—	10	—	ns
Row Address Set Up Time		tASR	0	—	0	—	0	—	ns
Row Address Hold Time		tRAH	10	—	10	—	10	—	ns
Column Address Set Up Time		tASC	0	—	0	—	0	—	ns
Column Address Hold Time		tCAH	12	—	12	—	15	—	ns
$\overline{RAS}$ to Column Address Delay Time	11	tRAD	15	30	15	35	15	40	ns
Column Address to $\overline{RAS}$ Lead Time		tRAL	30	—	35	—	40	—	ns
Column Address to $\overline{CAS}$ Lead Time		tCAL	30	—	35	—	40	—	ns
Read Command Set Up Time		tRCS	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	12	tRRH	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{CAS}$	12	tRCH	0	—	0	—	0	—	ns
Write Command Set Up Time	13	tWCS	0	—	0	—	0	—	ns
Write Command Hold Time		tWCH	10	—	10	—	12	—	ns
$\overline{WE}$ Pulse Width		tWP	10	—	10	—	12	—	ns

Return to the DRAM Menu

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB85285–80		MB85285–10		MB85285–12		Unit
			Min	Max	Min	Max	Min	Max	
Write Command to $\overline{RAS}$ Lead Time		tRWL	15	—	20	—	20	—	ns
Write Command to $\overline{CAS}$ Lead Time		tCWL	15	—	18	—	20	—	ns
DIN Set Up Time		tDS	0	—	0	—	0	—	ns
DIN Hold Time		tDH	10	—	10	—	12	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay Time	13	tRWD	60	—	70	—	80	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time	13	tCWD	15	—	20	—	20	—	ns
Column Address to $\overline{WE}$ Delay Time	13	tAWD	30	—	35	—	40	—	ns
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		tRPC	0	—	0	—	0	—	ns
$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before–$\overline{RAS}$ Refresh		tCSR	0	—	0	—	0	—	ns
$\overline{CAS}$ Hold Time for $\overline{CAS}$–before–$\overline{RAS}$ Refresh		tCHR	10	—	10	—	12	—	ns
$\overline{WE}$ Set Up Time from $\overline{RAS}$	16	tWSR	0	—	0	—	0	—	ns
$\overline{WE}$ Hold Time from $\overline{RAS}$	16	tWHR	10	—	10	—	10	—	ns
Fast Page Mode RAS Pulse Width		tRASP	—	200000	—	200000	—	200000	ns
Fast Page Mode Read/Write Cycle Time		tPC	40	—	45	—	45	—	ns
Fast Page Mode Read–Modify–Write Cycle Time		tPRWC	60	—	68	—	70	—	ns
Access Time from $\overline{CAS}$ Precharge	7,14	tCPA	—	35	—	40	—	40	ns
Fast Page Mode $\overline{CAS}$ Precharge Time		tCP	10	—	10	—	10	—	ns
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time		tCPWD	35	—	40	—	40	—	ns
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		tRHCP	35	—	40	—	40	—	ns

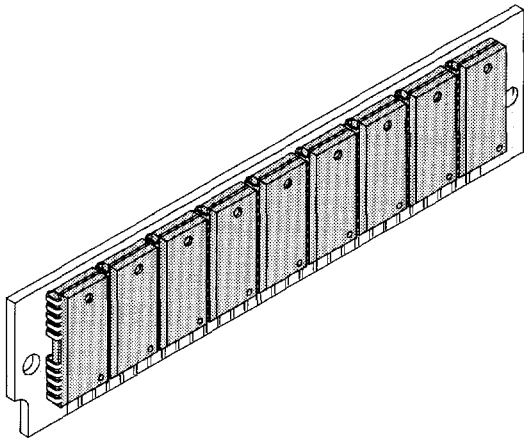
Notes:

1. An Initial pause ($\overline{RAS}$=$\overline{CAS}$=VIH) of 200µs is required after power–up followed by any eight $\overline{RAS}$–only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$–before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5ns.
3. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also transition times are measured between VIH (min) and VIL (max).
4. Assumes that tRCD ≤ tRCD (max), tRAD ≤ tRAD (max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will be increased by the amount that tRCD exceeds the value shown.
5. If tRCD ≥ tRCD (max), tRAD ≥ tRAD (max), and tASC ≥ tAA – tCAC – tT, access time is tCAC.
6. If tRAD ≥ tRAD (max) and tASC ≤ tAA – tCAC – tT, access time is tAA.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. tOFF is specified that output buffer change to high impedance state.
9. Operation within the tRCD (max) limit ensures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, access time is controlled exclusively by tCAC or tAA.
10. tRCD (min) = tRAH (min) + 2tT + tASC (min).
11. Operation within the tRAD (max) limit ensures that tRAC (max) can be met. tRAD (max) is specified as a reference point only; if tRAD is greater than the specified tRAD (max) limit, access time is controlled exclusively by tCAC or tAA.
12. Either tRRH or tRCH must be satisfied for a read cycle.
13. tWCS, tCWD, tRWD and tAWD are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If tWCS ≥ tWCS (min), the cycle is an early write cycle and DOUT pin will maintain high impedance state thoughout the entire cycle. If tCWD ≥ tCWD (min), tRWD ≥ tRWD (min) and tAWD ≥ tAWD (min), the cycle is a read–modify–write cycle and data from the selected cell will appear at the DOUT pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the DOUT pin, and write operation can be exected by satisfying tRWL, tCWL, tCAL and tRAL specifications.
14. tCPA is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if tCP is long, tCPA is longer than tCPA (max).
15. Assumes that $\overline{CAS}$–before–$\overline{RAS}$refresh.
16. Assumes that Test mode function.

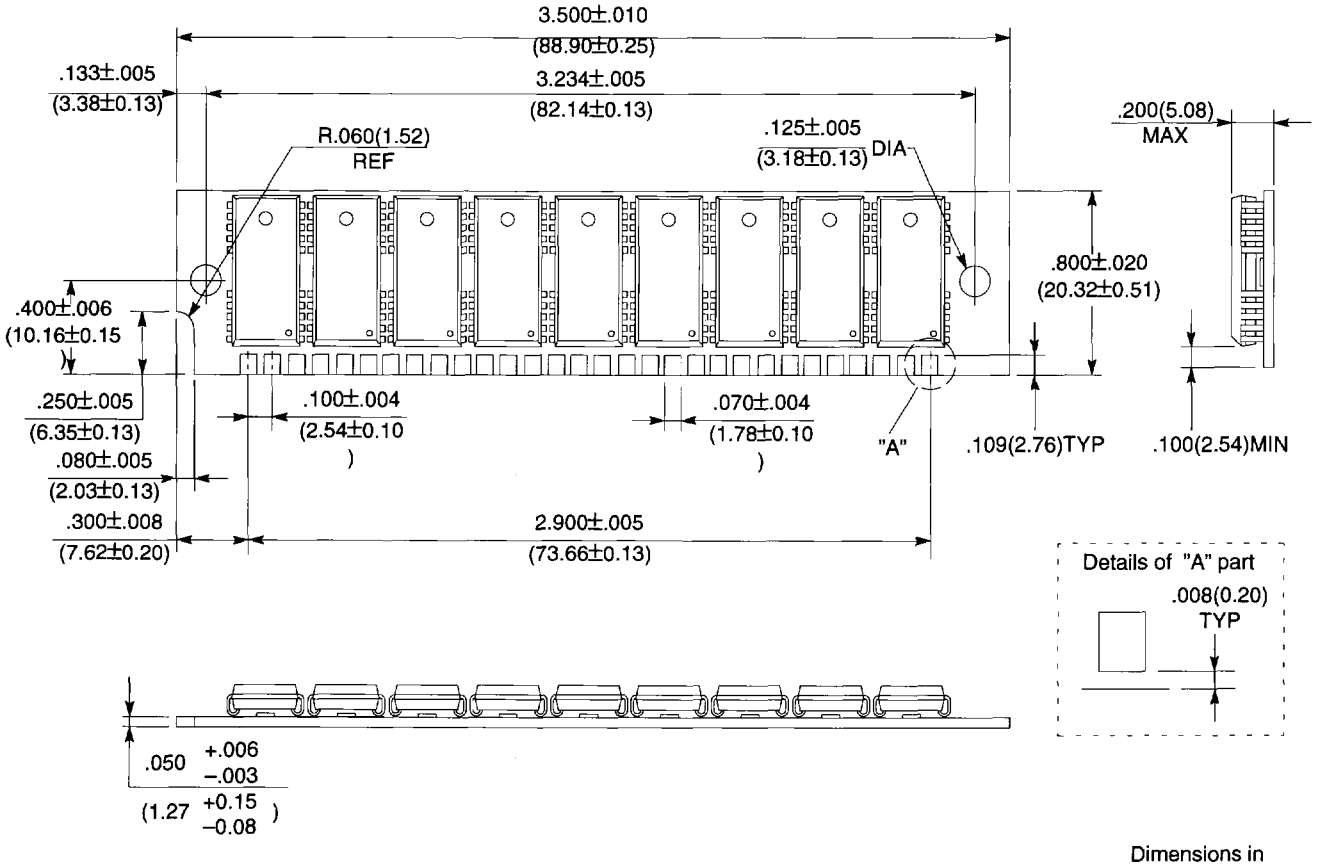
Return to the DRAM Menu

PACKAGE DIMENSIONS

(Suffix : PJPB)



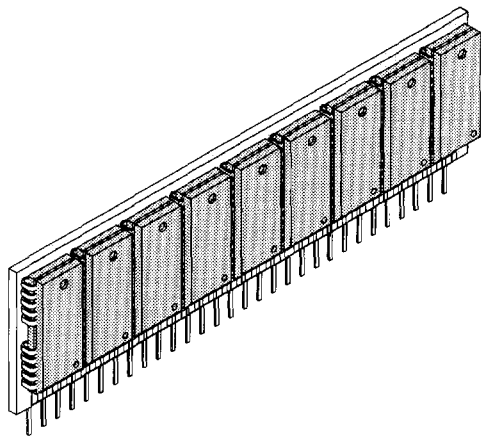
30-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-30P-P03)



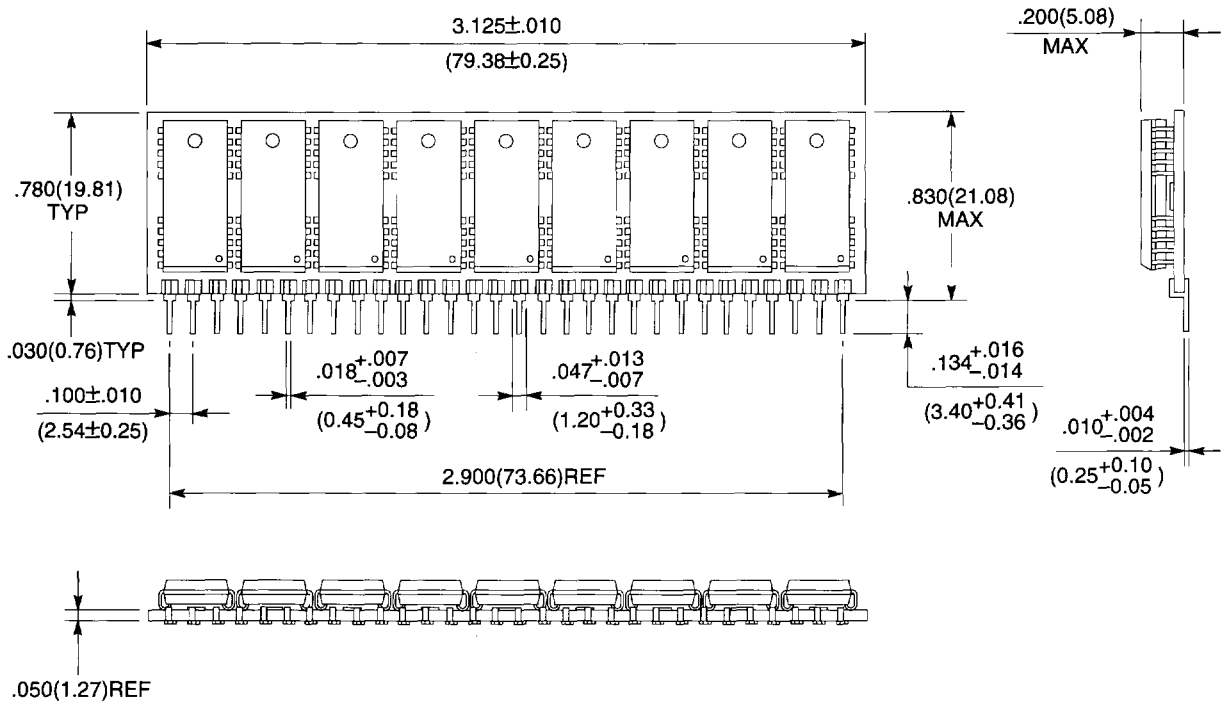
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : PJPS)



30-LEAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSP-30P-P04)



Dimensions in
inches (millimeters)

Return to the DRAM Menu

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete Information sufficient for construction purposes is not necessarily given.

The information contained in this document has been carefully checked and is believed to be reliable. However, Fujitsu assumes no responsibility for inaccuracies.

The Information contained in this document does not convey any license under the copyrights, patent rights or trademarks claimed and owned by Fujitsu.

Fujitsu reserves the right to change products or specifications without notice.

Return to the DRAM Menu

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Electronic Devices International
Sales and Engineering Support Division
1015,Kamikodanaka Nakahara–ku,
Kawasaki 211, Japan
Tel: (044)754–3753
FAX: (044)754–3332

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3455 North First Street
San Jose, CA 95134–1804, USA.
Tel: 408 –922–9000
FAX: 408–432–9044

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6–10,
63303 Dreieich-Buchschlag,
Germany
Tel: (06103) 690–0,
Telex: 411963 fmg d
FAX: (06103) 690–122

Asia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
#06–04 to #06–07
Plaza By The Park
No.51 Bras Basah Road
Singapore 0719
Tel: 336–1600
Telex: 55573
FAX: 336–1609

Printed in Japan JV0012–941J2