To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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M62301SP/FP

10 to 12-bit 4-ch Integrating A/D Converter

REJ03D0861-0300
Rev.3.00
Mar 25, 2008

Description

M62301 semiconductor integrated circuit forms an integrating A/D converter, being connected to a microcomputer unit. By using selection signals and counter clock signals from the unit, a 10 to 12-bit A/D converter can be created at a low cost.
The integration time and resolution can be set at the users option by changing external parameters. In addition, the built-in circuit offset, delay time and temperature fluctuation are adjustable, enabling a wide range of applications. M62301 has a 3 input decoder circuit, high-precision reference voltage (1.22 V) generator, current supply and comparator for integration, and voltage-monitoring reset circuit for a 5 V power supply. It is also equipped with girdling to prevent current leak from integration capacitor.

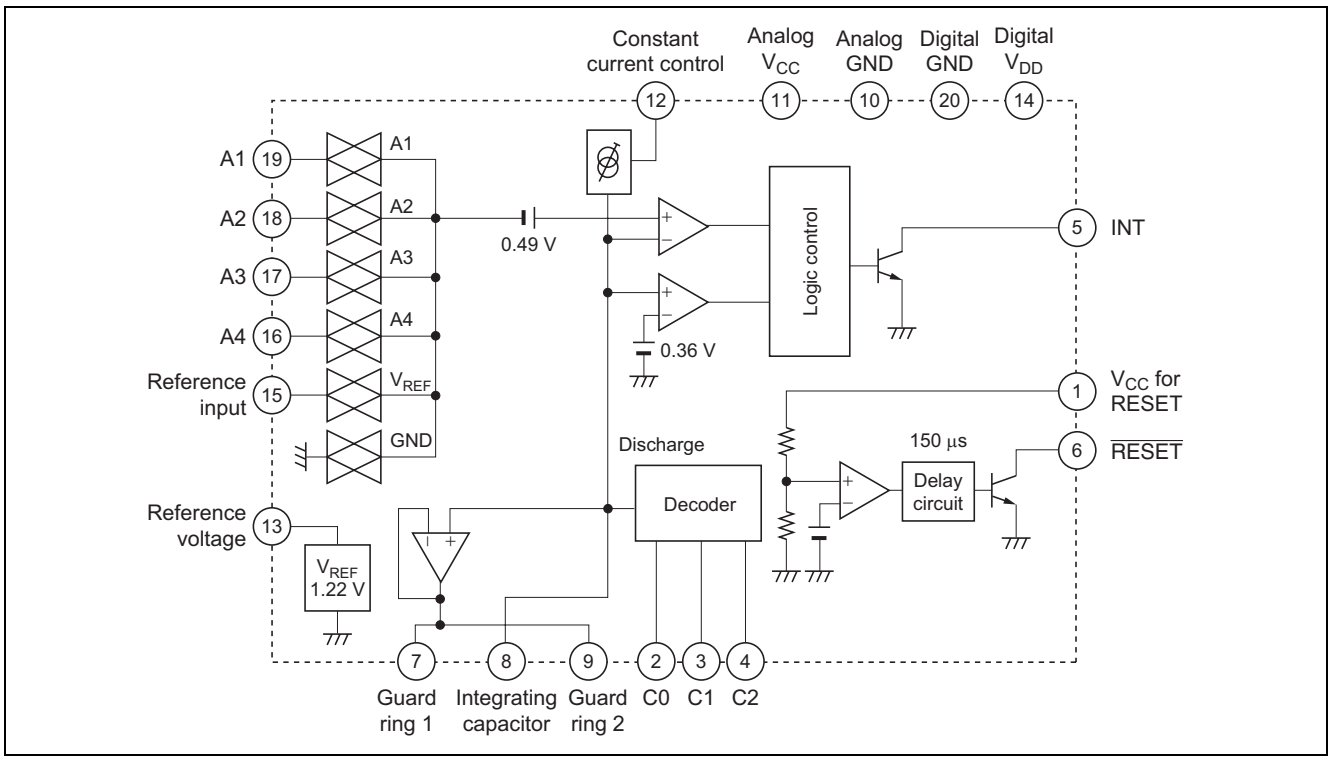
Features

- Separate power supplies for analog section and digital section.
- Low power dissipation: 2 mA (Typ)
  (1 mA for A/D conversion and the other 1 mA for reset)
- Linear error: ±0.02% (Typ)
- Conversion time: 526 µs/ch (Typ)
- Built-in system reset: 4.45 V (Typ)

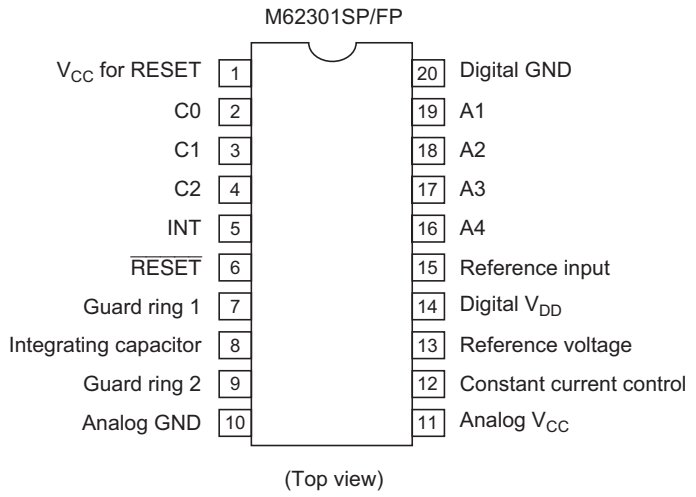
Application

High-precision control systems such as temperature control and speed control

Block Diagram



Pin Arrangement



Outline: PRDP0020BA-A (20P4B)
PRSP0020DA-A (20P2N-A)

Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit
Analog section supply voltage	V_{CC}	15	V
Digital section supply voltage	V_{DD}	8	V
Digital input voltage	V_{ID}	–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{IA}	–0.3 to V_{DD} + 0.3	V
INT output current	I_{OINT}	6	mA
Reset output current	I_{ORE}	6	mA
INT output withstand voltage	V_{INT}	15	V
Reset output withstand voltage	V_{RESET}	15	V
Reset supply voltage	V_{RE}	6	V
Power dissipation	Pd	990 (P) / 660 (FP)	mW
Thermal derating	Kθ	9.9 (P) / 6.6 (FP)	mW/°C
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–40 to +125	°C

Recommended Operating Conditions

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Analog section supply voltage	V_{CC}	4.5	8.0	12.0	V
Digital section supply voltage	V_{DD}	4.5	5.0	5.5	V
Analog input voltage range (I_I = 50 μA)	V_{IA}	0	—	No more than (V_{CC} – 2.5 V) and V_{DD}*1	V
Reference input voltage (I_I = 50 μA)	V_{IR}	1	—	No more than (V_{CC} – 2.5 V) and V_{DD}*1	V
Integration capacity	C_I	300	—	22000	pF
Resistance to determine charge current	R_I	6	—	60	kΩ
Output current	I_O	—	—	4	mA

Note: 1. Maximum analog input voltage is less than the difference between V_{CC} – 2.5 V as well as V_{DD}.

$$\text{Charging current} \quad I_I = \frac{V_{REF}}{R1}$$

Electrical Characteristics

(V_{CC} = 5.0 V, V_{DD} = 5.0 V, Ta = 25°C, unless otherwise noted)

	Item	Symbol	Limits			Unit	Test Conditions
			Min	Typ	Max		
A/D Converter	Supply current	I_{CC}	—	1.0	2.0	mA	
	Analog input voltage range	V_{IA}	0	—	2.5	V	I_I = 100 μA
					2.2		I_I = 200 μA
	Reference input voltage	V_{REF}	1.17	1.22	1.27	V	I_{REF} = ±5 μA C_{REF} = 4700 pF
	Permissible current inflow at reference voltage	I_{REF+}	—	—	50	μA	
		I_{REF-}			–10		
	Conversion error	E_C	—	0.05	0.1	%/FSR	R_I = 24 kΩ*1
	Linear error	E_L	—	0.02	0.09	%/FSR	R_I = 24 kΩ*2
	Conversion time	T_T	—	526	—	μs	V_{IA} = 2.5 V, C_I = 0.01 μF R_I = 24 kΩ
	Discharge time	Tdi	—	3	17	μs	$V_{(8)}$ = 3 V → 0.3 V C_I = 4700 pF
	Analog input current	I_B	—	–0.35	–3.5	μA	
	Digital input "H" level	V_{IH}	3.5	—	—	V	
	Digital input "L" level	V_{IL}	—	—	0.8	V	
	INT output "L" level	V_{LINT}	—	0.1	0.4	V	I_{OL} = 1 mA
	INT output leak current	I_{OHINT}	—	—	1	μA	$V_{(5)}$ = 15 V
Reset Section	Detection voltage	V_{DET}	4.30	4.45	4.60	V	
	Hysteresis voltage	ΔV_{DET}	30	50	80	mV	
	Delay time	T_{DE}	75	150	300	μs	
	Reset output "L" level	V_{LRE}	—	0.1	0.4	V	I_{OL} = 1 mA
	Reset output leak current	I_{OHRE}	—	—	1	μA	$V_{(6)}$ = 15 V
	Supply current	I_{RE}	—	1.0	2.0	mA	V_{RE} = 5 V
	Limit operating voltage	V_{OPL}	—	0.75	1.0	V	R_L = 2.2 kΩ, $V_{L\overline{RE}} \leq$ 0.4 V
			—	0.6	0.8		R_L = 100 kΩ, $V_{L\overline{RE}} \leq$ 0.4 V

Notes: 1. Conversion error; Deviation from the line that links the "0" scale point (mode 0) and reference scale point (mode 3. V_{FSR} = 2.5 V). Associated with all channels.

2. Linear error; Deviation from the line that links the 0 V input point and 2.5 V input point on a given channel.

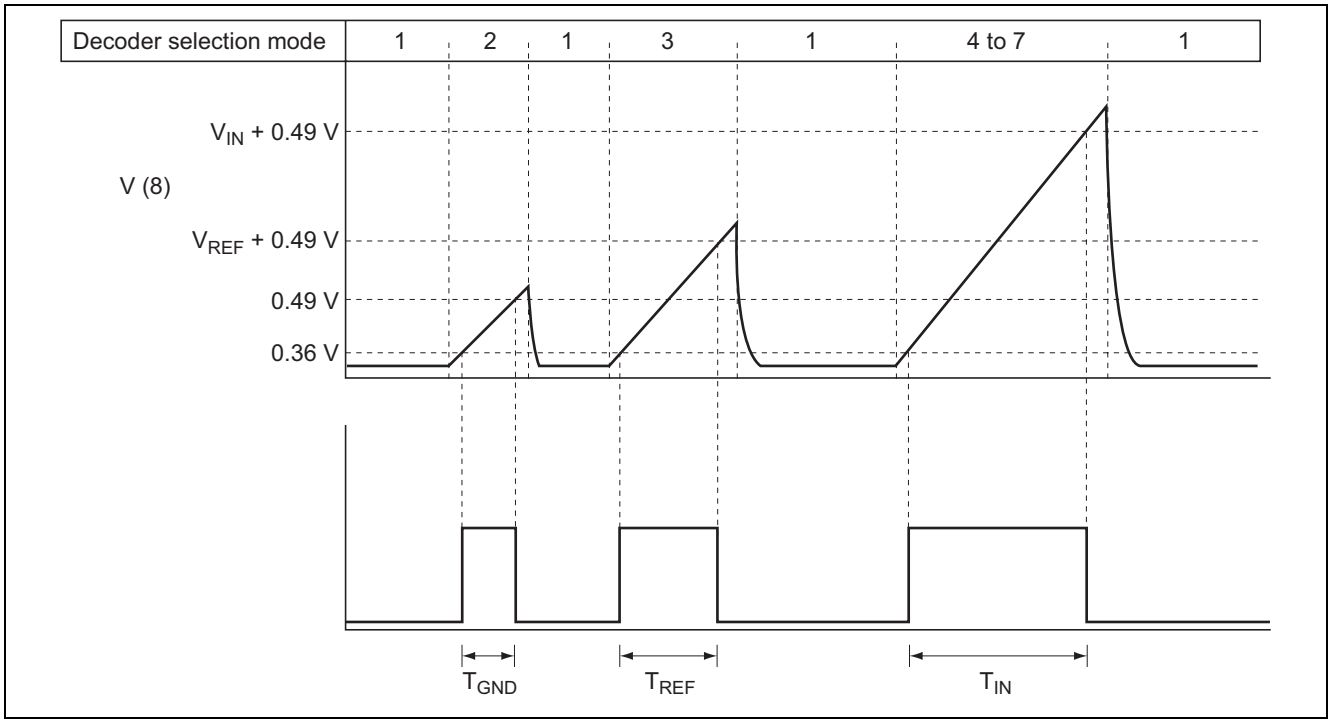
Operating Description

(1) Decoder

Based on digital inputs to C0, C1, C2, the analog switch is set to on, and the input of "0" scale (GND input), input of reference scale (reference voltage input), input to A1-A4, or discharge from integration capacitor (C_I) is performed. None of these operations is performed when the "mode 8" input is given:

Mode	1	2	3	4	5	6	7	8
C0	0	1	0	1	0	1	0	1
C1	0	0	1	1	0	0	1	1
C2	0	0	0	0	1	1	1	1
	Discharge	GND	V_{REF}	A1	A2	A3	A4	—

(2) A/D conversion



Multiplexer first selects V_{GND}, obtaining minimum pulse T_{GND}. It then selects V_{REF}, obtaining reference pulse T_{REF}. Input is selected next, obtaining input pulse T_{IN}. V_{IN} is obtained by deducting T_{GND}, as the offset, from T_{REF} and T_{IN}.

$$V_{IN} = V_{REF} \bullet \frac{T_{IN} - T_G}{T_{REF} - T_G}$$

By measuring voltage at the maximum input for approximately 500 µs under the counter clock of 8 MHz, resolution of approximately 12 bits can be obtained;

$$\frac{500\ \mu s}{125\ ns} \approx 2^{12}$$

Note: To ensure discharge from capacitor C_I, the decoder input as in the above diagram should stay in mode 1 at least for the period calculated above: $Tdi = (C_I \times \frac{V_{IAmax} + 0.49}{1\ mA})$

It is not necessary to measure T_{GND}, and T_{REF} for each channel.

(3) Constant current control

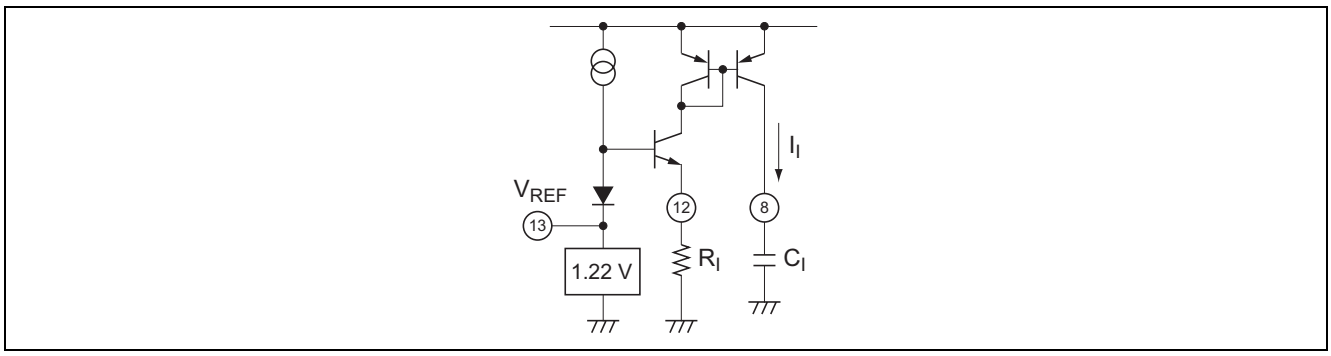
Integrating current I_I can be obtained based on the reference voltage (1.22 V) by the built-in high-precision generator and resistance R_I.

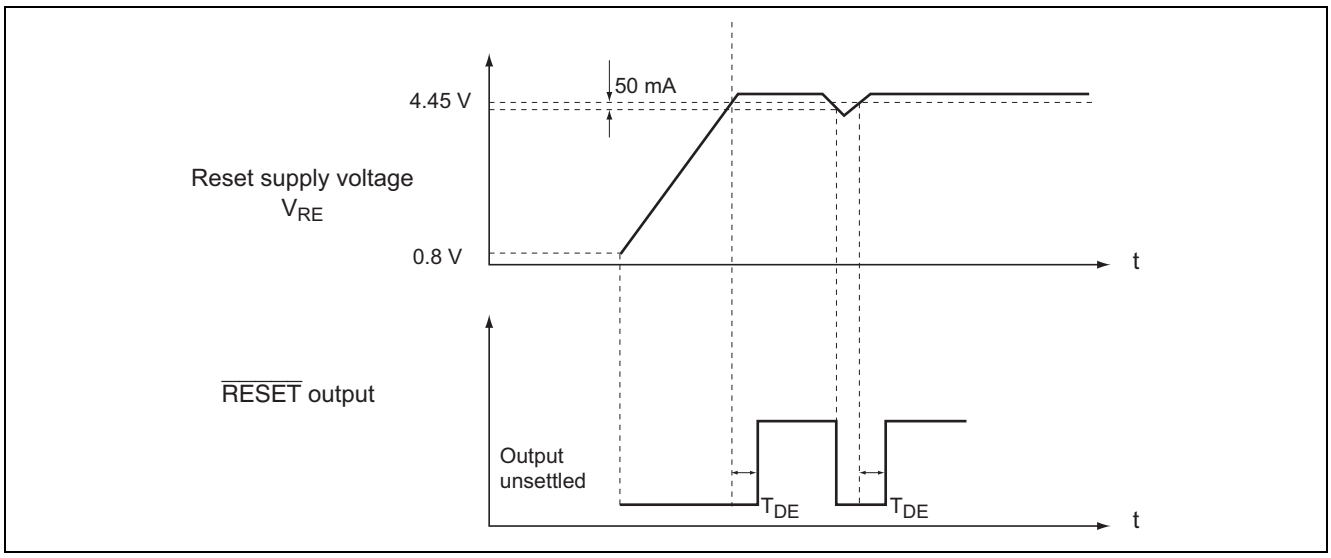
$$I_I = \frac{1.22}{R_I} \quad (A) \quad \text{..... (1)}$$

Integration time T_I can be calculated as follows;

$$T_I = (V_{IN} + 0.49)\frac{C_I}{I_I} \quad \text{..... (2)}$$

However, parameters such as built-in comparator offset voltage, analog switch offset, voltage leak current and delay time are not counted.

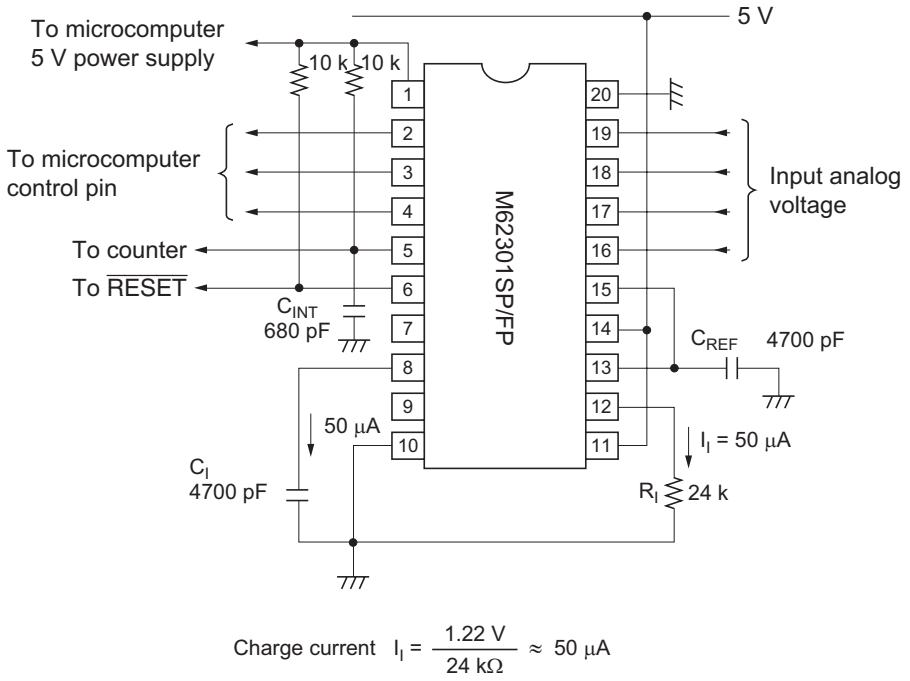




When voltage applied to pin V_{RE} becomes less than 4.45 V, the $\overline{\text{RESET}}$ output status becomes "L". If voltage increases over 4.50 V, the $\overline{\text{RESET}}$ status becomes "H" within 150 μs.

Application Suggestion

1. 4-channel 11-bit A/D converter system



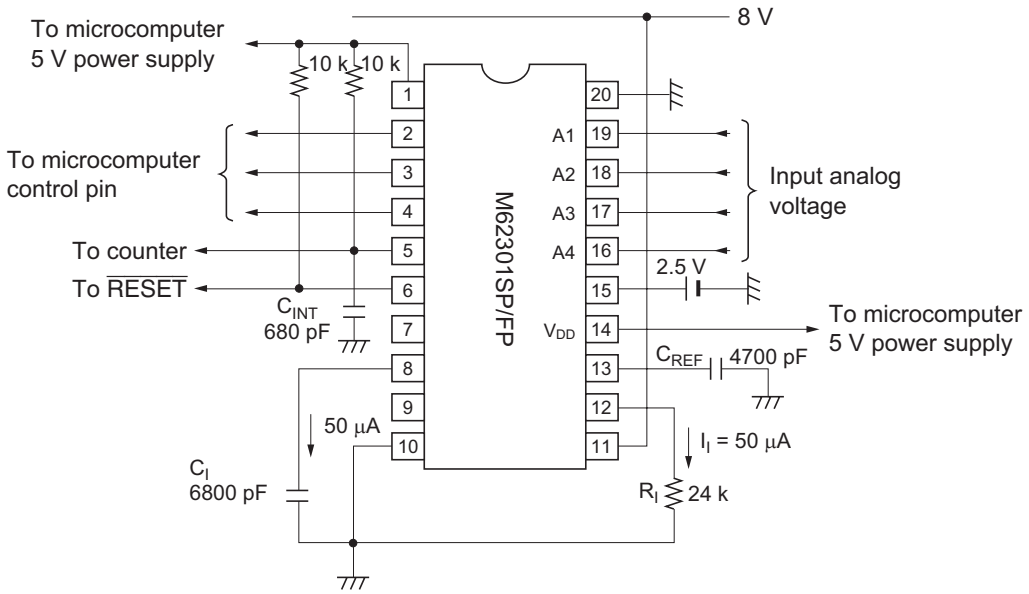
Note: C_{REF}: To stabilize reference voltage, be sure to connect capacitance of approximately 4700 pF.
C_{INT}: We suggest that this capacitance be connected to prevent malfunction due to noise.
Use C_I that leaks as slight current as possible. To prevent leak to the circuit board, we recommend providing guard ring (7), (9).

Resolution depends on the number of microcomputer counter clock pulses that are generated while the INT output status is "high" at the maximum input voltage 2.5 V (V_{CC} – 2.5 V).
When the microcomputer counter clock frequency is 8 MHz, the resolution can be calculated by using the constant calculated above, as follows;

$$\frac{4700\ \text{pF} \times \dfrac{(2.5 + 0.13)}{50\ \mu\text{A}}}{\dfrac{1}{8\ \text{M}}} \approx 2^{11}$$

Therefore, the resolution of this system is approximately 11 bits.

2. 4-channel 12-bit A/D converter system
   Separate power supplies to analog section and digital section, analog input voltage range mode wider up to V_{DD}, external reference voltage for integration.



Note: C_{REF}: To stabilize reference voltage, be sure to connect capacitance of approximately 4700 pF.
C_{INT}: We suggest that this capacitance be connected to prevent malfunction due to noise.
Use C_I that leaks as slight current as possible. To prevent leak to the circuit board, we recommend providing guard ring (7), (9).

Because separate power supplies are provided for the analog are digital sections, the M62301 has two supply voltage V_{CC} and V_{DD}, enabling a wide analog input voltage range V_{IA}. The upper limit of the range is required to be no more than the difference between $V_{CC} - 2.5$ V as well as V_{DD}, therefore, the analog input voltage range in this application is 0 V to 5 V.
When the counter clock frequency is 8 MHz, resolution is;

$$\frac{6800\ \text{pF} \times \dfrac{(5 + 0.13)}{50\ \mu\text{A}}}{\dfrac{1}{8\ \text{M}}} \approx 2^{12}$$

An A/D converter system with resolution of approximately 12 bits can be formed.

Recommended operational settings according to clock frequency, resolution, and time required for discharge (decoder mode 1)

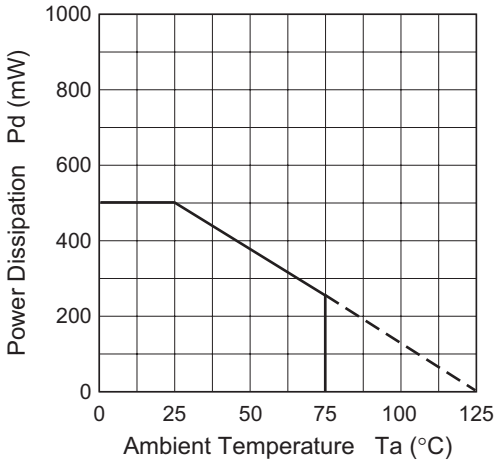
Counter Clock	Resolution	Change Current I_I (μA)	Resistance to Determine Constant Current R_I (kΩ)	Integration Capacitance C_I	Discharge Time Tdi (μs)
8 MHz	10-bit	50	24	1400 pF	7.7
		100	12	2800 pF	15.4
	11-bit	50	24	2800 pF	15.4
		100	12	5600 pF	30.7
	12-bit	50	24	5600 pF	30.7
		100	12	12000 pF	65.9
16 MHz	10-bit	50	24	700 pF	3.9
		100	12	1400 pF	7.7
	11-bit	50	24	1400 pF	7.7
		100	12	2800 pF	15.4
	12-bit	50	24	2800 pF	15.4
		100	12	5600 pF	30.7

Note: 1. Discharge time $Tdi = \left(C_I \times \frac{(V_{IAmax} + 0.49)}{1\ mA} \right)$

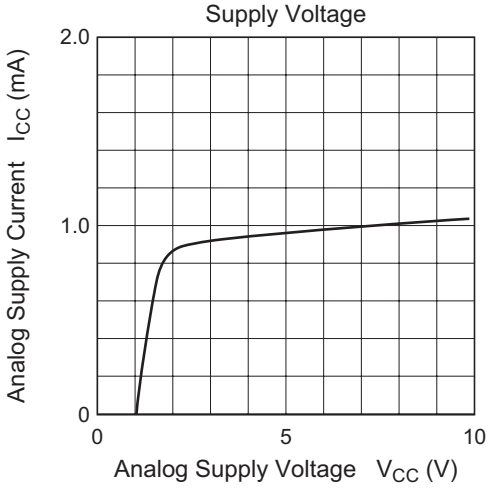
The values in this table apply when V_{IAmax} is 5 V.

Typical Characteristics

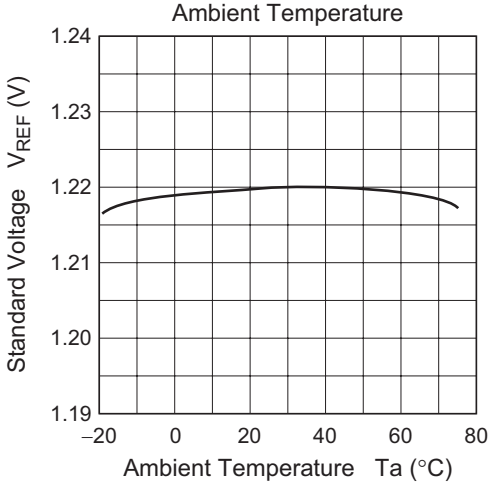
Thermal Derating



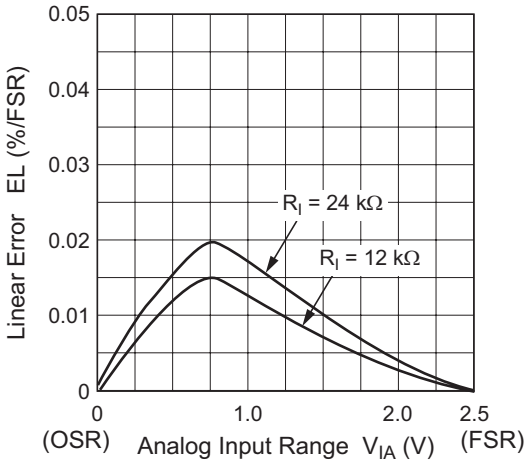
Analog Part Supply Current vs. Supply Voltage



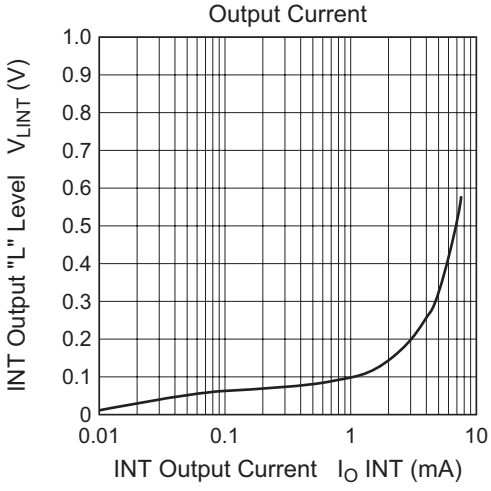
Standard Voltage vs. Ambient Temperature



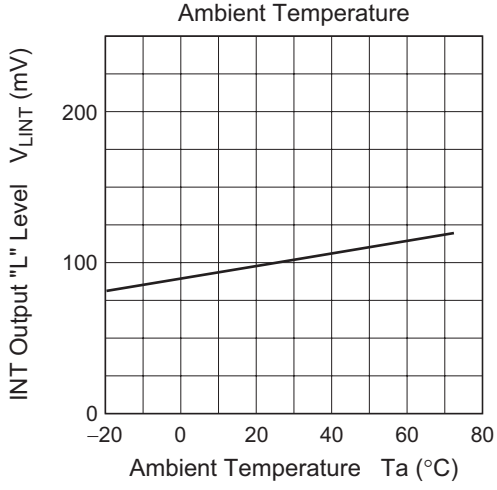
Linear Error



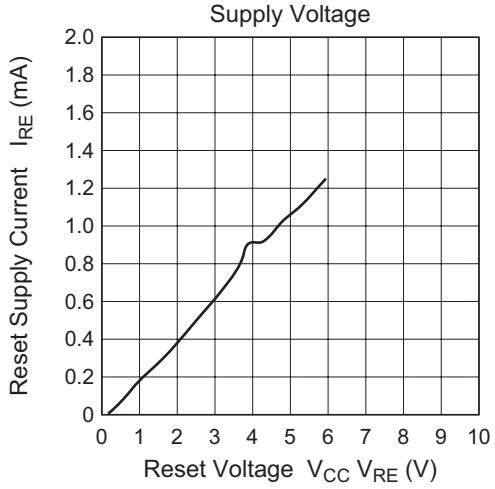
INT Output "L" Level vs. Output Current



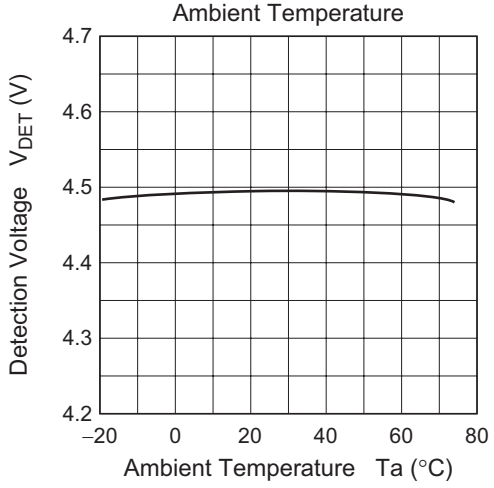
INT Output vs. Ambient Temperature



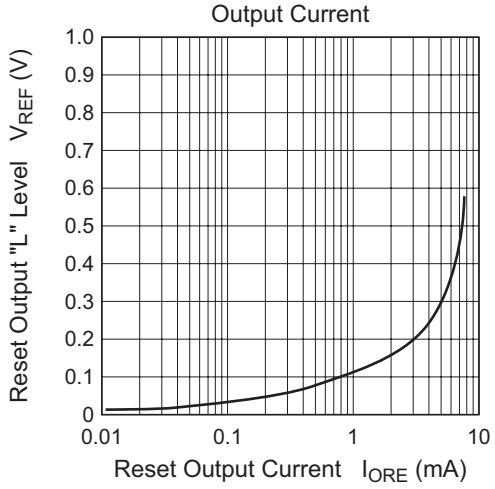
Reset Supply Current vs. Supply Voltage



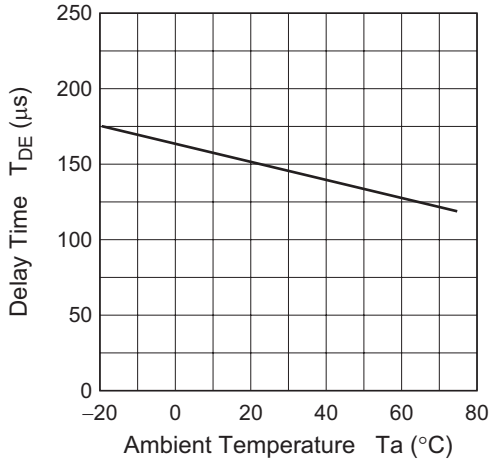
Detection Voltage vs. Ambient Temperature



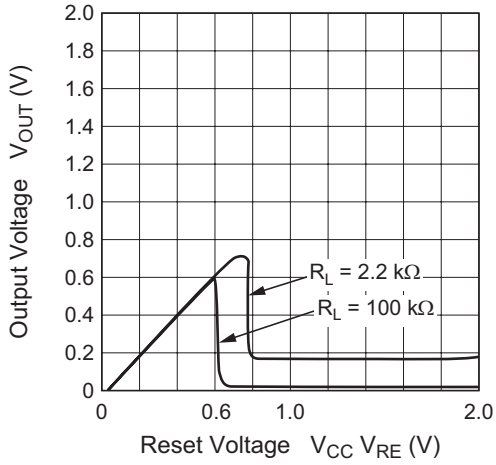
Reset Output "L" Level vs. Output Current



Delay Time vs. Ambient Temperature

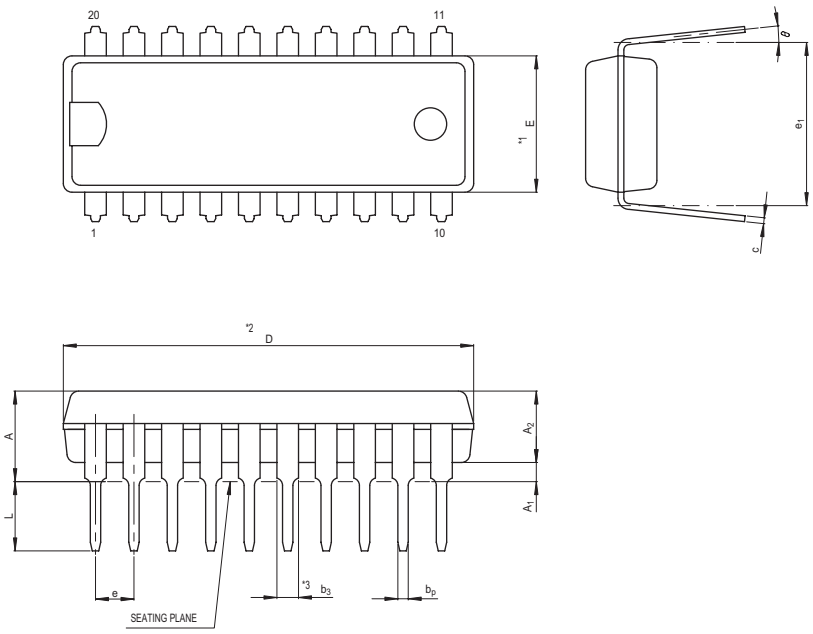


Limit Reset Voltage



Package Dimensions

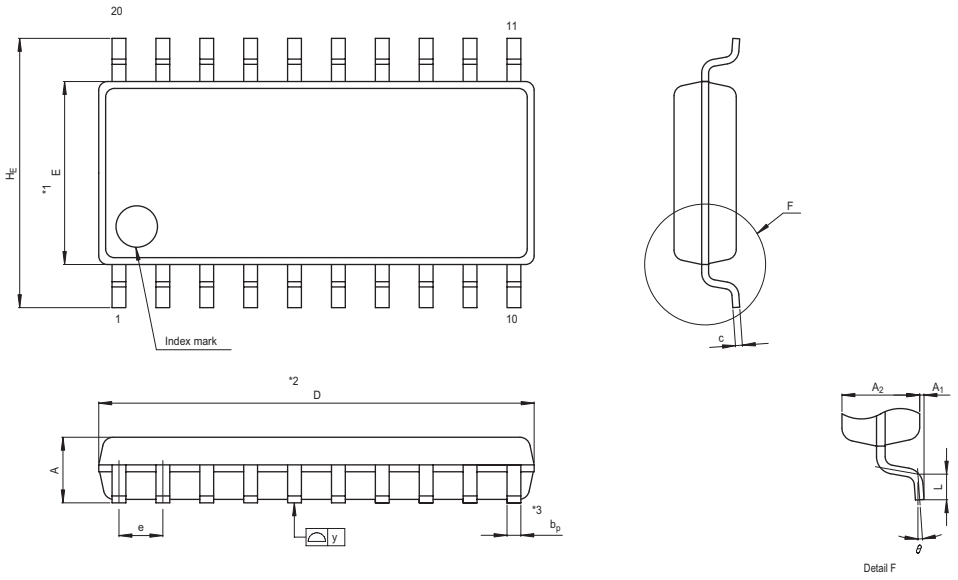
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP20-6.3x19-1.78	PRDP0020BA-A	20P4B	1.0g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	18.8	19.0	19.2
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.38	0.48	0.58
b_3	0.9	1.0	1.3
c	0.22	0.27	0.34
θ	0°	—	15°
e	1.528	1.778	2.028
L	3.0	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.3x12.6-1.27	PRSP0020DA-A	20P2N-A	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	12.5	12.6	12.7
E	5.2	5.3	5.4
A_2	—	1.8	—
A_1	0	0.1	0.2
A	—	—	2.1
b_p	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8

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