STL40DN3LLH5

Dual N-channel 30 V, 0.016 Ω typ., 11 A STripFET™ V Power MOSFET in a PowerFLAT™ 5x6 double island

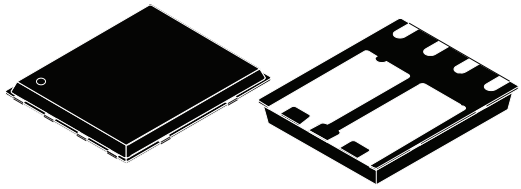
Datasheet — production data

Features

Order code	V_{DSS}	$R_{DS(on)}$ max.	I_D
STL40DN3LLH5	30 V	< 0.018 Ω	11 A (1)

1. The value is rated according $R_{thj\text{-}pcb}$

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



PowerFLAT™ 5x6 double island

Applications

- Automotive switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™ V technology. The device has been optimized to achieve very low on-state resistance, contributing to a FOM that is among the best in its class.

Figure 1. Internal schematic diagram

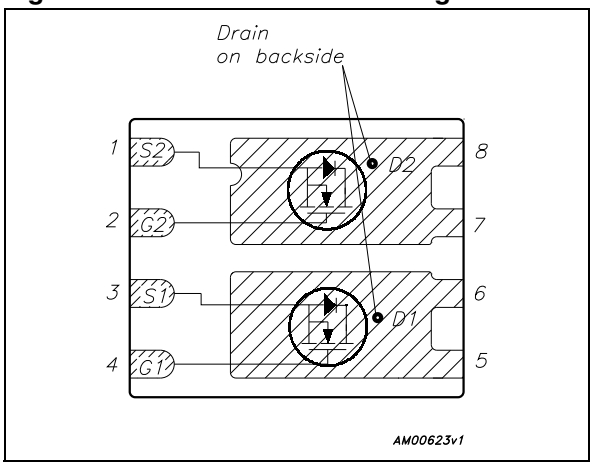


Table 1. Device summary

Order code	Marking	Package	Packaging
STL40DN3LLH5	40DN3LLH5	PowerFLAT™ 5x6 double island	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 22	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	40	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	26	A
I_D (2)	Drain current (continuous) at T_C = 25 °C	11	A
I_D (2)	Drain current (continuous) at T_C=100°C	7	A
I_{DM} (3)	Drain current (pulsed)	44	A
P_{TOT} (1)	Total dissipation at T_C = 25°C	60	W
P_{TOT} (2)	Total dissipation at T_C = 25°C	4	W
	Derating factor	0.03	W/°C
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. The value is rated according $R_{thj\text{-}c}$
2. The value is rated according $R_{thj\text{-}pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case drain, steady state	2.08	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-ambient	32	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 30 V, V_{DS} = 30 V @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 22 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1	1.5		V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 5.5 A V_{GS}= 4.5 V, I_D= 5.5 A		0.016 0.02	0.018 0.025	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	475 97 19	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15 V, I_D = 11 A V_{GS} =4.5 V *(see Figure 13)*	-	4.5 1.7 1.9	-	nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=15 V, I_D= 11 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 12)*	-	4 22 13 2.8	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
I_{SDM}(1)	Source-drain current (pulsed)		-		44	A
V_{SD}(2)	Forward on voltage	I_{SD} = 11 A, V_{GS}=0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD}=25 V, Tj=150 °C	-	16.2 1 8.1		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

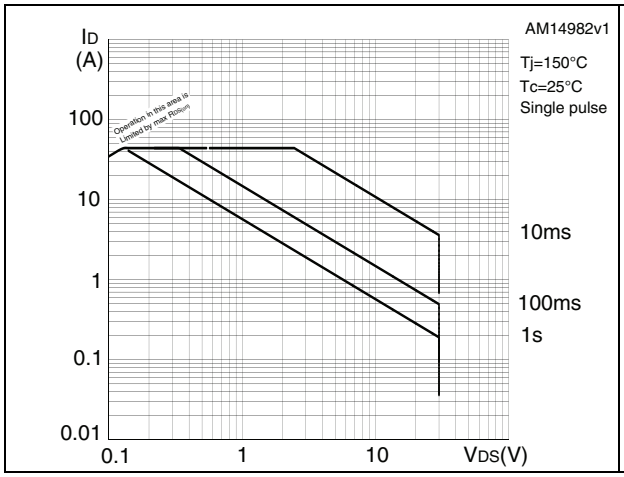


Figure 3. Thermal impedance

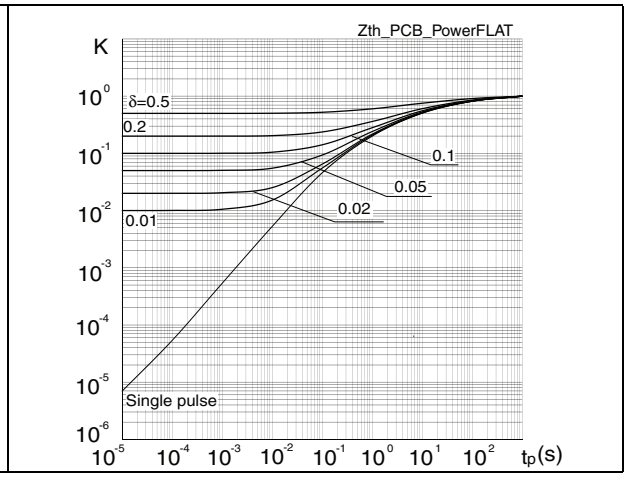


Figure 4. Output characteristics

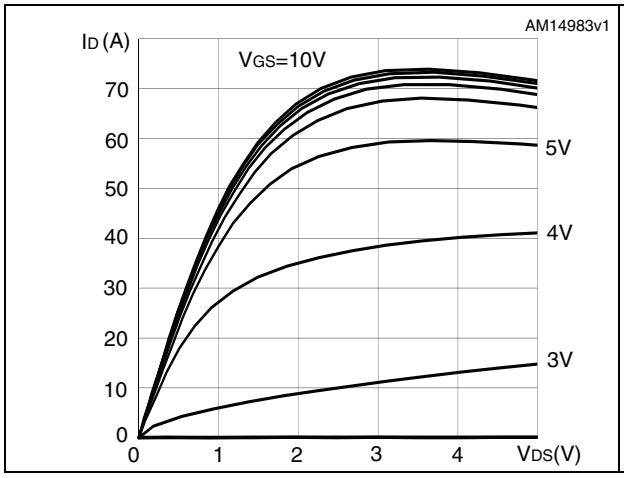


Figure 5. Transfer characteristics

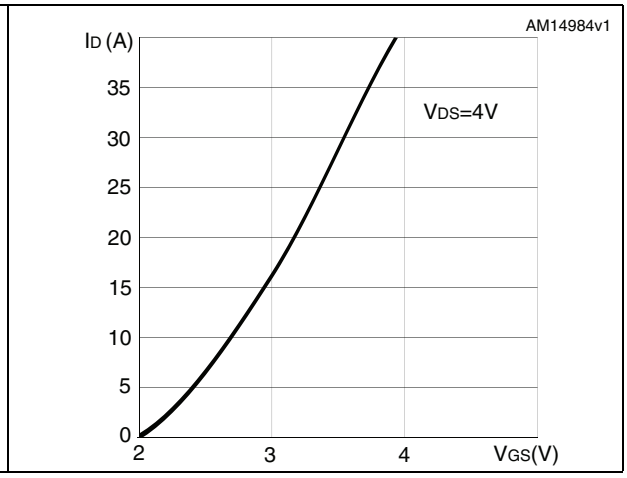


Figure 6. Normalized B_{VDSS} vs temperature

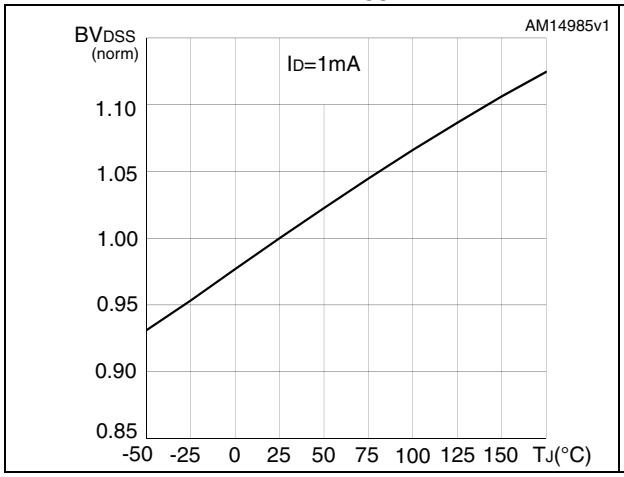


Figure 7. Static drain-source on-resistance

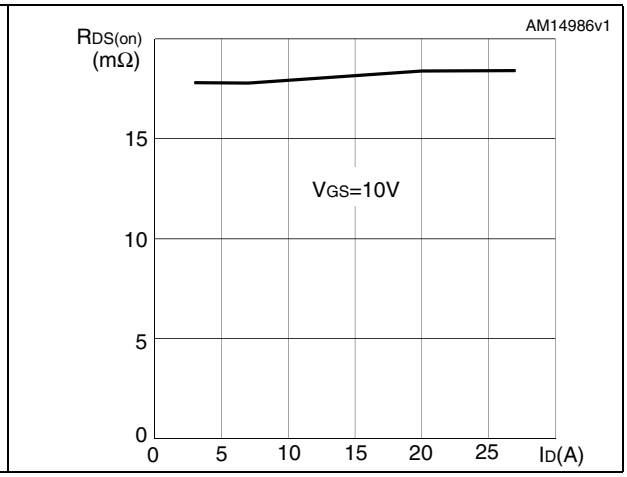


Figure 8. Gate charge vs gate-source voltage

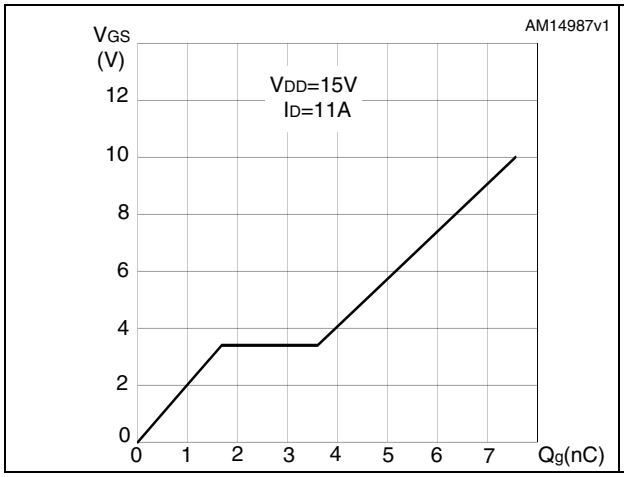


Figure 9. Capacitance variations

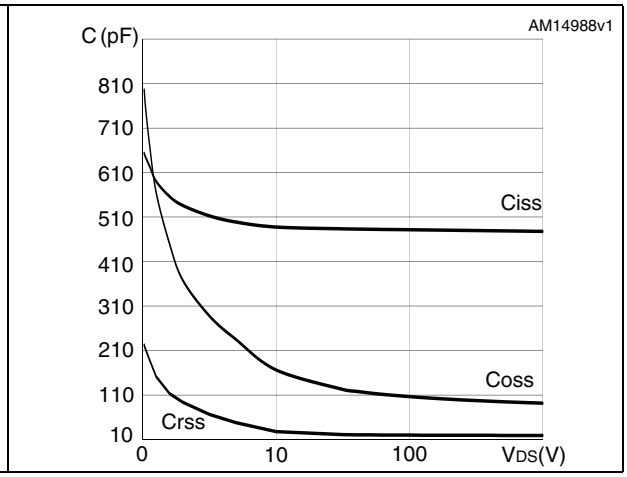


Figure 10. Normalized gate threshold voltage vs temperature

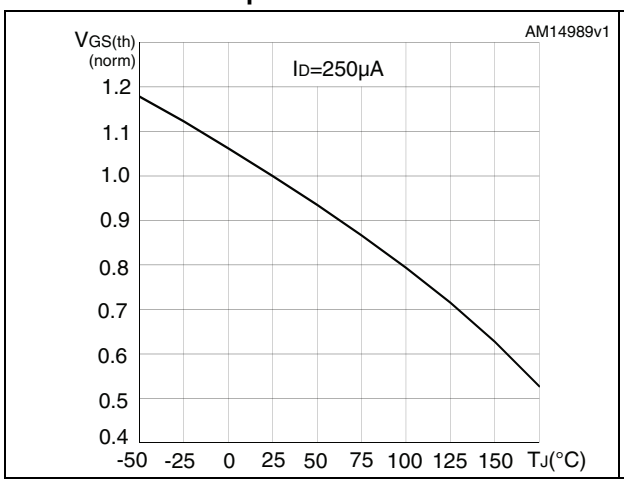
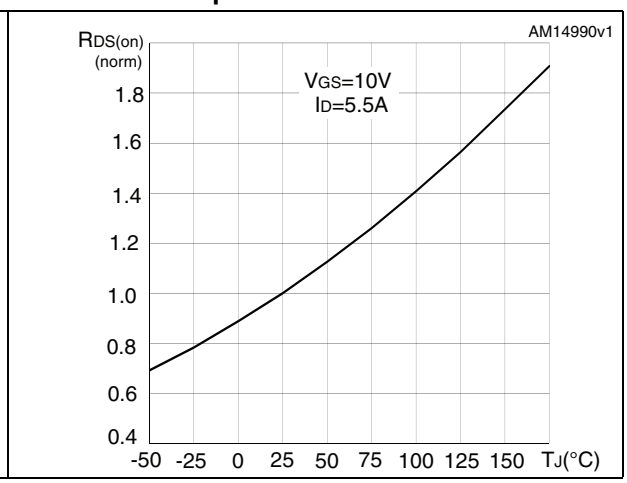


Figure 11. Normalized on-resistance vs temperature



3 Test circuits

Figure 12. Switching times test circuit for resistive load

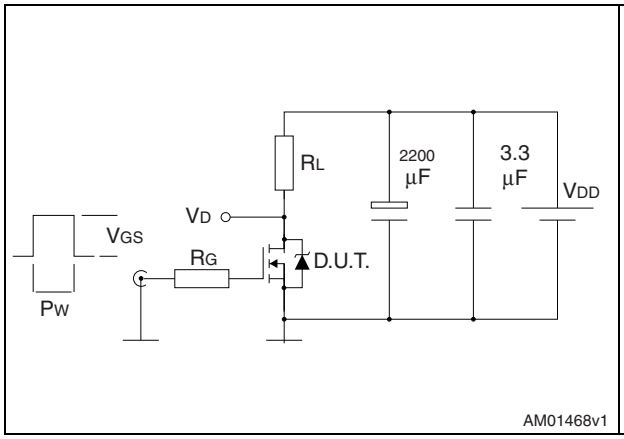


Figure 13. Gate charge test circuit

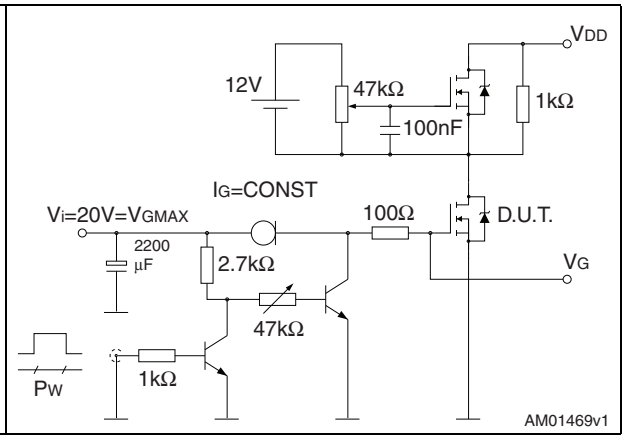


Figure 14. Test circuit for inductive load switching and diode recovery times

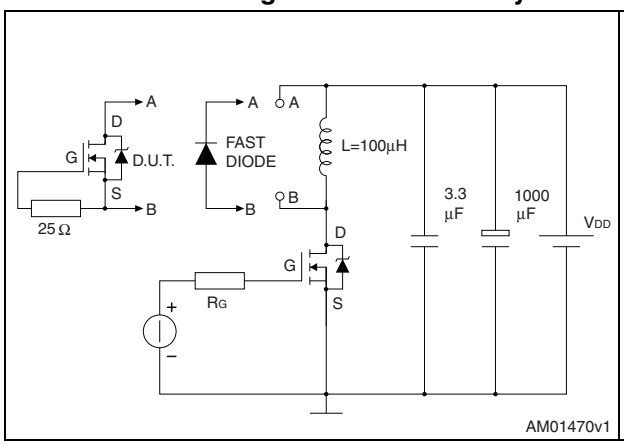


Figure 15. Unclamped inductive load test circuit

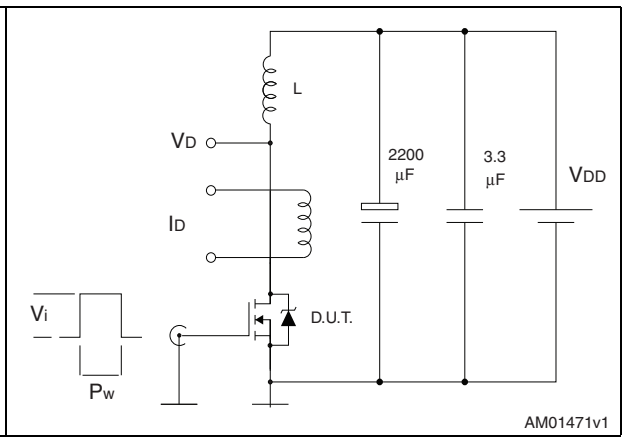


Figure 16. Unclamped inductive waveform

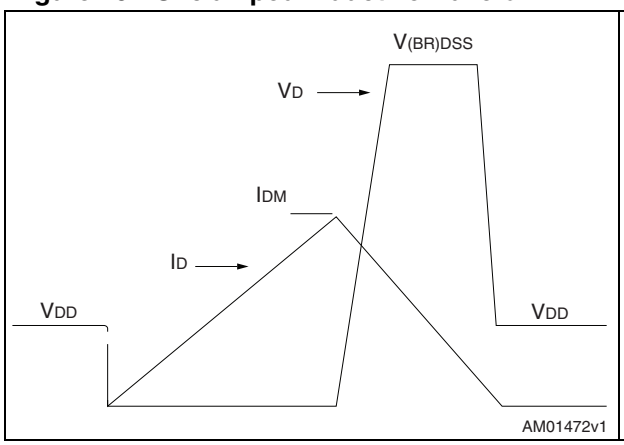
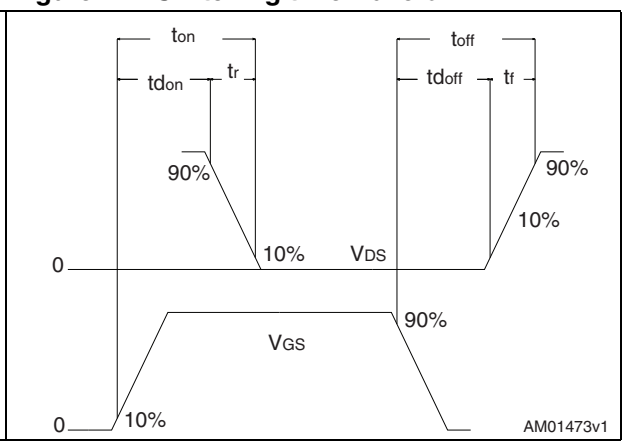


Figure 17. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
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Table 8. PowerFLAT™ 5x6 - 8 leads dual pad (ribbon) mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.50		0.80
K	1.275		1.575

Figure 18. PowerFLAT™ 5x6 - 8 leads dual pad drawing (dimensions are in mm)

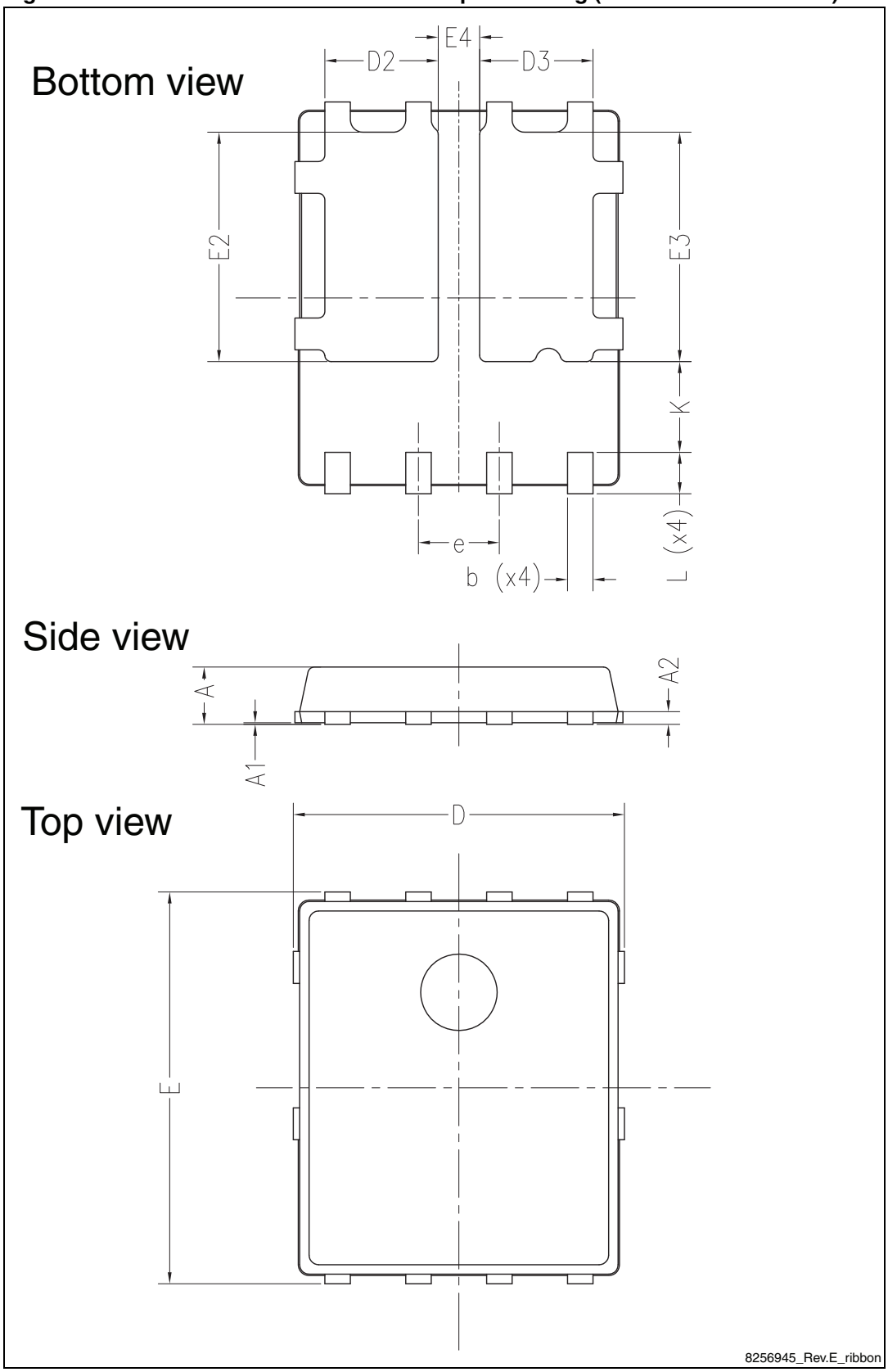
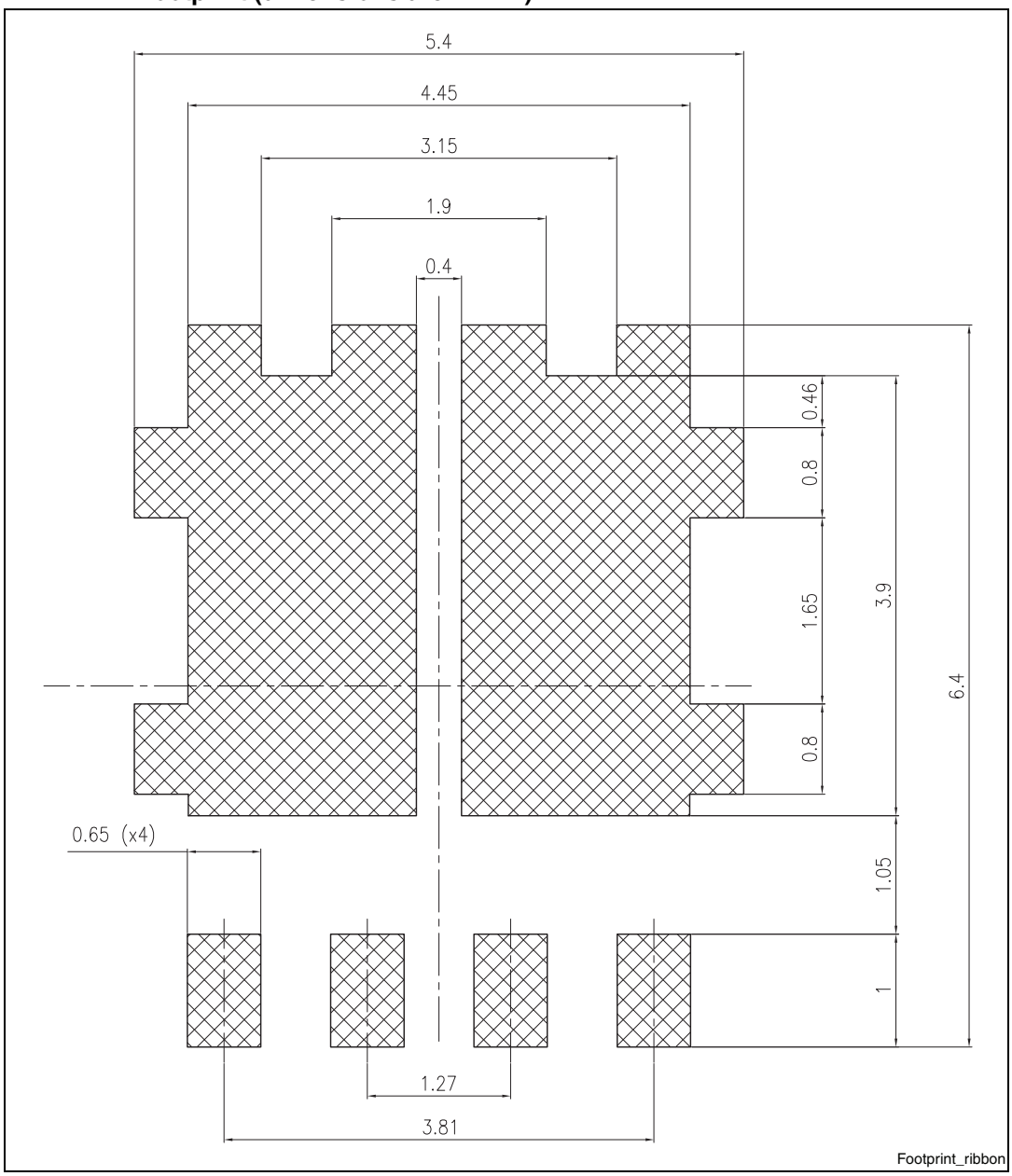


Figure 19. PowerFLAT™ 5x6 - 8 leads dual pad (ribbon) drawing recommended footprint (dimensions are in mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-Jan-2011	1	First release.
03-Oct-2012	2	*Section 2.1: Electrical characteristics (curves)* has been added. Document status promoted from preliminary data to datasheet. Minor text changes.
14-Dec-2012	3	Modified the Applications section on the coverpage to "Automotive switching applications".

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