Advance Information Data Sheet

TMOS E-FET™
Power Field Effect Transistor DPAK For Surface Mount or Insertion Mount

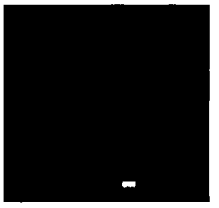
N-Channel Enhancement Mode Silicon Gate

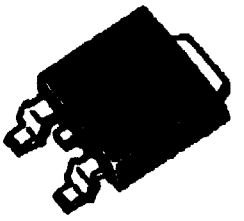
MTD3055V

TMOS POWER FET
12 AMPERES
60 VOLTS
RDS(on) = 0.15 OHM

This advanced TMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters, PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- IDSS and VDS(on) Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13-inch/ 2500 Unit Tape & Reel, Add -T4 Suffix to Part Number
- Available in Insertion Mount, Add -1 or 1 to Part Number





CASE369A-13

MAXIMUM RATINGS (TJ = 25 °C Unless Otherwise Noted.)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	VDSS	60	Vdc
Drain-to-Gate Voltage, (RGS = 1 MΩ)	VDGR	60	Vdc
Gate-to-Source Voltage- Continuous	VGS	±20	Vdc
- Non-repetitive (tp ≤ 10 ms)	VGSM	±20	Vpk
Drain Current - Continous @ Tc = 25 °C	ID	12	Adc
- Continous @ Tc = 100 °C	ID	7.3	
- Single Pulse (tp ≤ 10 µs)	IDM	37	Apk
Total Power Dissipation @ Tc = 25 °C	PD	40	Watts
Derate above 25 °C		0.32	W/°C
Total Power Dissipation @ Tc = 25 °C (1)		1.75	Watts
Operating and Storage Temperature Range	Tj and Tstg	-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy - STARTING TJ = 25 °C (VDD = 25 Vdc, VGS = 10 Vdc, PEAK IL = 12 Apk, L = 0 mH, RG = 25 Ω)	EAS	TBD	mJ
Thermal Resistance			
-Junction to Case	RØJC	3.16	°C/W
-Junction-to-Ambient	RØJA	100	
-Junction-to-Ambient(1)	RØJA	71.4	
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 sec.	TL	260	°C

This data sheet contains advance information only and is subject to change without notice.

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (Tc = 25 °C Unless Otherwise Noted)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage	V(BR)DSS				Vdc
(VGS = 0 Vdc, ID = 0.25 mAdc)		60	-	-	
Temperature Coefficient (Positive)		-	65	-	mV/°C
Zero Gate Voltage Drain Current	IDSS				µAdc
(VDS = 60 Vdc, VGS = 0 Vdc)		-	-	10	
(VDS = 60 Vdc, VGS = 0 Vdc, TJ = 125 °C)		-	-	100	
Gate-Body Leakage Current	IGSS				nAdc
(VGS = ±20 Vdc, VDS = 0 Vdc)		-	-	100	
ON CHARACTERISTICS(1)					
Gate Thresghold Voltage	VGS(th)				Vdc
(VDS = VGS, ID = 250 µAdc)		2	2.7	4	
Threshold Temperature Coefficient (Negative)		-	5.4	-	mV/°C
Static Drain-to-Source On-Resistance	RDS(on)				Ohms
(VGS = 10 Vdc, ID = 6 Adc)		-	0.105	0.15	
Drain-to-Source On-Voltage (VGS = 10 Vdc)	VDS(on)				Vdc
(ID = 12 Adc)		-	-	2.2	
(ID = 6 Adc, TJ = 125 °C)		-	-	1.9	
Forward Transconductance	gFS				Mhos
(VDS = 7 Vdc, ID = 6 Adc)		4	5	-	
DYNAMIC CHARACTERISTICS					
Input Capacitance (VDS = 25 Vdc, VGS = 0 Vdc, f = 1 MHz)	Ciss	-	410	500	pF
Output Capacitance	Coss	-	130	180	
Transfer Capacitance	Crss	-	25	50	
SWITCHING CHARACTERISTICS(2)					
Turn-On Delay Time (VDD = 30 Vdc, ID = 12 Adc, VGS = 10 Vdc,	td(on)	-	7	10	ns
Rise Time RG = 9.1 Ω)	tr	-	34	60	
Turn-Off Delay Time	td(off)	-	17	30	
Fall Time	tf	-	18	50	
Gate Charge (VDS = 48 Vdc, ID = 12 Adc, VGS = 10 Vdc)	QT	-	12.2	17	nC
(see figure 8)	Q1	-	3.2	-	
	Q2	-	5.2	-	
	Q3	-	5.5	-	
SOURCE-DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	VSD				Vdc
(IS = 12 Adc, VGS = 0 Vdc)		-	1	1.6	
(IS = 12 Adc, VGS = 0 Vdc, TJ = 125 °C)		-	0.91	-	
Reverse Recovery Time (IS = 12 Adc, VGS = 0 Vdc, dIS/dt = 100 A/µ	trr	-	56	-	ns
(see figure 15)	ta	-	40	-	
	tb	-	16	-	
Reverse Recovery Stored Charge	QRR	-	0.128	-	µC
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance	Ld				nH
(Measured from drain lead 0.25" from package to center of die.		-	4.5	-	
Internal Source Inductance	Ls				
(Measured from the source lead 0.25" from package to source bond pad.)		-	7.5	-	

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

Figure 1. On-Region Characteristics

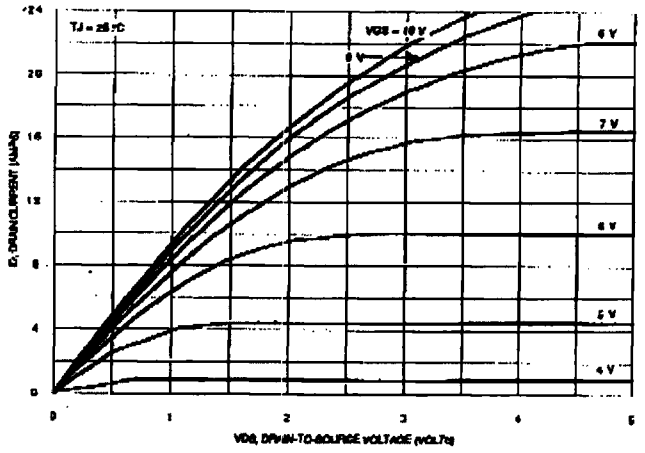


Figure 2. Transfer Characteristics

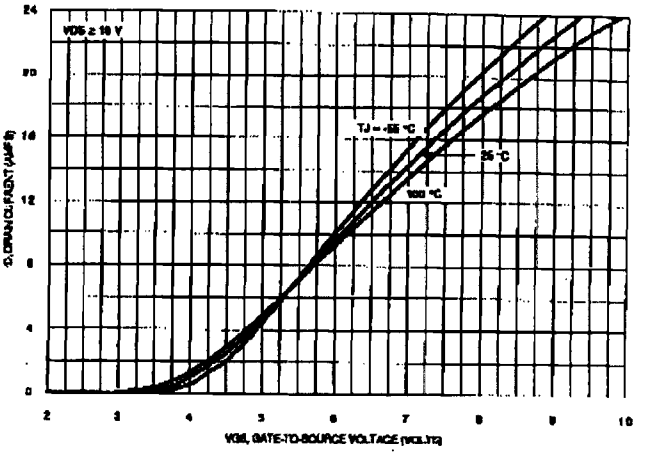


Figure 3. On-Resistance versus Drain Current and Temperature

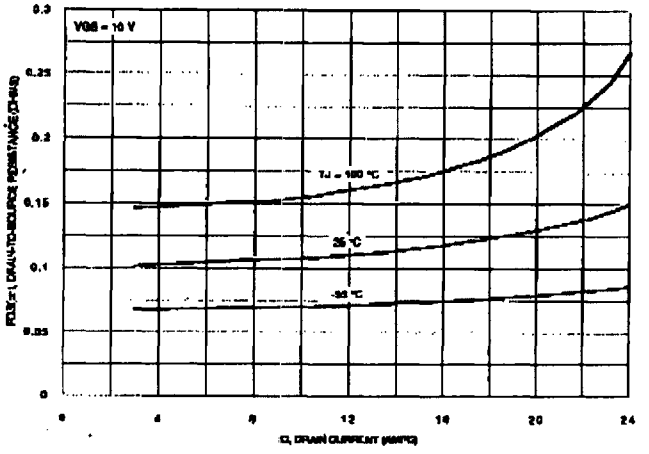


Figure 4. On-Resistance versus Drain Current and Gate Voltage

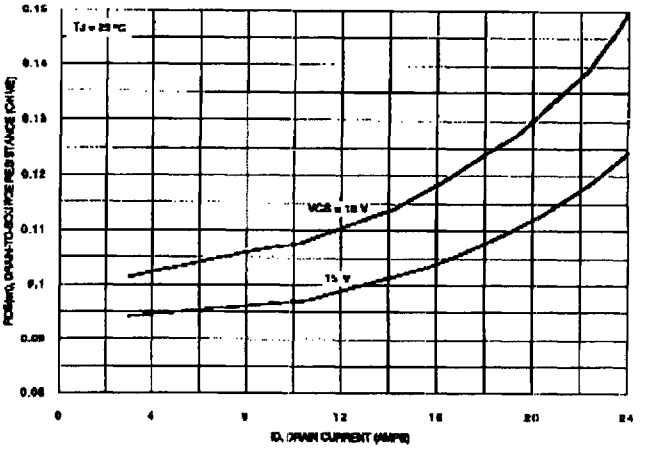


Figure 5. On-Resistance Variation with Temperature

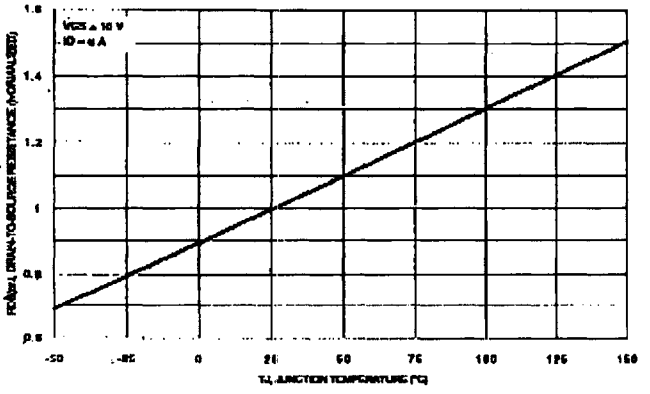


Figure 6. Drain-to-Source Leakage Current versus Voltage

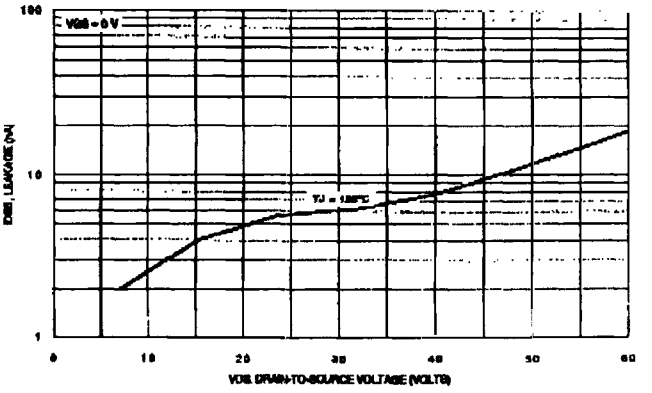


Figure 7. Capacitance Variation

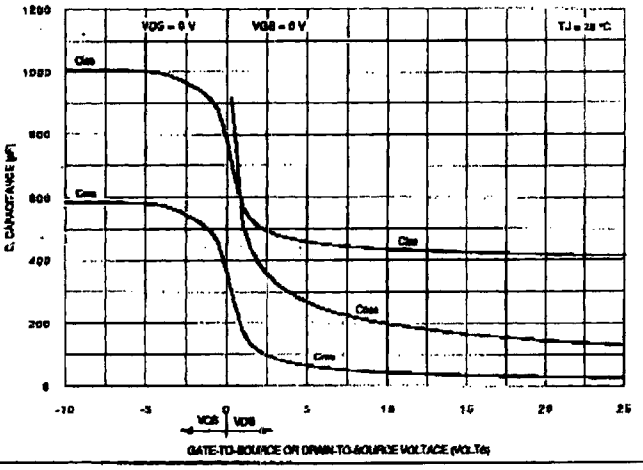


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

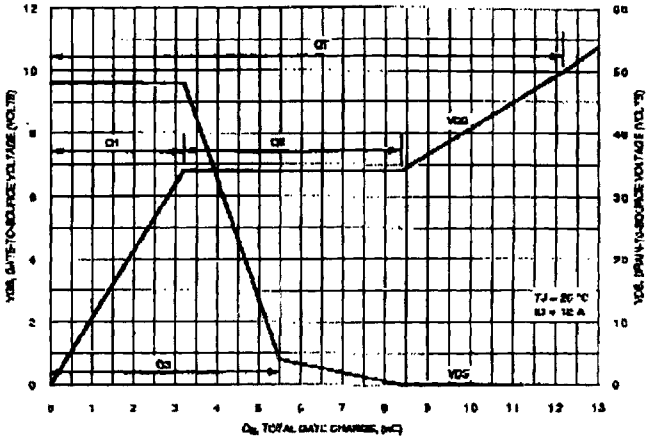


Figure 9. Resistive Switching Time Variation versus Gate Resistance

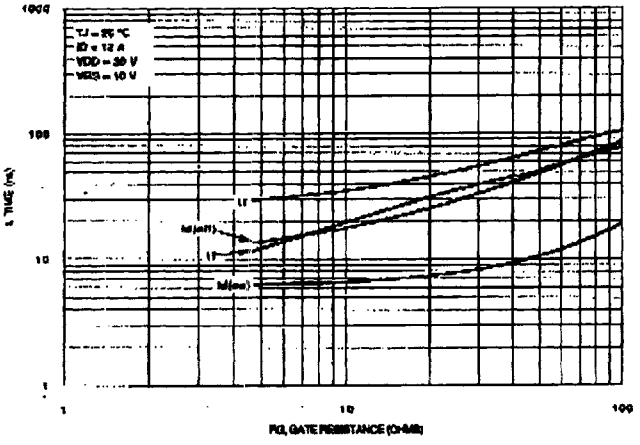


Figure 10. Stored Charge

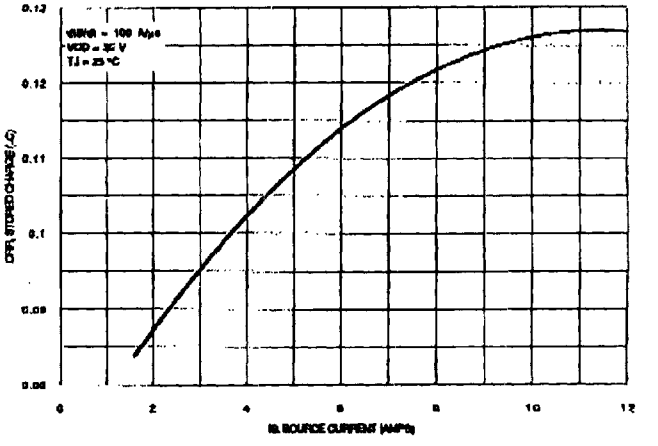


Figure 11. Diode Forward Voltage Versus Current

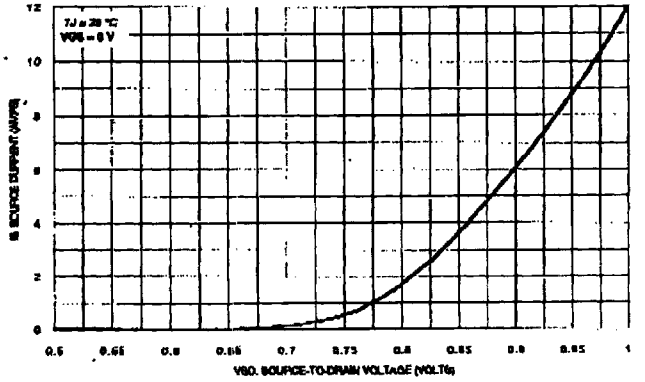
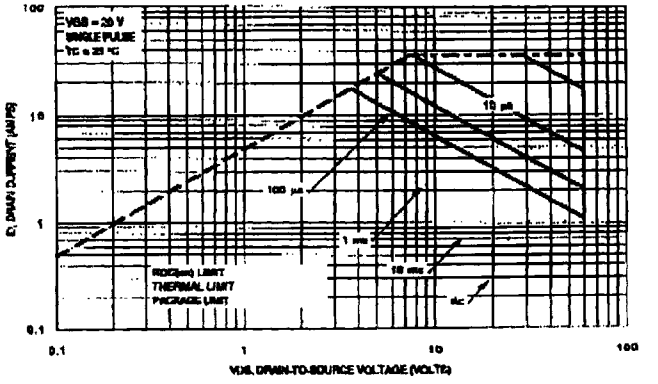


Figure 12. Maximum Rated Forward Biased Safe Operating Area



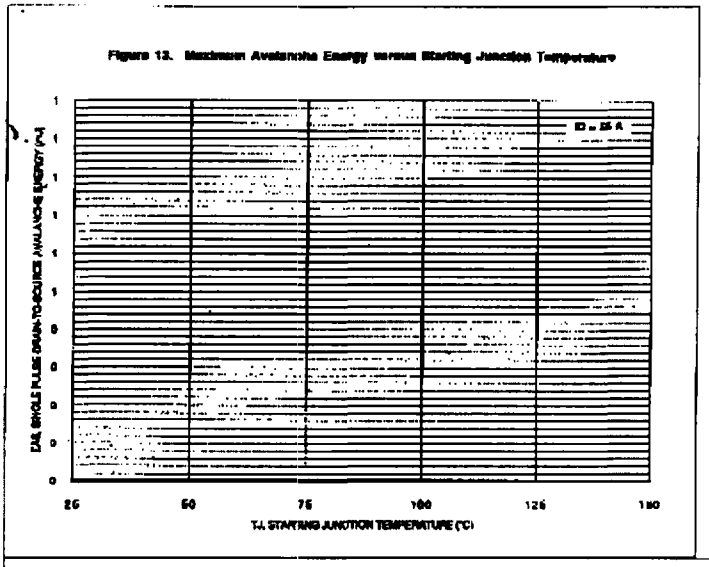


Figure 14. Thermal Response