8/16-bit Data Bus Static RAM Card

Connector Type

Two-piece 68-pin

MF365A-LCDATXX
MF3129-LCDATXX
MF3257-LCDATXX
MF3513-LCDATXX
MF31M1-LCDATXX
MF32M1-LCDATXX

DESCRIPTION

Mitsubishi's static RAM cards provide large memory capacities on a device approximately the size of a credit card (85.6mm × 54mm × 3.3mm). The cards use an 8/16-bit data bus. The devices use a replaceable lithium battery to maintain data. Available in 64 K byte - 2 M byte capacities, Mitsubishi's Static RAM cards are available with a 63-pin, two-piece connector.

- Electrostatic discharge protection to 15kV
- Buffered interface
- 68-pin connector
- 8 -bit and 16-bit data width
- Write protect switch
- Battery voltage pin

FEATURES

- Uses TSOP (Thin Small Outline Package) to achieve very high memory density coupled with high reliability, without enlarging card size.

APPLICATIONS

- Office automation
- Data Communications
- Computers
- Industrial
- Telecommunications
- Consumer

PRODUCT LIST

Item / Type name	Memory capacity	Low power	Attribute memory	Auxiliary battery	Memory organization	Outline drawing
MF365A-LCDATXX	64KB	YES	NO	NO	256K bit SRAM × 2	68P-003
MF3129-LCDATXX	128KB				256K bit SRAM × 4	
MF3257-LCDATXX	256KB				1 M bit SRAM × 2	
MF3513-LCDATXX	512KB				1 M bit SRAM × 4	
MF31M1-LCDATXX	1 MB				1 M bit SRAM × 8	
MF32M1-LCDATXX	2 MB				1 M bit SRAM × 16	

PIN ASSIGNMENT

Two-Piece Type (68-pin)

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D3		36	$\overline{CD1}$	Card detect 1
3	D4		37	D11	
4	D5	Data I/O	38	D12	
5	D6		39	D13	Data I/O
6	D7		40	D14	
7	$\overline{CE1}$	Card enable 1	41	D15	
8	A10	Address input	42	$\overline{CE2}$	Card enable 2
9	$\overline{OE}$	Output enable	43	NC	
10	A11		44	NC	No connection
11	A9		45	NC	
12	A8	Address input	46	A17	A17(NC for ≤128KB types
13	A13		47	A18	A18(NC for ≤256KB types Address input
14	A14		48	A19	A19(NC for ≤512KB types
15	$\overline{WE}$	Write enable	49	A20	A20(NC for ≤1MB types
16	NC	No connection	50	NC	No connection
17	Vcc	Power supply voltage	51	Vcc	Power supply voltage
18	NC	No connection	52	NC	
19	A16	A16 (NC for 64KB type)	53	NC	
20	A15		54	NC	
21	A12		55	NC	
22	A7		56	NC	No connection
23	A6		57	NC	
24	A5	Address input	58	NC	
25	A4		59	NC	
26	A3		60	NC	
27	A2		61	$\overline{REG}$	REG function
28	A1		62	BVD2	Battery voltage detect 2
29	A0		63	BVD1	Battery voltage detect 1
30	D0		64	D8	
31	D1	Data I/O	65	D9	Data I/O
32	D2		66	D10	
33	WP	Write protect	67	$\overline{CD2}$	Card detect 2
34	GND	Ground	68	GND	Ground

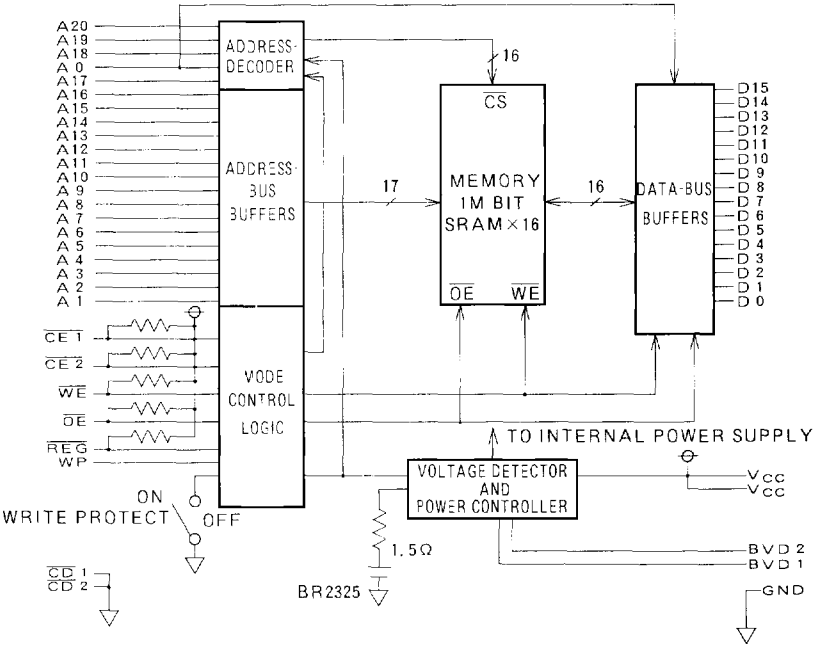
WRITE PROTECT MODE (WP)

When the write protect switch is switched on, this card goes into a write protect mode that allows seading but not writing of data.

In this mode, the WP pin is set to "H" level when V_{CC} is applied.

At shipment the write protect switch is switched off (Normal mode : The card can be written ; WP pin set to "L" level).

BLOCK DIAGRAM (2 MB)



FUNCTION TABLE

Mode	REG	CE 1	CE 2	OE	WE	A 0	D15~D 8	D 7~D 0	Icc
Standby	X	H	H	X	X	X	High impedence	High impedence	Standby
Read A (16-bit) common	H	L	L	L	H	X	Odd byte data out	Even byte data out	Active
Write A (16-bit) common	H	L	L	H	L	X	Odd byte data in	Even byte data in	Active
Read B (8-bit) common	H	L	H	L	H	L	High-impedance	Even byte data out	Active
	H	L	H	L	H	H	High-impedance	Odd byte data out	Active
Write B (8-bit) common	H	L	H	H	L	L	High-impedance	Even byte data in	Active
	H	L	H	H	L	H	High-impedance	Odd byte data in	Active
Read C (8-bit) common	H	H	L	L	H	X	Odd byte data out	High-impedance	Active
Write C (8-bit) common	H	H	L	H	L	X	Odd byte data in	High-impedance	Active
Output disable	X	X	X	H	H	X	High-impedance	High-impedance	Active
Read A (16-bit) attribute	L	L	L	L	H	X	Data out (not valid)	Data out (FFh)	Active
Read B (8-bit) attribute	L	L	H	L	H	L	High-impedance	Data out (FFh)	Active
	L	L	H	L	H	H	High-impedance	Data out (not valid)	Active
Read C (8-bit) attribute	L	H	L	L	H	X	Data out (not valid)	High-impedance	Active

Note 1 : H = V_{IH}, L = V_{IL}, X = V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～0.6	V
V_I	Input voltage		−0.3～V_{CC}+0.3	V
V_O	Output voltage		0～V_{CC}	V
T_{opr} 1	Operating temperature 1	Read, Write, Operation	0～70	℃
T_{opr} 2	Operating temperature 2	Data retention	0～70	℃
T_{stg}	Storage temperature		−30～80	℃

RECOMMENDED OPERATING CONDITIONS (T_a= 0～55℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	V_{CC} supply voltage	4.50	5.0	5.25	V
GND	System ground		0		V
V_{IH}	High input voltage	3.5		V_{CC}	V
V_{IL}	Low input voltage	0		0.8	V

ELECTRICAL CHARACTERISTICS (T_a= 0～55℃, V_{CC}=4.50～5.25V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High output voltage	I_{OH} = −1.0mA		2.4			V
V_{OL}	Low output voltage	I_{OL} = 1 mA				0.4	V
I_{IH}	High input current	V_I = V_{CC} V				10	μA
I_{IL}	Low input current	V_I = 0 V	$\overline{CE1}$, $\overline{CE2}$, $\overline{WE}$, $\overline{OE}$, $\overline{REG}$	−10		−70	μA
			Other inputs			−10	
I_{OZH}	High output current in state	$\overline{CE1}$ = $\overline{CE2}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_O = V_{CC}				10	μA
I_{OZL}	Low output current in off state	$\overline{CE1}$ = $\overline{CE2}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_O = 0 V				−10	μA
I_{CC}1・1	Active supply current	Other inputs V_{IH} or V_{IL}, Outputs=open, Cycle time=250ns	16bit			160	mA
			8 bit			120	
I_{CC}1・2	Active supply current 2	Other inputs≤0.2V or≥V_{CC}−0.2V, Outputs=open, Cycle time=250ns	16bit			150	mA
			8 bit			110	
I_{CC}2・1	Standby supply current	$\overline{CE1}$ = $\overline{CE2}$ = V_{IH}, other inputs V_{IH} or V_{IL}, Outputs=open				10	mA
I_{CC}2・2	Standby supply current	$\overline{CE1}$ = $\overline{CE2}$ ≥ V_{CC}−0.2V, other inputs≤0.2V or≥V_{CC}−0.2V	2 MB		0.30	0.65	mA
			1 MB 512KB		0.15	0.45	
			256KB 128KB 64KB		0.15	0.30	
VBDET 1	Battery detect reference voltage 1 *	V_{CC}= 5 V, T_a=25℃		2.27	2.37	2.47	V
VBDET 2	Battery detect reference voltage 2 *	V_{CC}= 5 V, T_a=25℃		2.55	2.65	2.75	V

Note 2 : Currents flowing into the IC are taken as positive (unsigned).
3 : Typical values are measured at V_{CC}= 5 V, T_a=25℃.
*Pin asserted when battery voltage drops below specified level.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz, T_a=25℃			45	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz, T_a=25℃			45	pF

Note 4 : These parameters are not 100% tested.

SWITCHING CHARACTERISTICS

Read Cycle (T_a=0～55℃, V_{CC}=4.50～5.25V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{CR}	Read cycle time	200			ns
$t_{a(A)}$	Address access time			200	ns
$t_{a(CE)}$	Card enable access time			200	ns
$t_{a(OE)}$	Output enable access time			100	ns
$t_{dis(CE)}$	Output disable time (from $\overline{CE}$)			90	ns
$t_{dis(OE)}$	Output disable time (from $\overline{OE}$)			90	ns
$t_{en(CE)}$	Output enable time (from $\overline{CE}$)	5			ns
$t_{en(OE)}$	Output enable time (from $\overline{OE}$)	5			ns
$t_{V(A)}$	Data valid time after address change	0			ns

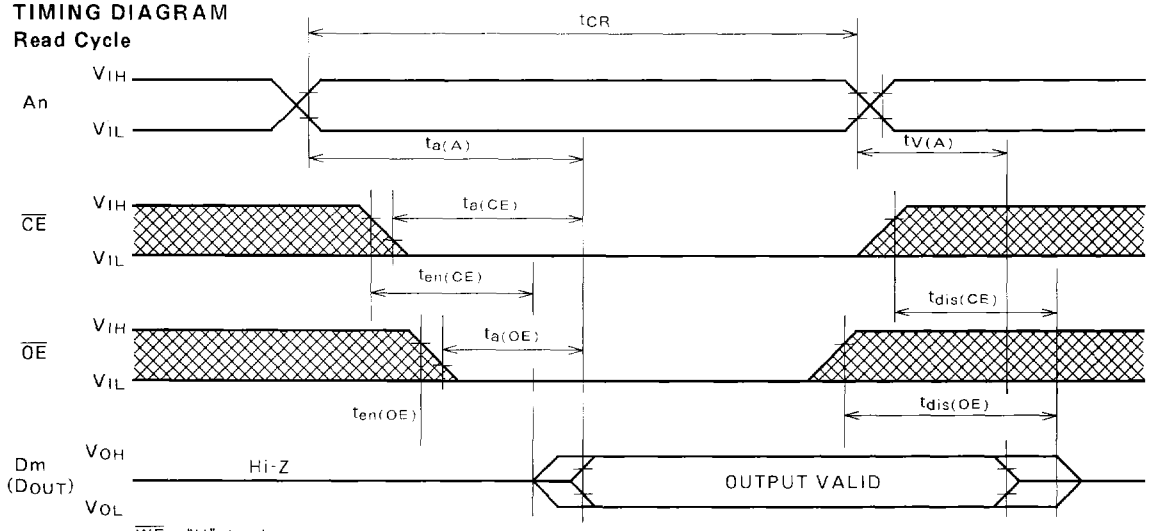
TIMING REQUIREMENTS

Write Cycle (T_a=0～55℃, V_{CC}=4.50～5.25V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{CW}	Write cycle time	200			ns
$t_{W(WE)}$	Write pulse width	120			ns
$t_{SU(A)}$	Address setup time	20			ns
$t_{SU(A-WEH)}$	Address setup time with respect to $\overline{WE}$ high	140			ns
$t_{SU(CE-WEH)}$	Card enable setup time with respect to $\overline{WE}$ high	140			ns
$t_{SU(D-WEH)}$	Data setup time with respect to $\overline{WE}$ high	60			ns
$t_{h(D)}$	Data hold time	30			ns
$t_{rec(WE)}$	Write recovery time	30			ns
$t_{dis(WE)}$	Output disable time (from $\overline{WE}$)			90	ns
$t_{dis(OE)}$	Output disable time (from $\overline{OE}$)			90	ns
$t_{en(WE)}$	Output enable time (from $\overline{WE}$)	5			ns
$t_{en(OE)}$	Output enable time (from $\overline{OE}$)	5			ns
$t_{SU(OE-WE)}$	$\overline{OE}$ setup time with respect to $\overline{WE}$ low	10			ns
$t_{h(OE-WE)}$	$\overline{OE}$ hold time with respect to $\overline{WE}$ high	10			ns

TIMING DIAGRAM

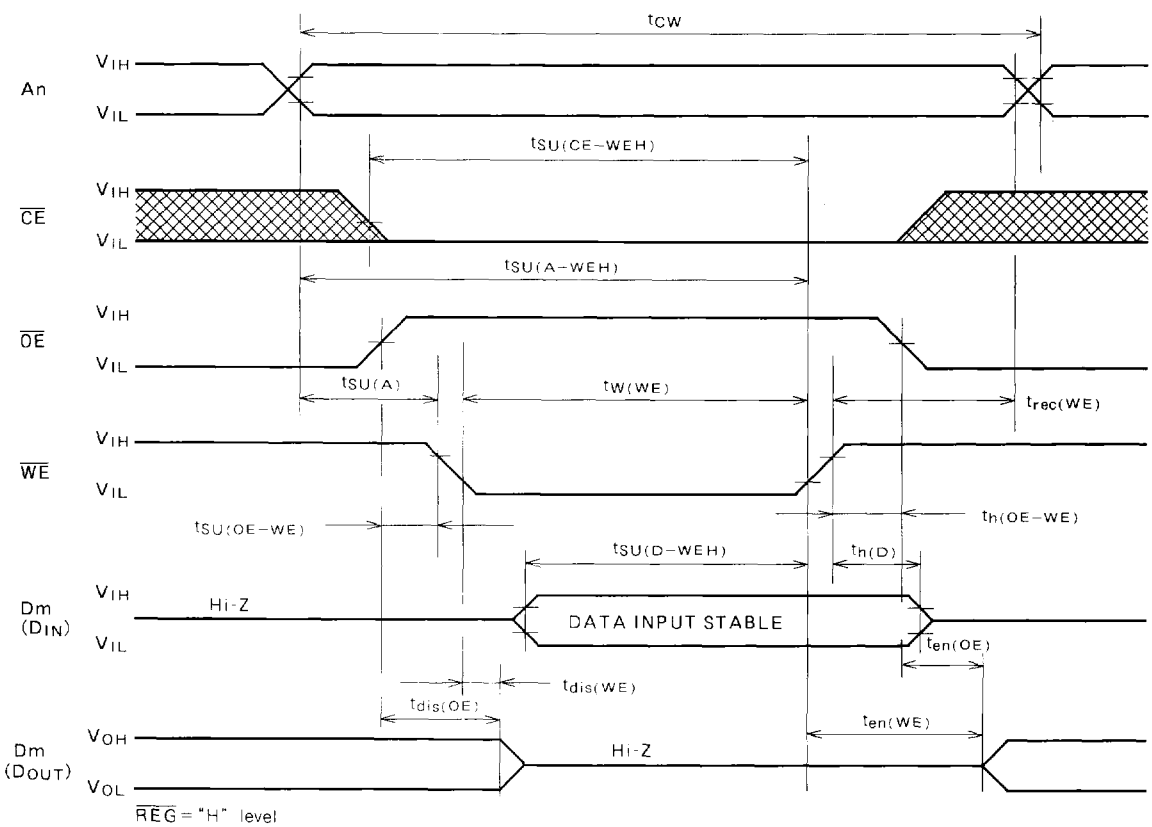
Read Cycle



WE = "H" level
REG = "H" level

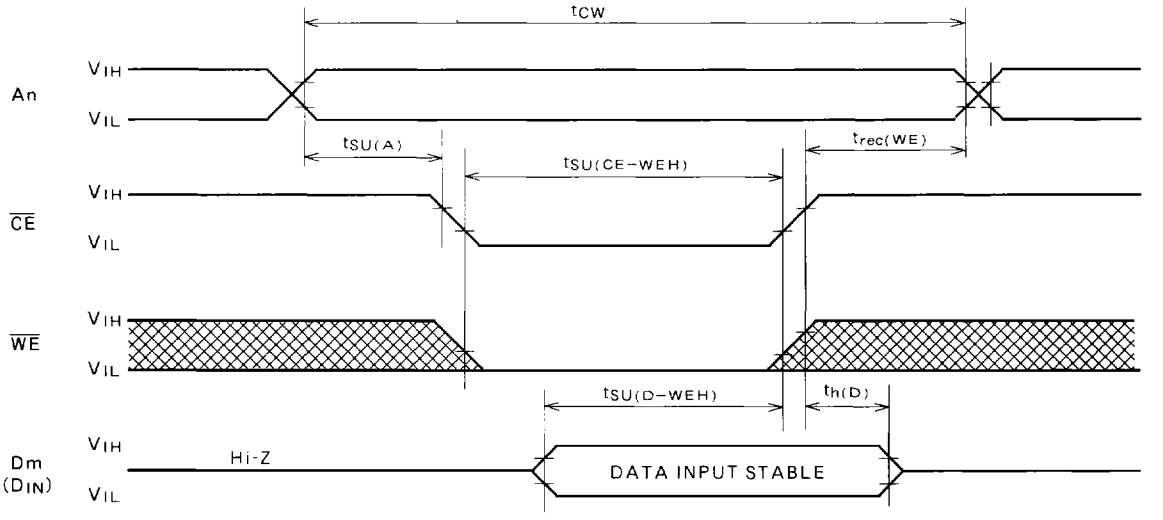
Note 5 : Indicates the don't care input.

Write Cycle (WE control)



REG = "H" level

Write Cycle ($\overline{CE}$ control)



$\overline{OE}$ = "H" level
$\overline{REG}$ = "H" level

SWITCHING CHARACTERISTICS (Attribute)

Read Cycle (T_a = 0 ~55℃, V_{CC} = 4.50~5.25V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{CR}R$	Read cycle time	300			ns
$t_{a(A)}R$	Address access time			300	ns
$t_{a(CE)}R$	Card select access time			300	ns
$t_{a(OE)}R$	Output enable access time			150	ns
$t_{dis(CE)}R$	Output disable time (from $\overline{CE}$)			100	ns
$t_{dis(OE)}R$	Output disable time (from $\overline{OE}$)			100	ns
$t_{en(CE)}R$	Output enable time (from $\overline{CE}$)	5			ns
$t_{en(OE)}R$	Output enable time (from $\overline{OE}$)	5			ns
$t_{V(A)}R$	Data valid time after address change	0			ns

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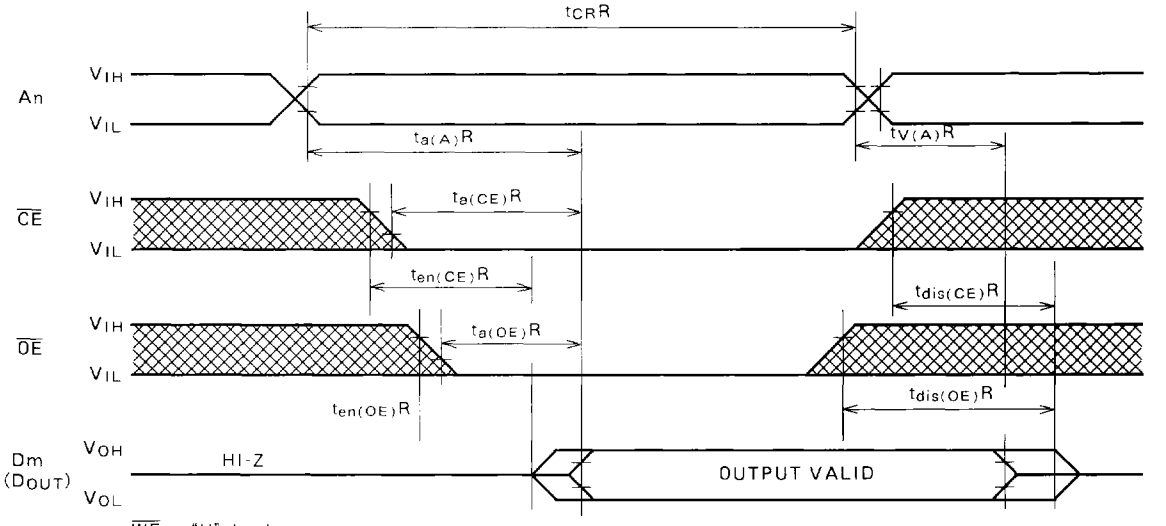
TIMING DIAGRAM (Attribute)

Read Cycle



WE = "H" level
REG = "L" level

Note 6 : Test Conditions
Input pulse levels : V_{IL} = 0.4V, V_{IH} = 4.0V
Input pulse rise, fall time : $t_r = t_f$ = 10ns
Reference voltage
Input : V_{IL} = 0.8V, V_{IH} = 3.5V
Output : V_{OL} = 0.8V, V_{OH} = 3.0V
(t_{en} and t_{dis} are measured when output voltage is ±500mV from steady state.)
Load : 100pF + 1 TTL gate
5 pF + 1 TTL gate (at t_{en} and t_{dis} measuring)

7 : The data write is performed during the interval when both $\overline{CE}$ and $\overline{WE}$ are "L" level.

8 : Don't apply inverted phase signal externally when Dm pin is in output mode.

9 : $\overline{CE}$ is indicated as follows :
Read A/Write A : $\overline{CE} = \overline{CE1} = \overline{CE2}$
Read B/Write B : $\overline{CE} = \overline{CE1}$, $\overline{CE2}$ = "H" level
Read C/Write C : $\overline{CE} = \overline{CE2}$, $\overline{CE1}$ = "H" level

ELECTRICAL CHARACTERISTICS

BATTERY BACK-UP (T_a = 0 ~55℃, unless otherwise noted)

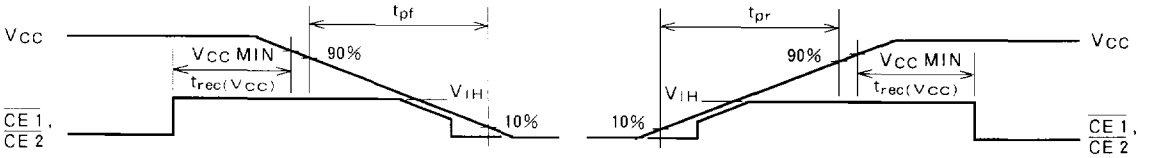
Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{BATT}	Back-up enable battery voltage	All pins open		2.6			V
$V_{I(CE)}$	Card enable voltage	2.4V ≤ V_{CC} ≤ 5.25V		2.4			V
		0 V ≤ V_{CC} < 2.4V		V_{CC} −0.1	V_{CC}	V_{CC} +0.1	
$I_{CC(BUP)}$	Battery back-up supply current	All pins open, V_{BATT} = 3 V, T_a = 25℃	64KB			3	μA
			128KB			5	
			256KB			3	
			512KB			5	
			1 MB			9	
			2 MB			17	
$I_{CC(BUP)}$	Battery back-up supply current	All pins open, V_{BATT} = 3 V,	64KB			40	μA
			128KB			70	
			256KB			100	
			512KB			200	
			1 MB			400	
			2 MB			800	

TIMING REQUIREMENTS (T_a = 0 ~55℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{pr}	Power supply rise time	0.1		300	ms
t_{pf}	Power supply fall time	3		300	ms
$t_{su(VCC)}$	Set up time at power on	20			ms
$t_{rec(VCC)}$	Recovery time at power off	1000			ns

CARD INSERTION/REMOVAL TIMING DIAGRAM

V_{CC} MIN means Minimum Operating Voltage=4.50V.



Note 10 : The battery must not be removed unless V_{CC} is present, otherwise all data will be lost.

BATTERY SPECIFICATIONS

A replaceable battery (type BR2325) with a capacity of 165mAH is used :

Estimated battery life when the card is left continuously without external power.

MF365A-LCDATXX	5.9years
MF3129-LCDATXX	3.6years
MF3257-LCDATXX	5.9years
MF3513-LCDATXX	3.6years
MF31M1-LCDATXX	2.0years
MF32M1-LCDATXX	1.1years

Conditions

Temperature : 25℃

Humidity : 60%RH