Description

GM384XA series is high performance with fixed-frequency current mode PWM controllers. They are specially designed for off-Line and DC-to-DC converter applications. They require minimal external components to precisely tailor performance in a wide variety of applications.

GM384XA series includes a trimmed oscillator for precise duty cycle control, a temperature-compensated reference, high gain error amplifier, a current-sensing comparator, and a high-current totem pole output for driving a power MOSFET.

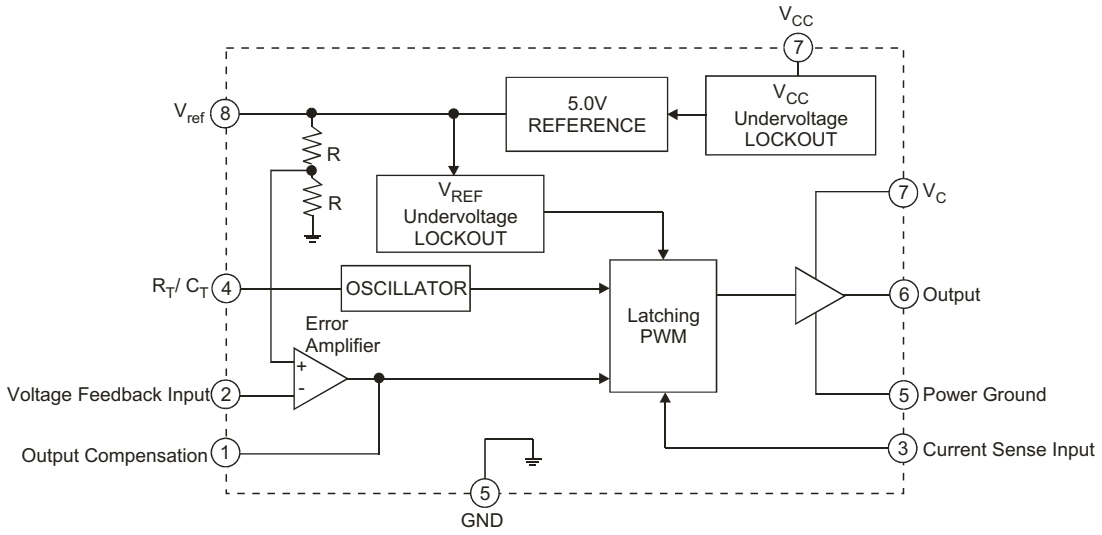
On-chip protection features include undervoltage lockouts with hysteresis for both input and reference, cycle-by-cycle current limiting, programmable output deadtime, and a latch for single pulse metering. All these are in a simple DIP-8 or SOP-8 package!

GM3842A and GM3844A have UVLO thresholds of 16V (on)/10V(off); GM3843A and GM3845A have UVLO thresholds of 8.4V (on)/ 7.6V (off). GM3842A and GM3843A operate within 100% duty cycle; GM3844A and GM3845A operate within 50% duty cycle.

Features

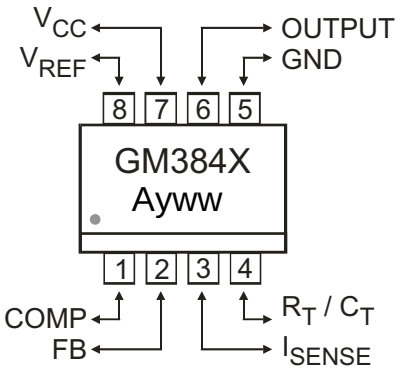
- **Low Start-Up and Operating Current**
- **Automatic Feed Forward Compensation**
- **Current Mode Operating Frequency up to 500kHz**
- **Trimmed Oscillator Discharge Current for Precise Duty Cycle Control**
- **Latching PWM for Cycle-By-Cycle Current Limiting**
- **Undervoltage Lockout with Hysteresis**
- **High Current Totem Pole Output**
- **The GM384XA Have Start-up Current 0.17mA**

SIMPLIFIED BLOCK DIAGRAM

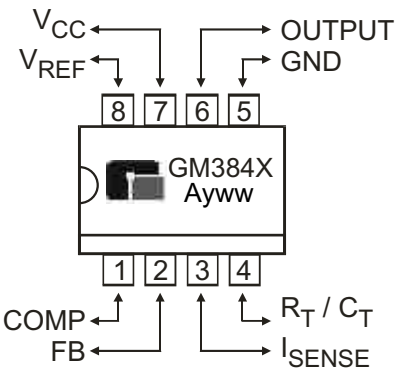


◆ MARKING INFORMATION & PIN CONFIGURATIONS (TOP VIEW)

SOP - 8



DIP - 8



A = Assembly Location
Y = Year
W W = Weekly

◆ ORDERING INFORMATION (Green Package Products are available now!)

Ordering Number	Package	Shipping
GM3842AS8T	SOP - 8	100 Units/ Tube
GM3842AS8R	SOP - 8	2,500 Units/ Tape & Reel
GM3842AD8T	DIP-8	60 Units/ Tube
GM3843AS8T	SOP - 8	100 Units/ Tube
GM3843AS8R	SOP - 8	2,500 Units/ Tape & Reel
GM3843AD8T	DIP-8	60 Units/ Tube
GM3844AS8T	SOP - 8	100 Units/ Tube
GM3844AS8R	SOP - 8	2,500 Units/ Tape & Reel
GM3844AD8T	DIP-8	60 Units/ Tube
GM3845AS8T	SOP - 8	100 Units/ Tube
GM3845AS8R	SOP - 8	2,500 Units/ Tape & Reel
GM3845AD8T	DIP-8	60 Units/ Tube

* For detail ordering number identification, please see last page.
** For green package products, please add " G" at the end of each part number.

◆ ABSOLUTE MAXIMUM RATINGS

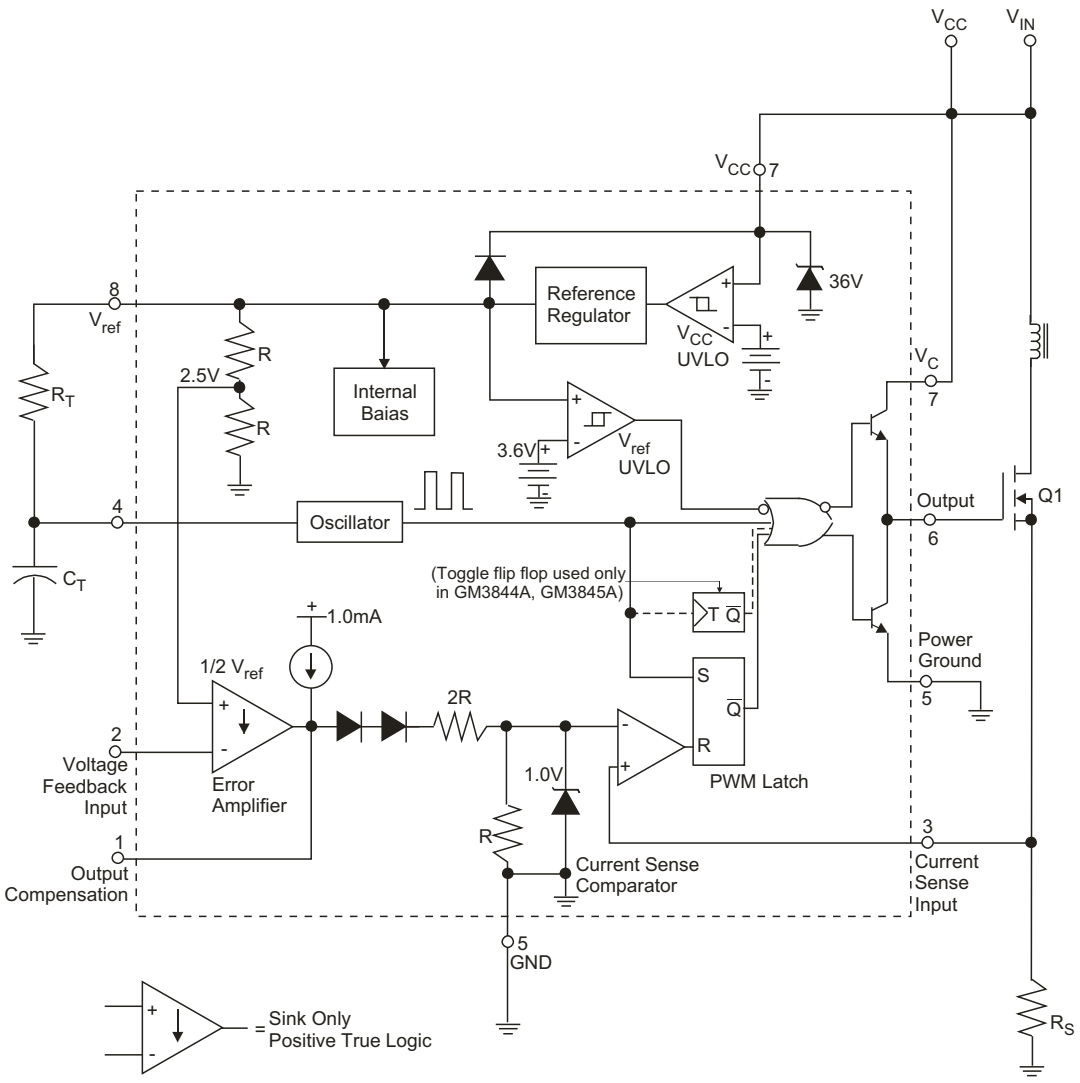
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage (low impedance source)	V_{CC}	30	V
Output Current, Source or Sink *	I_O	±1.0	A
Input Voltage (analog inputs pins 2)	V_I	- 0.3 to + 5.5	V
Maximum Power Dissipation (T_A= 25°C)	P_D	1.0	W
Error Amp Output Sink Current	$I_{SINK(E.A)}$	10	mA
Storage Temperature Range	T_{stg}	- 65 to + 150	°C
Lead Temperature (soldering 5 sec.)	T_L	260	°C

* Note: Maximum Package Power Dissipation Limits must be observed.

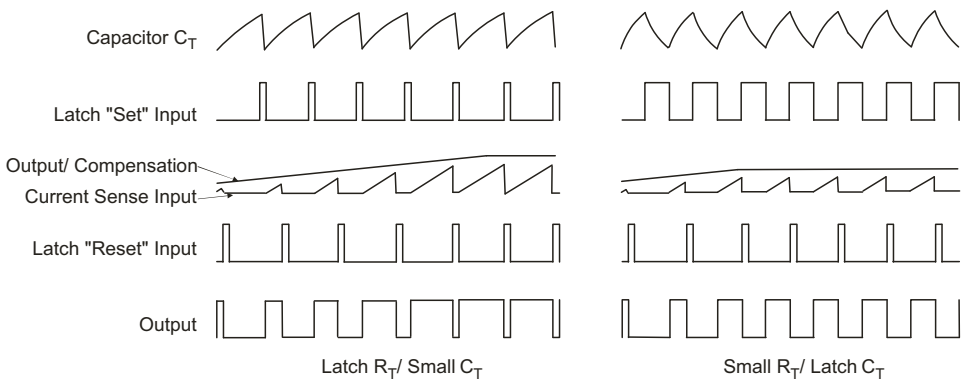
◆ PACKAGE PIN DESCRIPTION

PIN lead	FUNCTION	FUNCTION
1	COMP	This pin is Error Amplifier output and is made available for loop compensation.
2	V_{FB}	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/ C_T	Oscillator frequency and maximum Output cycle are programmed by connecting resistor R_T to V_{REF} and capacitor C_T to ground.
5	GND	This pin is the combined control circuitry and power ground.
6	Output	This output directly drives the gate of a power MOSFET. Peak current up to 1.0A are sourced and sunk by this pin.
7	V_{CC}	This pin is the positive supply of the control integrated circuit (IC)
8	V_{REF}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.

◆ REPRESENTATIVE BLOCK DIAGRAM



◆ TIMING DIAGRAM



◆ ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, *V_{CC}=15V, C_T=3.3nF, R_T=10k , unless otherwise specified)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Section						
Reference Output Voltage	V_{REF}	T_J= 25°C, I_{REF}= 1mA	4.9	5.0	5.1	V
Line Regulation	V_{REF}	12V ≤ V_{CC} ≤ 25V		6.0	20	mV
Load Regulation	V_{REF}	1mA ≤ I_{REF} ≤ 20mA		6.0	25	mV
Short Circuit Output Current	I_{SC}	T_A=25°C		-100	-180	mA
Oscillator Section						
Oscillation Frequency	f	T_J= 25°C	47	52	57	kHz
Frequency Change with Voltage	f/ V_{CC}	12V ≤ V_{CC} ≤ 25V		0.05	1.0	%
Oscillator Amplitude	$V_{(OSC)}$	(Peak to Peak)		1.6		V
Error Amplifier Section						
Input Bias Current	I_{BIAS}	V_{FB}= 3V		-0.1	-2	μA
Input Voltage	$V_{I(EA)}$	V_{PIN1}=2.5V	2.42	2.5	2.58	V
Open Loop Voltage Gain	A_{VOL}	2V ≤ V_O ≤ 4V	65	90		dB
Power Supply Rejection Ratio	PSRR	12V ≤ V_{CC} ≤ 25V	60	70		dB
Output Sink Current	I_{SINK}	V_{PIN2}=2.7V, V_{PIN1}=1.1V	2	7		mA
Output Source Current	I_{SOURCE}	V_{PIN2}=2.3V, V_{PIN1}=5V	-0.5	-1.0		mA
High Output Voltage	V_{OH}	V_{PIN2}=2.3V, R_L=15k to GND	5.0	6.0		V
Low Output Voltage	V_{OL}	V_{PIN2}=2.7V, R_L=15k to PIN8		0.8	1.1	V
Current Sense Section						
Current Sense Input Voltage Gain	G_V	(Note 1 and 2)	2.85	3.0	3.15	V/ V
Maximum Input Signal	$V_{I(MAX)}$	V_{PIN1}=5V (Note 1)	0.9	1.0	1.1	V
Supply Voltage Rejection	SVR	12V ≤ V_{CC} ≤ 25V (Note 1)		70		dB
Input Bias Current	I_{BIAS}	V_{PIN3}=3V		-3.0	-10	μA
Output Section						
Low Output Voltage	V_{OL}	I_{SINK}= 20mA		0.08	0.4	V
		I_{SINK}= 200mA		1.4	2.2	
High Output Voltage	V_{OH}	I_{SOURCE}= 20mA	13	13.5		V
		I_{SOURCE}= 200mA	12	13		
Rise Time	t_R	T_J= 25°C, C_L= 1nF(Note 3)		45	150	nS
Fall Time	t_F	T_J= 25°C, C_L= 1nF(Note 3)		35	150	nS
Undervoltage Lockout Section						
Start Threshold	$V_{TH(ST)}$	GM3842A, GM3844A	14.5	16.0	17.5	V
		GM3843A, GM3845A	7.8	8.4	9.0	
Minimum Operating Voltage (after tum ON)	$V_{OPR(MIN)}$	GM3842A, GM3844A	8.5	10	11.5	V
		GM3843A, GM3845A	7.0	7.6	8.2	

◆ ELECTRICAL CHARACTERISTICS (Continued)

(T_A = 0°C to 70°C, *V_{CC}=15V, C_T=3.3nF, R_T=10k , unless otherwise specified)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM Section						
Maximum Duty Cycle	$D_{(MAX)}$	GM3842A, GM3843A	95	97	100	%
		GM3844A, GM3845A	47	48	50	%
Minimum Duty Cycle	$D_{(MIN)}$				0	%
Total Standby Current						
Start-Up Current	I_{ST}	GM3842A/ 43A/ 44A/ 45A		0.17	0.3	mA
Operating Supply Current	$I_{CC(OPR)}$	V_{PIN3}= V_{PIN2}=0V		13	17	mA
Zener Voltage	V_Z	I_{CC}= 25mA	30	38		V

* Adjust V_{CC} above the Startup threshold before setting to 15 V.

Note1: Parameter measured at trip point of latch with V_{PIN2} = 0.

Note2: Gain defined as A= V_{PIN1} / V_{PIN3} ; 0 ≤ V_{PIN3} ≤ 0.8V

Note3: These parameters, although guaranteed, are not 100% tested in production

◆ TYPICAL PERFORMANCE CHARACTERISTICS

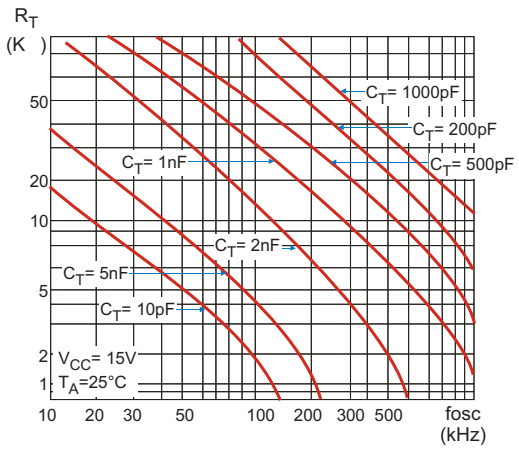


Figure 1. Timing Resistor vs. Oscillator Frequency

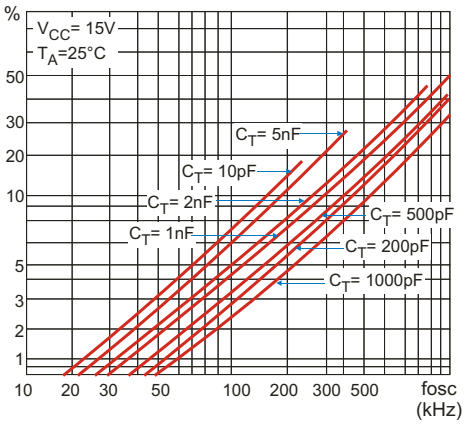


Figure 2. Output Dead-Time vs. Oscillator Frequency

◆ TYPICAL PERFORMANCE CHARACTERISTICS

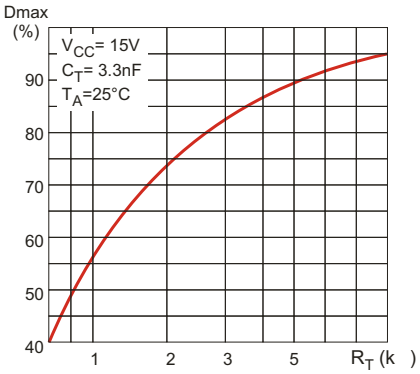


Figure 3. Maximum Output Duty Cycle vs. Timing Resistor (GM3842A/43A)

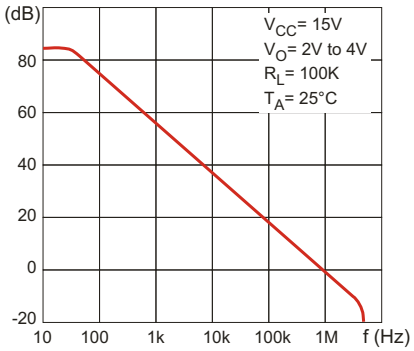


Figure 4. Error Amp Open-Loop Gain vs. Frequency

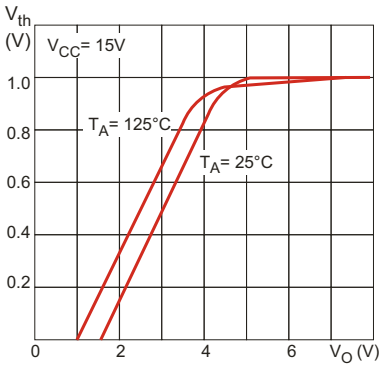


Figure 5. Current Sense Input Threshold vs. Error Amp Output Voltage

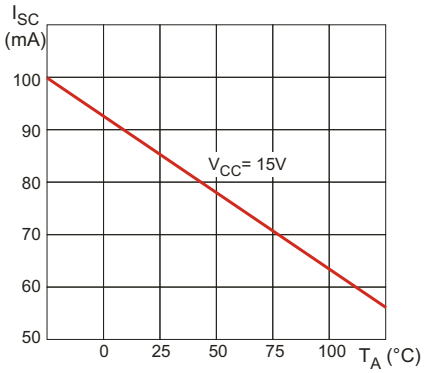


Figure 6. Reference Short Circuit Current vs. Temperature

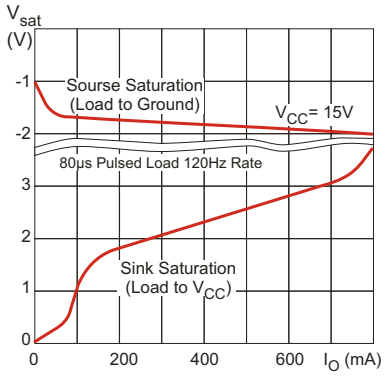


Figure 7. Output Saturation Voltage vs. Load Current T_A= 25°C

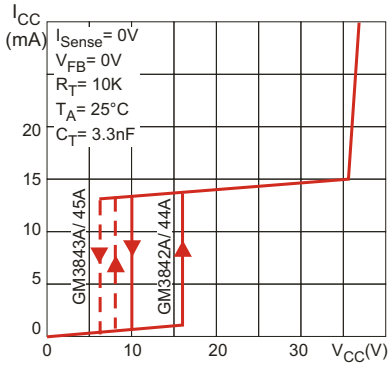


Figure 8. Supply Current vs. Supply Voltage

◆ OPERATING DESCRIPTION

GM3842A, GM3843A, GM3844A and GM3845A are high performance with fixed frequency, current mode controllers. They are designed for off-ine and DC-to-DC converter applications offering great versatility with minimal external components. A representative block diagram is shown on page 4.

Oscillator

The oscillator frequency is determined by the values of the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the output to be in a low state, thus producing a controlled amount of Figure 2 show R_T versus oscillator frequency and Figure 2, Output deadtime versus frequency, both for given values of C_T output deadtime.

Note that different values of R_T and C_T will give the same oscillator frequency, but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated. These interned circuit vefinements minimizes refinements of oscillator frequency and maximum output duty cycle. In many noise sensitive applications, it may be desirable to frequency-lock the converter to an external system clock. This can be accmplished by applying a clock signal to the circuit shown in Figure 9. For best locking results, set the free-unning oscillator frequency to about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 10. You can get very accurate output duty cycle clamping by tweaking the clock waveform.

Error Amplifier

GM384XA series has a fully compensated error amplifier with access to both the inverting input and output, and providing DC voltage gain of 90 dB (typical). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is -2.0 µA, which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amplifier Output (Pin 1) allows external loop compensation. The output voltage is offset by the two diode drops (≈ 1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This assures that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This happens when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 11, 12). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0(1.0V) + 1.4V}{0.5mA} = 8800$$

Current Sense Comparator and PWM Latch

GM384XA series operates as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin1). The error signal controls the peak inductor current cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration assures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(PIN1)} - 1.4V}{3\,R_S}$$

When the power supply output is overloaded or if output voltage sensing is lost, the chip operation is not normal. In these situations, the Current Sense Comparator threshold will be internally clamped to 1.0 V and the maximum peak switch current is:

$$I_{pk(mak)} = \frac{1.0V}{R_S}$$

When designing a high power switching regulator, it becomes desirable to reduce the internal clamp voltage in order, to keep a reasonable level of power dissipation of R_S. Adjusting the internal clamp voltage is very simple, as shown in Figure 11. The two external diodes compensate the internal diodes so you get a constant clamp voltage over temperature. Avoid too much reduction of the $I_{pk(max)}$ clamp voltage, or you will get noise pickup and erratic results.

A narrow spike on the leading edge of the current waveform often occurs and can cause the power supply instability when the output load is light. This spike is caused by power transformer interwinding capacitance and output rectifier recovery time. You can eliminate this problem by adding an RC filter on the Current Sense Input, with a time constant similar to the spike's duration; see Figure 16.

Undervoltage Lockout

Two UVLO comparators in GM384XA series assure that the chips are fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) have separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their thresholds are reached. The V_{CC} comparator's upper and lower thresholds are 16 V/10 V for GM3842A and GM3844A, and 8.4V/7.6V for GM3843A and GM3845A.

The V_{ref} comparator's upper and lower thresholds are 3.6V/3.4 V. The large hysteresis and low startup current of the GM3842A and GM3844A makes them ideal for off-line converter applications where efficient bootstrap startup is required.

GM3843A and GM3845A are intended for lower voltage DC-to-DC converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for GM3842A and GM3844A is 11V; for GM3843A and GM3845A it is 8.2V.

Output

GM384XA series has a single totem pole output stage that was designed for direct drive of power MOSFETs. It provides up to ±1.0 A peak drive current and has a typical rise/ fall time of 50 ns with a 1.0 nF load. Additional internal circuitry keeps the output in a sinking mode whenever a UVLO is active. This eliminates the need for an external pull-down resistor.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the GM384XA series. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and it can provide more than 20mA for powering additional control system circuitry.

Design Considerations

Do not make your converter to use wire-wrap or plug-in prototype boards. High-frequency circuit layout techniques must be observed to prevent pulsewidth jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. You can improve noice immunity by lowering circuit impedances at these points. The PCB layout should have a ground plane with low-current signal and high-current switch and output grounds returning on separate paths to the input filter capacitor. Ceramic bypass capacitors (0.1 µF) connected directly to V_{CC}, V_C, and V_{ref} may be required, depending upon circuit layout, to provide a low impedance path for filtering high frequency noise. All high-current loops should be as short as possible and use heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be placed as close as possible to the GM384XA, and as far as possible from the power switch and other noise- generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulators closed–loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 9.A shows the phenomenon graphically. At t_0, switch conduction begins and causes causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input
reaches the threshold established by the control voltage.

This causes the switch to turn off and the current to decay at a slope of m_2 until the next oscillator cycle. The unstable condition can be shown if a pertubation is added to the control voltage, and resulting in a small I (dashed line). With a fixed oscillator period, the current decay time is reduced and the minimum current at switch turn–on (t_2) is increased by I + I m_2/m_1. The minimum current at next cycle (t_3) decreases to (I + I m_2/m_1) (m_2/m_1). This pertubation is multiplied by $m_2.m_1$ on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn–on. Several oscillator cycles may be required before the inductor current reaches zero, which caused causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Figure 9.B shows that by adding an artificial ramp, that is synchronized with the PWM clock to the control voltage, the I pertubation will decrease to zero on succeeding cycles. This compensation ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage yielding true current mode operation. The compensating ramp can be

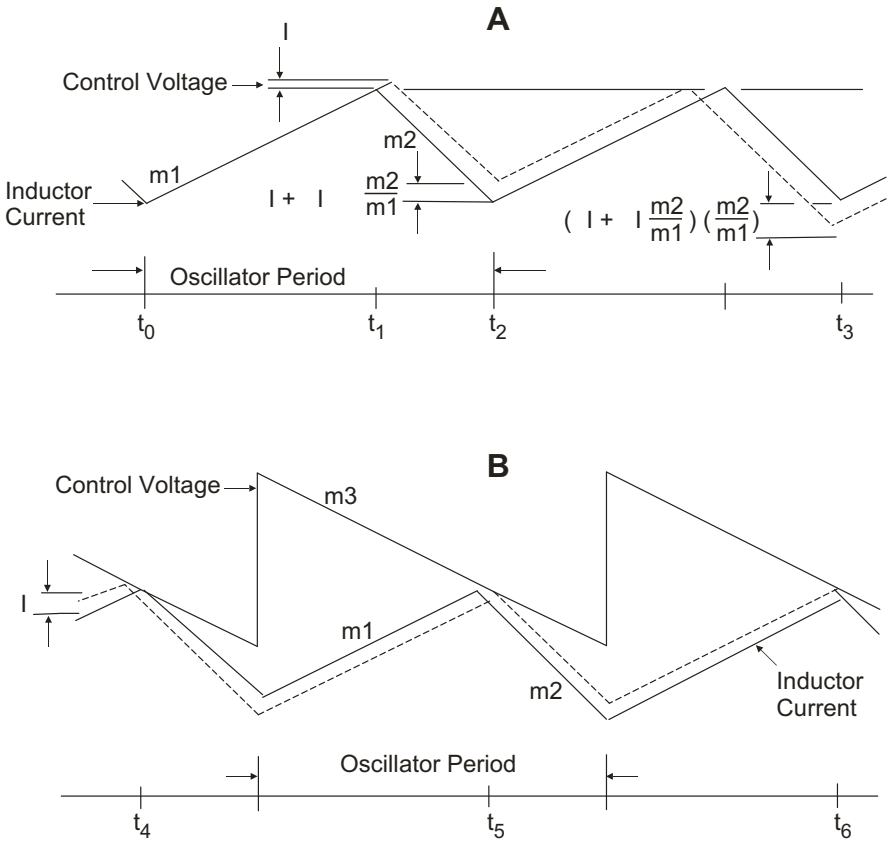
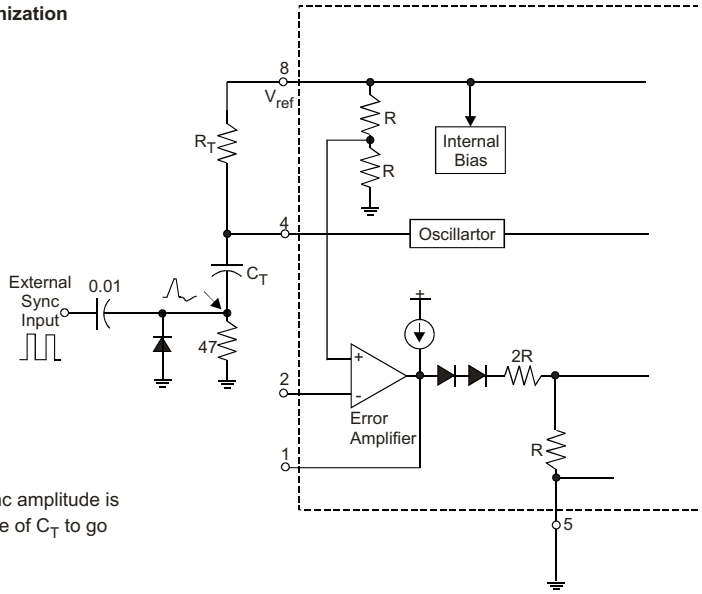


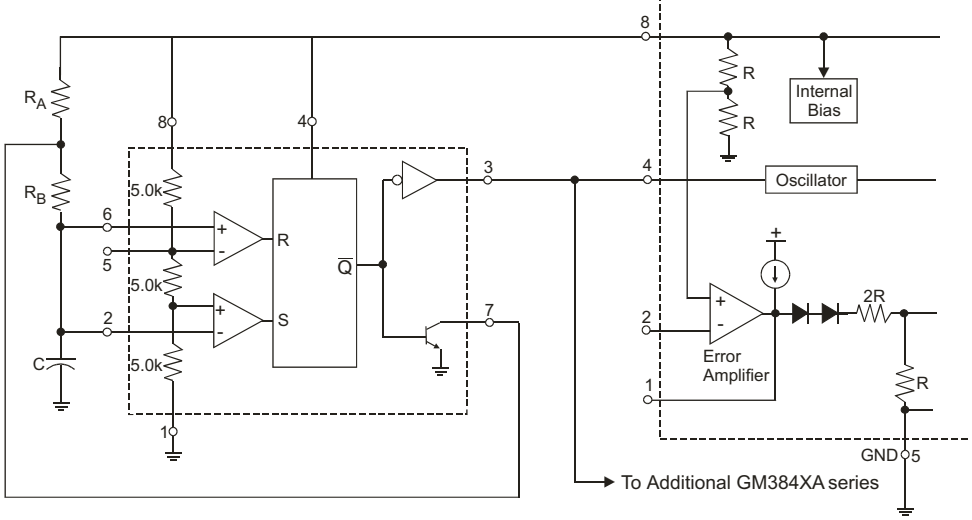
Figure 9. Continuous Current Waveforms

Figure 10. External Clock Synchronization



* The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 11. External DUTY CYCLE CLAMP and multi-unit synchronization



$$f = \frac{1.44}{(R_A + 2R_B)\,C} \qquad Dmax \frac{R_B}{R_A + 2R_B}$$

Figure 12. Adjustable reduction of clamp level

$$V_{clamp}=\frac{1.67}{(\frac{R2}{R1}+1)}+0.33X10\text{-}3\,(\frac{R1+R2}{R1+R2})$$

$$I_{PK(max)}=\frac{V_{clamp}}{RS}$$

where: $0 \le V_{clamp} \le 1.0V$

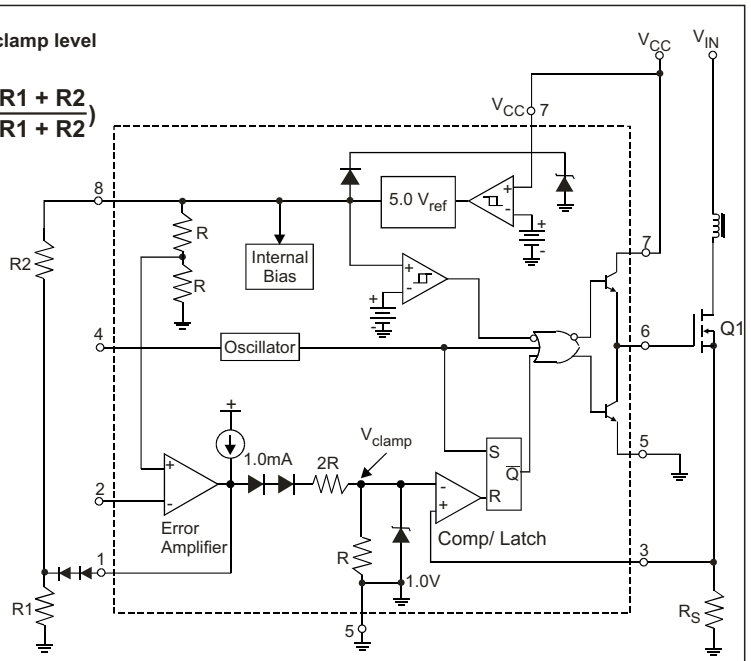
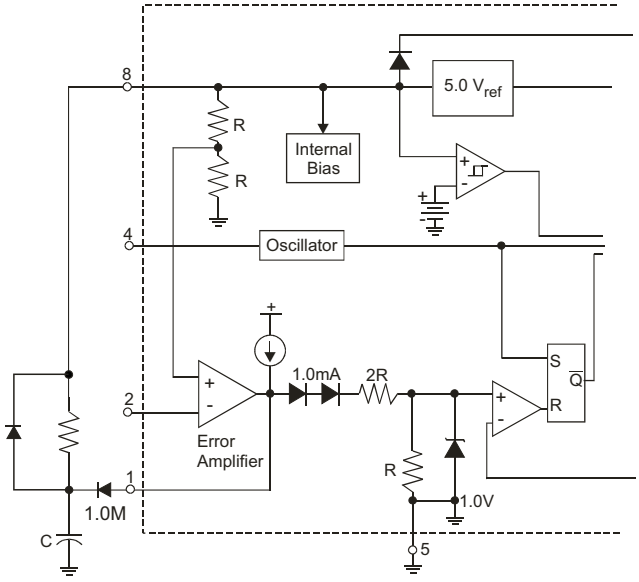


Figure 13. Soft-start circuit



$t_{soft\text{-}start} \approx 3600C$ in μF

Figure 14. Adjustable buffered reduction of clamp level with soft-start

$$V_{clamp} = \frac{1.67}{\left(\frac{R2}{R1} + 1\right)}$$

$$I_{PK(max)} = \frac{V_{clamp}}{RS}$$

where: $0 \leq V_{clamp} \leq 1.0V$

$$t_{softstart} = -\ln\left[1 - \frac{V_C}{3V_{clamp}}\right]$$

$$C\,\frac{R1 + R2}{R1 + R2}$$

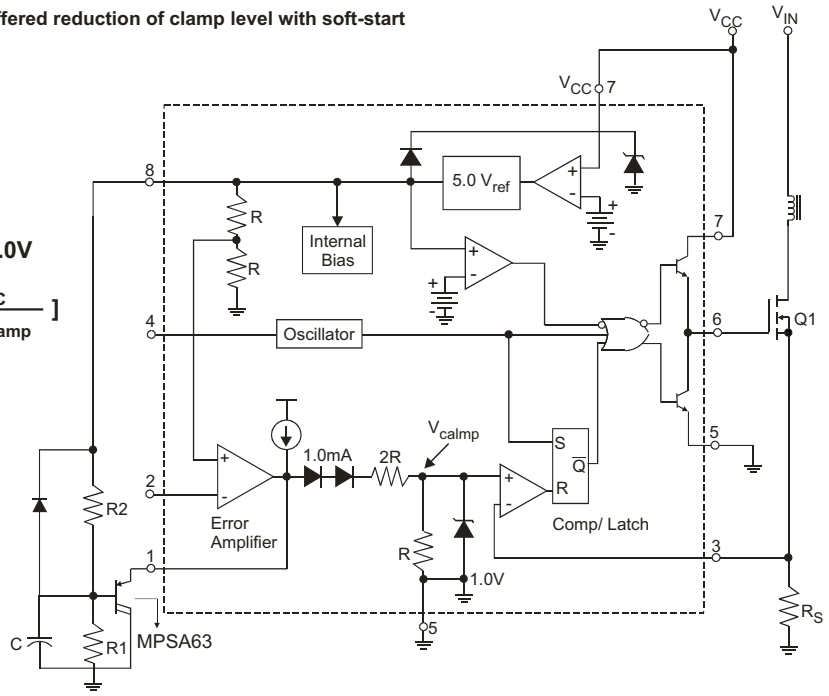
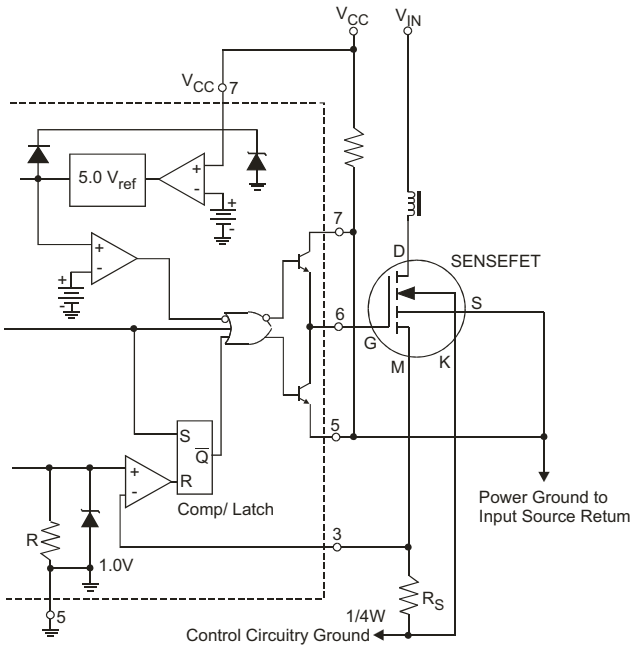


Figure 15. Current sensing power mosfet

$$V_{PIN\ 5} = \frac{R_S\, I_{PK}\, R_{DS(on)}}{R_{DS(on)} + R_S}$$

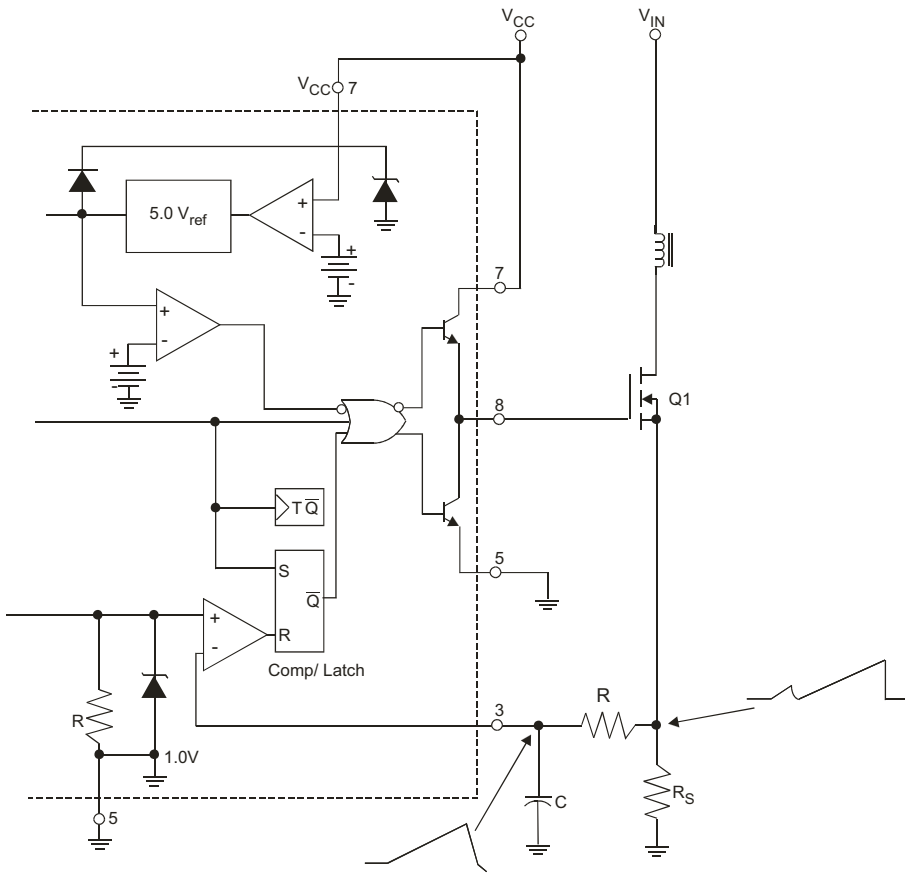
If= SENSEFET= MTP10N10M
R_S= 200

Then : $V_{PIN\ 5}$= 0.075 I_{PK}



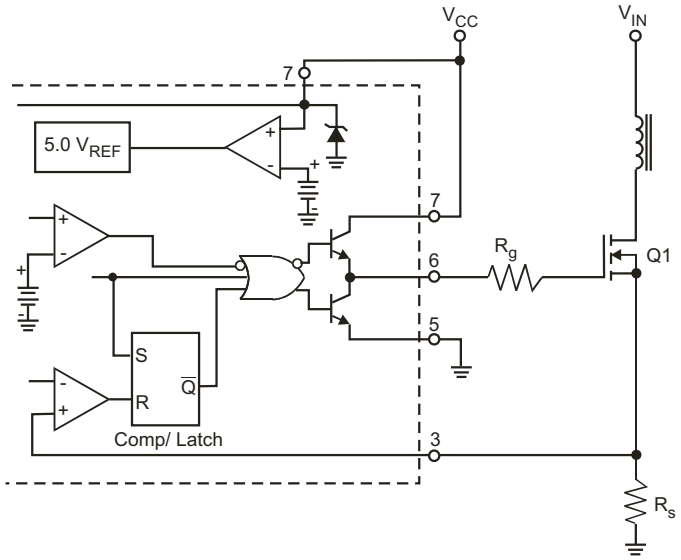
For proper operation during over current conditions, a reduction of the Ipk(max) clamp level must be implemented. Refer to Figures 11 and 12.

Figure 16. current wavefrom spike suppression



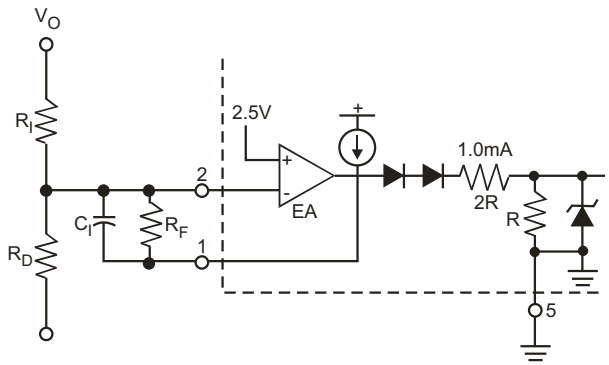
* The addition of the R_C filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 17. MOSFET Parasitic Oscillations



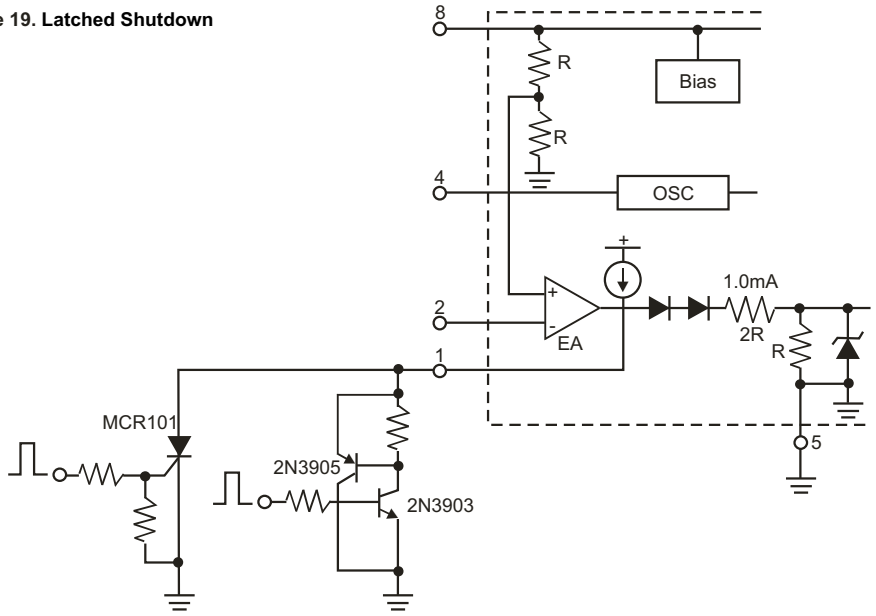
Series gate resistor Rg will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Figure 18. Isolated MOSFET Drive



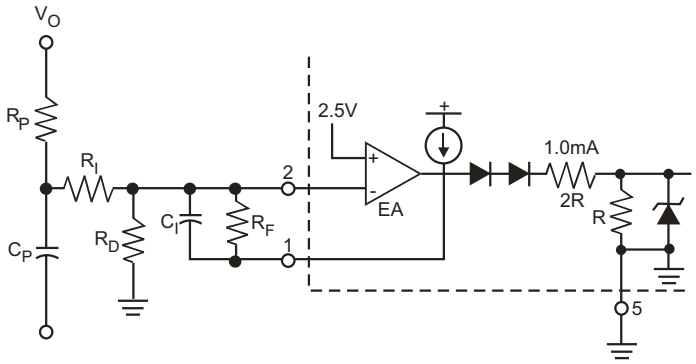
Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.

Figure 19. Latched Shutdown



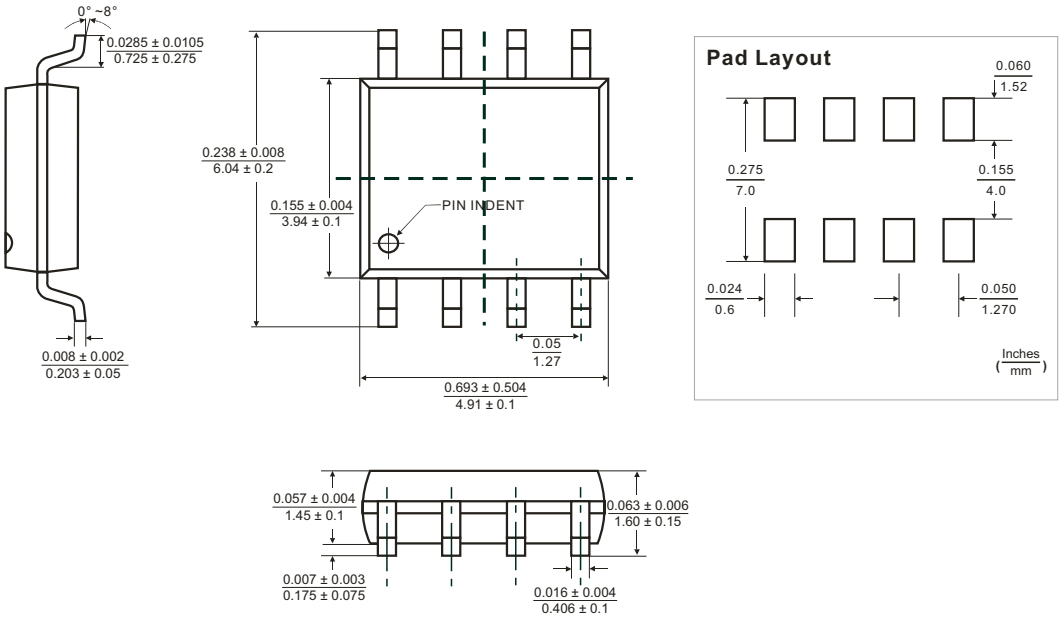
The MCR101 SCR must be selected for a holding of less than 0.5 mA at T_A(min).
The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure Error Amplifier Compensation

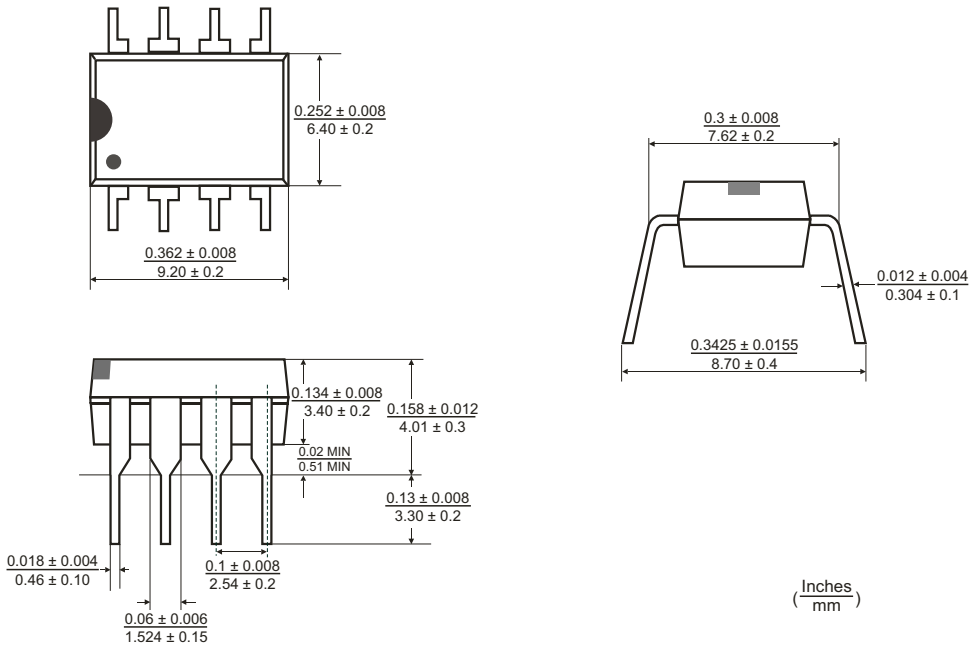


Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

◆ SOP-8 PACKAGE OUTLINE DIMENSIONS



◆ DIP-8 PACKAGE OUTLINE DIMENSIONS



◆ ORDERING NUMBER