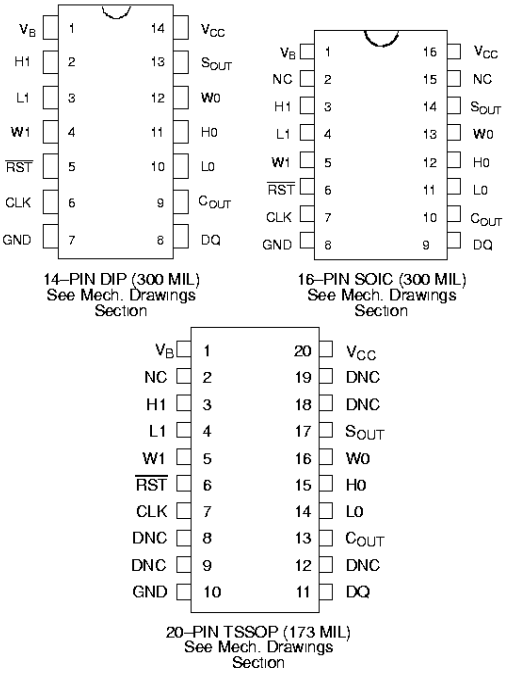
DALLAS SEMICONDUCTOR

DS1867
Dual Digital Potentiometer with EEPROM

FEATURES

- Nonvolatile version of the popular DS1267
- Low power consumption, quiet, pumpless design
- Operates from single 5V or ±5V supplies
- Two digitally controlled, 256–position potentiometers
- Wiper position is maintained in the absence of power
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide increased total resistance
- 16–pin SOIC and 20–pin TSSOP for surface mount applications
- Standard resistance values:
  - DS1867–10 ~ 10KΩ
  - DS1867–50 ~ 50KΩ
  - DS1867–100 ~ 100KΩ
- Temperature:
  - Commercial: 0°C to 70°C
  - Industrial: –40°C to +85°C

PIN ASSIGNMENT



14–PIN DIP (300 MIL) See Mech. Drawings Section

16–PIN SOIC (300 MIL) See Mech. Drawings Section

20–PIN TSSOP (173 MIL) See Mech. Drawings Section

DESCRIPTION

The DS1867 is the nonvolatile version of the popular DS1267 Dual Digital Potentiometer. The DS1867 consists of two digitally controlled potentiometers having 256–position wiper settings. Wiper position is maintained in the absence of power through the use of EEPROM memory cell arrays. Communication and control of the device is accomplished over a 3–wire serial port which allows reads and writes of the wiper position. Both potentiometers can be stacked for increased total resistance with the same resolution. For multiple device–single processor environments, the DS1867 can be cascaded for control over a single 3–wire bus. The DS1867 is offered in three standard resistance values and commercial and industrial temperature versions.

PIN DESCRIPTION

L0, L1	–	Low End of Resistor
H0, H1	–	High End of Resistor
W1, W2	–	Wiper End of Resistor
V_B	–	Substrate Bias
S_{OUT}	–	Wiper for Stacked Configuration
$\overline{RST}$	–	Serial Port Reset Input
DQ	–	Serial Port Data Input
CLK	–	Serial Port Clock Input
C_{OUT}	–	Cascade Serial Port Output
V_{CC}	–	+5 Volt Supply Input
GND	–	Ground
NC	–	No Internal Connection
DNC	–	Do Not Connect

OPERATION

The DS1867 contains two 256–position potentiometers whose wiper positions are set by an 8–bit value. These two 8–bit values are written to a 17–bit I/O shift register which is used to store wiper position and the stack select bit when the device is powered. An additional memory area, the shadow memory, stores the 17–bit I/O shift register during a power–down sequence which provides for wiper nonvolatility. A block diagram of the DS1867 is presented in Figure 1.

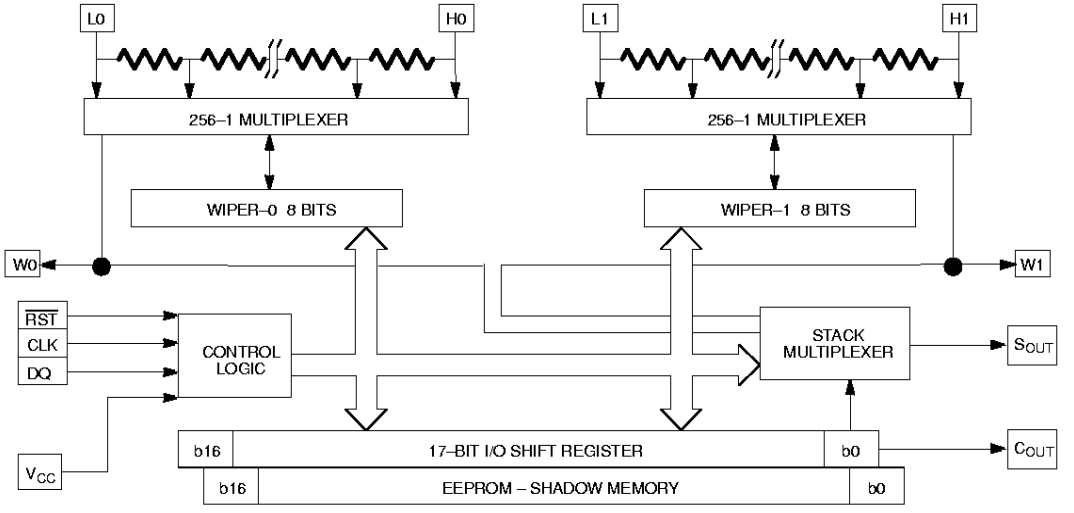
Communication and control of the DS1867 is accomplished through a 3–wire serial port interface that drives an internal control logic unit. The 3–wire serial interface consists of the three input signals: $\overline{RST}$, CLK, and DQ.

The $\overline{RST}$ control signal is used to enable 3–wire serial port operation of the device. The $\overline{RST}$ signal is an active high input and is required to begin any communication to the DS1867. The CLK signal input is used to provide timing synchronization for data input and output. The DQ signal line is used to transmit potentiometer wiper settings and the stack select bit configuration to the 17–bit I/O shift register of the DS1867.

Figure 2(a) presents the 3–wire serial port protocol. As shown, the 3–wire port is inactive when the $\overline{RST}$ signal input is low. Communication with the DS1867 requires the transition of the $\overline{RST}$ input from a low state to a high state. Once the 3–wire port has been activated, data is latched into the part on the low to high transition of the CLK signal input. Three–wire serial timing requirements are provided in the timing diagrams of Figure 2(b) and (c).

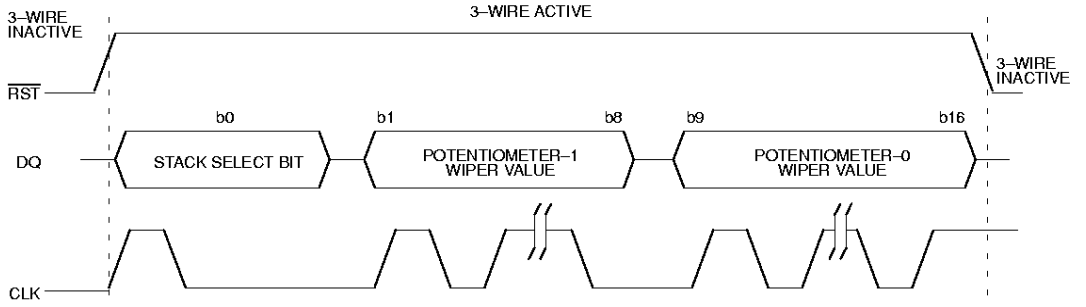
Data written to the DS1867 over the 3–wire serial interface is stored in the 17–bit I/O shift register (see Figure 3). The 17–bit I/O shift register contains both 8–bit potentiometer wiper position values and the stack select bit. The composition of the I/O shift register is presented in Figure 3. Bit 0 of the I/O shift register contains the stack select bit. This bit will be discussed in the section entitled Stacked Configuration. Bits 1 through 8 of the I/O shift register contain the potentiometer–1 wiper position value. Bit 1 will contain the MSB of the wiper setting for potentiometer–1 and bit 8 the LSB for the wiper setting. Bits 9 through 16 of the I/O shift register contain the value of the potentiometer–0 wiper position with the MSB for the wiper position occupying bit 9 and the LSB bit–16.

DS1867 BLOCK DIAGRAM Figure 1

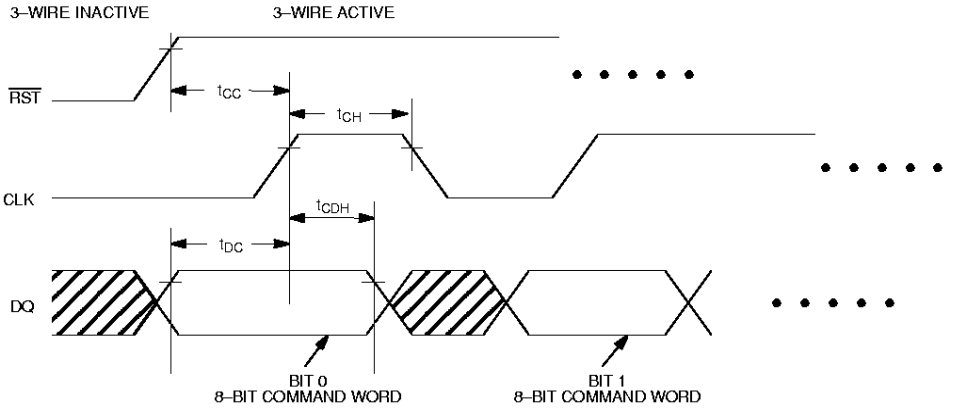


TIMING DIAGRAMS Figure 2

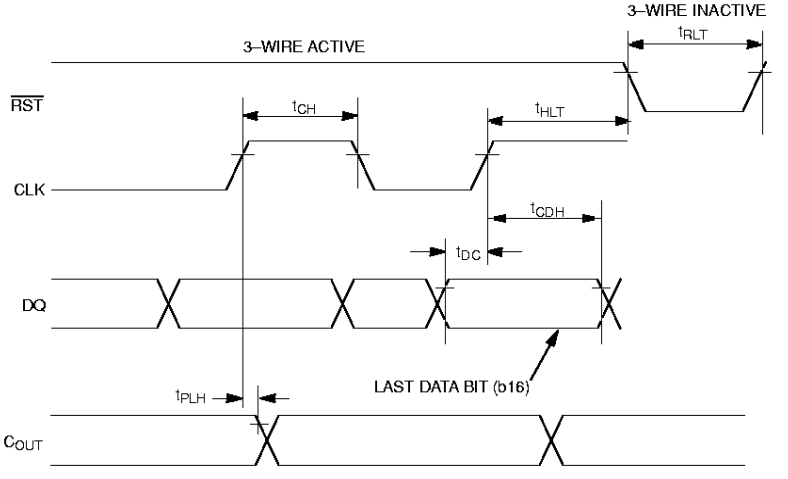
(a) 3–Wire Serial Interface General Overview



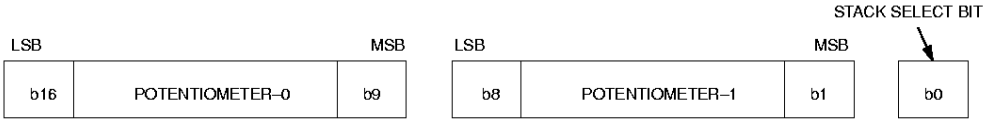
(b) Start of Communication Transaction



(c) End of Communication Transaction



I/O SHIFT REGISTER Figure 3



17–BIT I/O SHIFT REGISTER

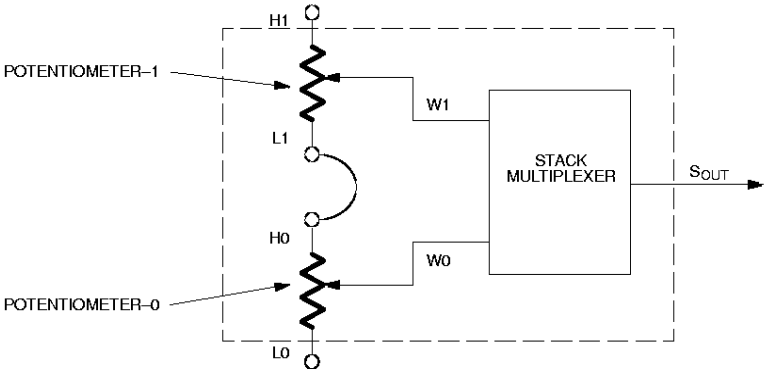
Transmission of data always begins with the stack select bit followed by the potentiometer–1 wiper position value and lastly the potentiometer–0 wiper position value (see Figure 2(a)).

When wiper position data is to be written to the DS1867, 17–bits (or some integer multiple) of data should always be transmitted. Transactions which do not send a complete 17–bits (or multiple) will leave the register incomplete and possibly an error in desired wiper position. After a communication transaction has been completed the $\overline{RST}$ signal input should be taken to a low state to prevent any inadvertent changes to the device shift register. Once $\overline{RST}$ has reached a low state, the contents of the I/O shift register are loaded into the respective multiplexers for setting wiper position. A new wiper position will only engage pending a $\overline{RST}$ transition to the low state. The wiper position for the high–end terminals H0 and H1 will have data values FF (hex), while the low–end terminals will have data values 00 (hex).

STACKED CONFIGURATION

The potentiometers of the DS1867 can be connected in series as shown in Figure 4. This is referred to as the stacked configuration and allows the user to double the total end–to–end resistance of the part. The resolution of the combined potentiometers will remain the same as a single potentiometer but with a total of 512 wiper positions available. Device resolution is defined as $R_{TOT}/256$ (per potentiometer); where R_{TOT} is equal to the device resistance value. The wiper output for the combined stacked potentiometer will be taken at the Sout pin, which is the multiplexed output of the wiper of potentiometer–0 (W0) or potentiometer–1 (W1). The potentiometer wiper selected at the Sout output is governed by the setting of the stack select bit (bit–0) of the 17–bit I/O shift register. If the stack select bit has value 0, the multiplexed output , Sout, will be that of the potentiometer–0 wiper. If the stack select bit has value 1, the multiplexed output, Sout, will be that of the potentiometer–1 wiper.

STACKED CONFIGURATION Figure 4



CASCADE OPERATION

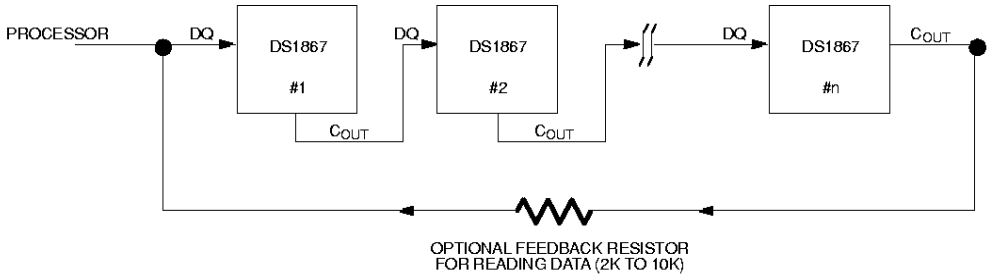
A feature of the DS1867 is the ability to control multiple devices from a single processor. Multiple DS1867s can be linked or daisy chained as shown in Figure 5. As a data bit is entered into the I/O shift register of the DS1867 it will appear at the Cout output after a maximum delay of 70 nanoseconds.

The Cout output of the DS1867 can be used to drive the DQ input of another DS1867. When connecting multiple devices, the total number of bits sent is always 17 times the number of DS1867s in the daisy chain.

An optional feedback resistor can be placed between the Cout terminal of the last device and the DQ input of the first DS1867, thus allowing the controlling processor to read, as well as, write data or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 2K to 10K ohms.

When reading data via the Cout pin and isolation resistor, the DQ line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 17 is present on the Cout pin, which is fed back to the input DQ pin through the isolation resistor. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on Cout and DQ of the next device. After 17 bits (or 17 times the number of DS1867s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded into the wiper–0, wiper–1, and stack select bit I/O register.

CASCADING MULTIPLE DEVICES Figure 5



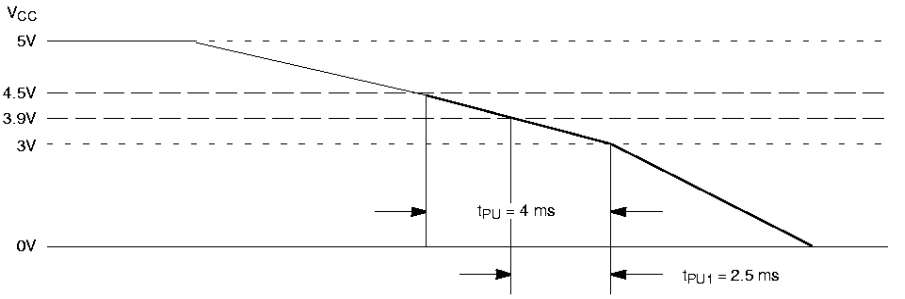
NONVOLATILE WIPER SETTINGS

The DS1867 maintains the position of the wiper in the absence of power. This feature is provided through the use of EEPROM type memory cell arrays. During normal operation, the position of the wiper is determined by the device multiplexers and stored in the shadow memory (EEPROM). The manner in which an update occurs has been optimized for reliability, durability, and performance. Additionally, the update operation is totally transparent to the user.

When power is applied to the DS1867, wiper settings will be the last recorded in the EEPROM memory cells or shadow memory before the last power–down. Changes to the EEPROM memory cells occur during a predefined power–down sequence. If the DS1867 detects a voltage transistion to 4.5 volts or less, on the power supply input, the part initiates an automatic wiper storage sequence. This storage sequence will save in EEPROM memory the contents of the I/O shift register before a total power–shutdown; provided specific power–down timing requirements are met. The minimum total power down time is specified at 4 milliseconds. Power–down timing requirements on V_{CC} are shown in Figure 6.

The EEPROM memory cells are specified to accept greater than 50,000 writes before a wear–out condition. If the EEPROM memory cells do reach a wear–out condition, the DS1867 will still function properly while power is applied. A minimum time of 4 ms between 4.5V and 3V is required to perform the proper position storage of the wiper.

POWER–DOWN EEPROM TIMING REQUIREMENTS Figure 6



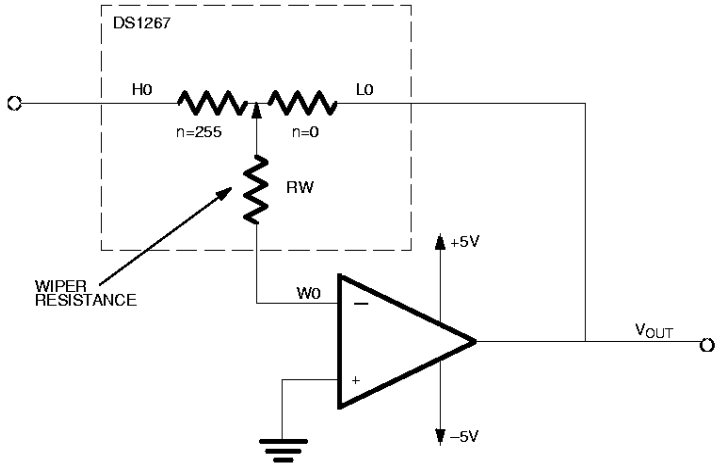
TYPICAL APPLICATION CONFIGURATIONS

Figures 7 and 8 show two typical application configurations for the DS1867. By connecting the wiper terminal of the part to a high impedance load, the effects of the wiper resistance is minimized, since the wiper resistance can vary from 400 to 1000 ohms depending on wiper voltage. Figure 7 presents the device connected in an inverting variblegain amplifier. The gain of the circuit on Figure 7 is given by the following equation:

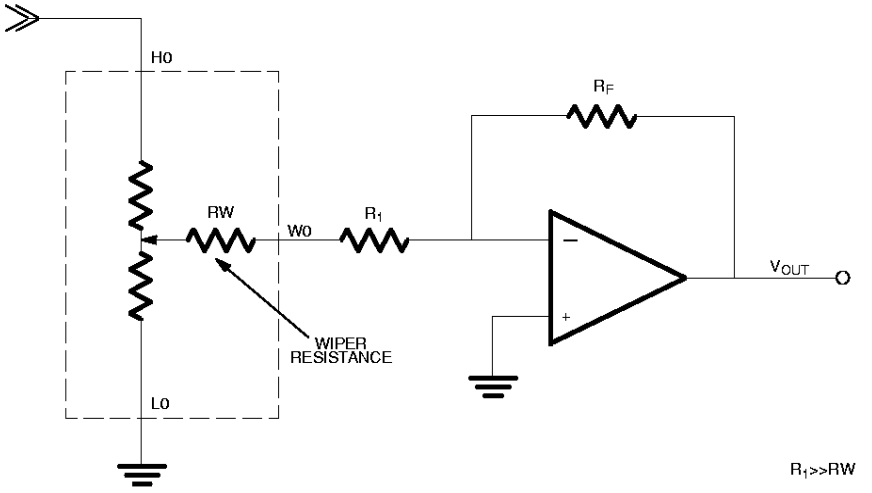
Av = –n/(255–n); where n = 0 to 255

Figure8 shows the device operaing in a fixed gain attenuator where the potentiometer is used to attenuate an incoming signal. Note the resistance R1 is chosen to be much greater than the wiper resistance to minimize its effect on circuit gain.

INVERTING VARIABLE GAIN AMPLIFIER Figure 7



FIXED GAIN ATTENUATOR Figure 8



ABSOLUTE AND RELATIVE LINEARITY

Absolute linearity is defined as the difference between the actual measured output voltage and the expected output voltage. Figure 9 presents the test circuit used to measure absolute linearity. Absolute linearity is given in terms of a minimum increment or expected output when the wiper position is moved one position. In the case of the test circuit, a minimum increment (MI) would equal 10/512 volts. The equation for absolute linearity is given in equation (1).

Eq: (1) Absolute Linearity

$$AL = \{Vo(actual) - Vo(expected)\}/MI$$

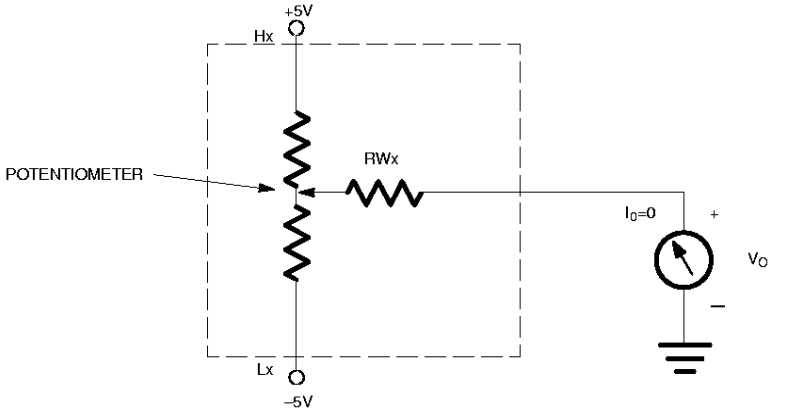
Relative Linearity is a measure of error between two adjacent wiper position points and is given in terms of MI by equation (2).

Eq: (2) Relative Linearity

$$RL = \{Vo(n+1) - Vo(n)\}/MI$$

Figure 10 is a plot of absolute linearity and relative linearity versus wiper position for the DS1867 at 25°C. The specification for absolute linearity of the DS1867 is ±0.75 MI typical. The specification for relative linearity of the DS1867 is ±0.30 MI typical.

LINEARITY MEASUREMENT CONFIGURATION Figure 9



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_B=GND)	–1.0V to +5.5V
Voltage on Resistor Pins when V_B=–5.5V	–5.5V to +5.5V
Operating Temperature	0°C to 70°C commercial; –40°C to +85°C industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5		5.5	V	
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	–0.5		+0.8	V	1
Substrate Bias	V_B	–5.5		GND	V	
Resistor Inputs	L, H, W	V_B		V_{CC}+0.5	V	2

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		250	900	µA	
Input Leakage	I_{LI}	–1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Logic 1 Output @ 2.4 Volts	I_{OH}	–1.0			mA	8
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	8
Standby Current	I_{STBY}		250		µA	
Power–Down Time	t_{PU} t_{PU1}	4 2.5			ms ms	9 10
Power Trip Point		3.9	4.2	4.5	V	
Recovery Time	t_{REC}	2	5	10	ms	11, 14

ANALOG RESISTOR CHARACTERISTICS

(–40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End–to–End Resistor Tolerance		–20		+20	%	
Absolute Linearity			±0.75		LSB	4
Relative Linearity			±0.30		LSB	5
–3 dB Cutoff Frequency	f_{CUTOFF}				Hz	7
Noise Figure			120		dB/(Hz)1/2	
Temperature Coefficient			+800		ppm/°C	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3
Output Capacitance	C_{OUT}			7	pF	3

AC ELECTRICAL CHARACTERISTICS

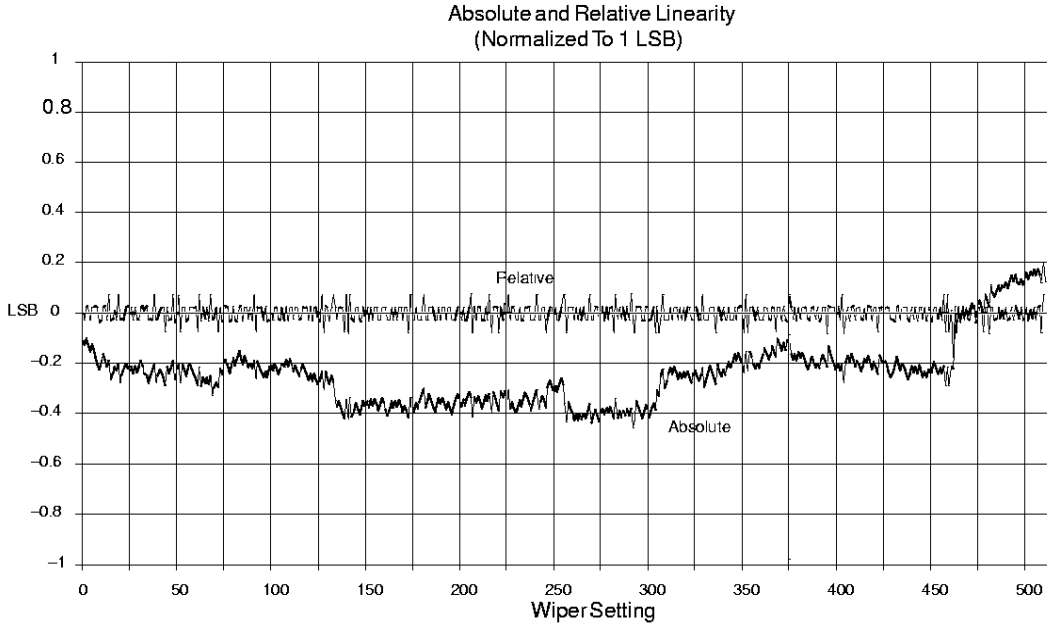
(–40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	15
Width of CLK Pulse	t_{CH}	50			ns	15
Data Setup Time	t_{DC}	30			ns	15
Data Hold Time	t_{CDH}	10			ns	15
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			70	ns	13, 15
Propagation Delay Time High to Low Level Clock to Output	t_{PHL}			70	ns	13, 15
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	15
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	15
CLK Rise Time	t_{CR}			50	ns	15
$\overline{RST}$ Inactive Time	t_{RLT}	200			ns	15

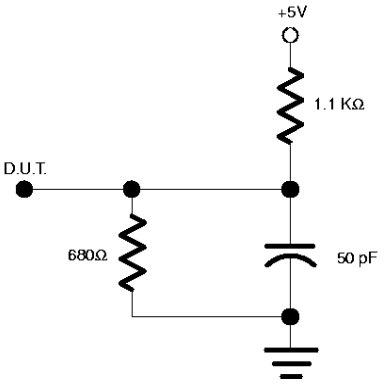
NOTES:

1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed the substrate bias voltage, V_B, in the negative direction.
3. Capacitance values apply at 25°C.
4. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position. Test limits for absolute linearity are ±1.6 LSB.
5. Relative linearity is used to determine the change in voltage between successive tap positions. Test limits for relative linearity are ±0.5 LSB.
6. Typical values are for t_A=25°C and nominal supply voltage.
7. –3 dB cuttof frequency characteristics for the DS1867 depend on potentiometer total resistance: DS1867–010; 1 MHz, DS1867–050; 200 KHz, DS1867–100; 100 KHz.
8. C_{OUT} is active regardless of the state of $\overline{RST}$.
9. Power–down time is specified at a minimum of 4 ms. It is the time required for the DS1867 to guarantee wiper position storage as V_{CC} moves from 4.5V to 3.0V.
10. This is the time from power trip point min (3.9V) to 3.0V to guarantee wiper storage.
11. t_{REC} is the time required before the DS1867 stored wiper position becomes valid on power–up.
12. Power trip points reference required voltage necessary for DS1867 to restore the stored wiper position setting.
13. See Figure 11.
14. During power up the wiper position will be set at 80H.
15. See Figure 2.

ABSOLUTE AND RELATIVE LINEARITY Figure 10



DIGITAL OUTPUT LOAD SCHEMATIC Figure 11



TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 12