

# 19MHz Rad Hard 40V Quad Rail-to-Rail Input-Output, Low-Power Operational Amplifiers

## ISL70444SEH

The ISL70444SEH features four low-power amplifiers optimized to provide maximum dynamic range. These op amps feature a unique combination of rail to rail operation on the input and output as well as a slew enhanced front end that provides ultra fast slew rates positively proportional to a given step size; thereby increasing accuracy under transient conditions, whether it's periodic or momentary. They also offer low power, low offset voltage, and low temperature drift, making it ideal for applications requiring both high DC accuracy and AC performance. With  $<5\mu\text{s}$  recovery for Single Event Transients (SET) ( $\text{LET}_{\text{TH}} = 86.4\text{MeV} \cdot \text{cm}^2/\text{mg}$ ), the number of filtering components needed is drastically reduced. The ISL70444SEH is also immune to Single Event Latch-up as it is fabricated in Intersil's Proprietary PR40 Silicon On Insulator (SOI) process.

They are designed to operate over a single supply range of 2.7V to 40V or a split supply voltage range of  $\pm 1.35\text{V}$  to  $\pm 20\text{V}$ . Applications for these amplifiers include precision instrumentation, data acquisition, precision power supply controls, and process controls.

The ISL70444SEH is available in a 14 Ld Hermetic Ceramic Flatpack and die forms that operate over the temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

## Related Literature

- ISL70444SEH Evaluation Board User's Guide [AN1824](#)
- ISL70444SEH Single Event Effects Report [AN1838](#)
- ISL70444SEH SMD [5962-13214](#)
- ISL70444SEH [Radiation Test Report](#)

## Features

- Electrically screened to DLA SMD# [5962-13214](#)
- Acceptance tested to 50krad(Si) (LDR) wafer-by-wafer
- $<5\mu\text{s}$  recovery from SEE ( $\text{LET}_{\text{TH}} = 86.4\text{MeV} \cdot \text{cm}^2/\text{mg}$ )
- Unity gain stable
- Rail-to-rail input and output
- Wide gain-bandwidth product ..... 19MHz
- Wide single and dual supply range. .... 2.7V to 40V Max
- Low input offset voltage ..... 300 $\mu\text{V}$
- Low current consumption (per amplifier) ..... 1.1mA, Typ
- No phase reversal with input overdrive
- Slew rate
  - Large signal ..... 60V/ $\mu\text{s}$
- Operating temperature range. ....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Radiation tolerance
  - High dose rate (50-300rad(Si)/s). .... 300krad(Si)
  - Low dose rate (0.01rad(Si)/s) ..... 100krad(Si)\*
  - SEL/SEB  $\text{LET}_{\text{TH}}$  .....  $86.4\text{MeV} \cdot \text{cm}^2/\text{mg}$

\* Product capability established by initial characterization.

## Applications

- Precision instruments
- Active filter blocks
- Data acquisition
- Power supply control
- Process control

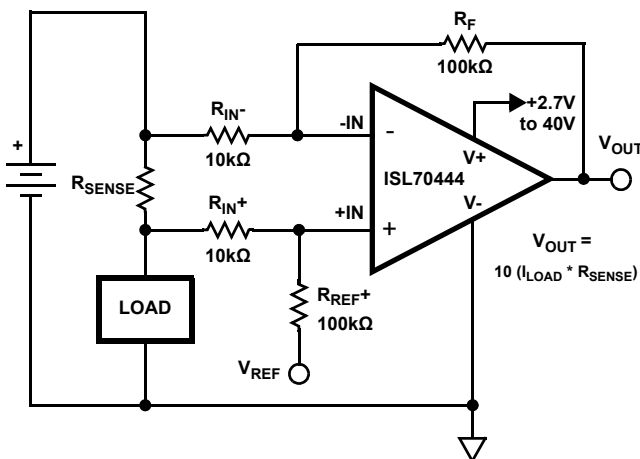


FIGURE 1. TYPICAL APPLICATION: SINGLE-SUPPLY, HIGH-SIDE CURRENT SENSE AMPLIFIER

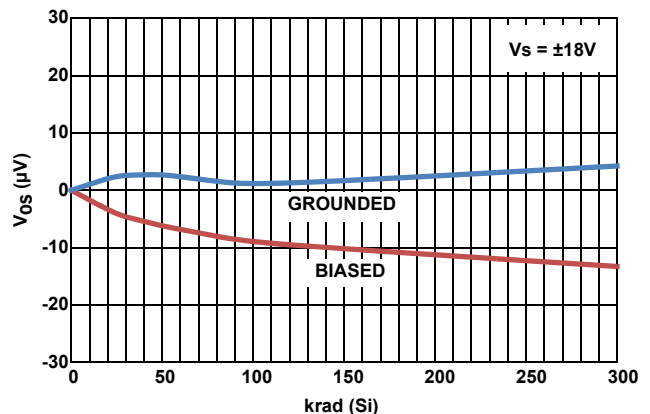
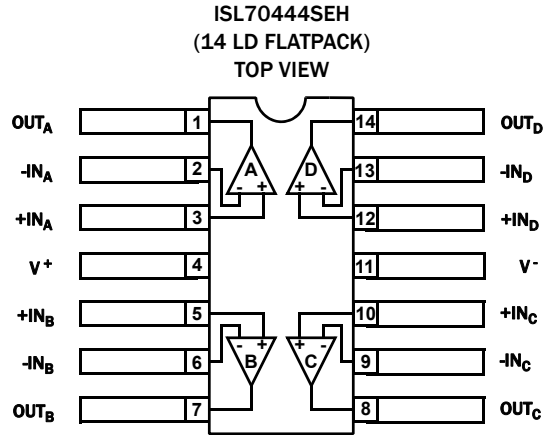


FIGURE 2.  $V_{0S}$  SHIFT vs HIGH DOSE RATE RADIATION

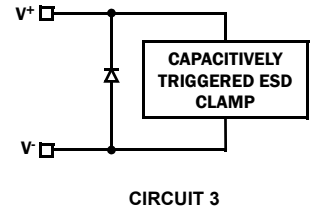
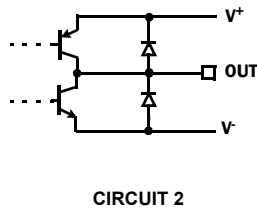
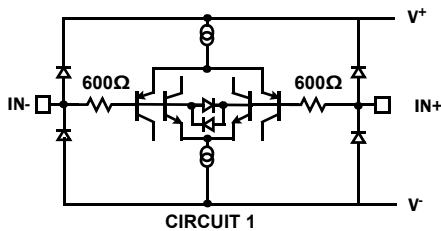
# ISL70444SEH

## Pin Configuration



## Pin Descriptions

PIN NUMBER	PIN NAME	EQUIVALENT ESD CIRCUIT	DESCRIPTION
1	OUT <sub>A</sub>	Circuit 2	Amplifier A output
2	-IN <sub>A</sub>	Circuit 1	Amplifier A inverting input
3	+IN <sub>A</sub>	Circuit 1	Amplifier A non-inverting input
4	V <sup>+</sup>	Circuit 3	Positive power supply
5	+IN <sub>B</sub>	Circuit 1	Amplifier B non-inverting input
6	-IN <sub>B</sub>	Circuit 1	Amplifier B inverting input
7	OUT <sub>B</sub>	Circuit 2	Amplifier B output
8	OUT <sub>C</sub>	Circuit 2	Amplifier C output
9	-IN <sub>C</sub>	Circuit 1	Amplifier C inverting input
10	+IN <sub>C</sub>	Circuit 1	Amplifier C non-inverting input
11	V <sup>-</sup>	Circuit 3	Negative power supply
12	+IN <sub>D</sub>	Circuit 1	Amplifier D non-inverting input
13	-IN <sub>D</sub>	Circuit 1	Amplifier D inverting input
14	OUT <sub>D</sub>	Circuit 2	Amplifier D output
-	E-Pad	None	E-Pad under Package (Unbiased, tied to package lid)



# ISL70444SEH

## Ordering Information

ORDERING/SMD NUMBER	PART NUMBER	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F1321401VXC	ISL70444SEHVF	-55 to +125	14 Ld Flatpack	K14.C
ISL70444SEHF/PROTO	ISL70444SEHF/PROTO	-55 to +125	14 Ld Flatpack	K14.C
5962F1321401V9A	ISL70444SEHVX	-55 to +125	DIE	
ISL70444SEHX/SAMPLE	ISL70444SEHX/SAMPLE	-55 to +125	DIE	
ISL70444SEHEVAL1Z	ISL70444SEHEVAL1Z	Evaluation Board		

### NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. For Moisture Sensitivity Level (MSL), please see device information page for [ISL70444SEH](#). For more information on MSL please see Tech Brief [TB363](#).
3. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table must be used when ordering.

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## Absolute Maximum Ratings

Maximum Supply Voltage	42V
Maximum Supply Voltage (Note 6)	42V
Maximum Differential Input Current	20mA
Maximum Differential Input Voltage	42V or $V^- - 0.5V$ to $V^+ + 0.5V$
Min/Max Input Voltage	42V or $V^- - 0.5V$ to $V^+ + 0.5V$
Max/Min Input Current for Input Voltage $>V^+$ or $<V^-$	$\pm 20mA$
ESD Tolerance	
Human Body Model (Tested per MIL-PRF-883 3015.7)	2kV
Machine Model (Tested per JESD22-A115-A)	200V
Charged Device Model (Tested per CDM-22C10ID)	750V

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ ( $^{\circ}C/W$ )	$\theta_{JC}$ ( $^{\circ}C/W$ )
14 Ld Flatpack Package (Notes 4, 5)	35	9
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$	

## Recommended Operating Conditions

Ambient Operating Temperature Range	$-55^{\circ}C$ to $+125^{\circ}C$
Maximum Operating Junction Temperature	$+150^{\circ}C$
Single Supply Voltage	$3V \pm 10\%$ to $36V \pm 10\%$
Split Rail Supply Voltage	$\pm 1.5V \pm 10\%$ to $\pm 18V \pm 10\%$

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- Theta-ja is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief [TB379](#) for details.
- For  $\theta_{JC}$ , the "case temp" location is the center of the package underside.
- Tested in a heavy ion environment at LET =  $86.4MeV \cdot cm^2/mg$  at  $+125^{\circ}C$  ( $T_C$ ) for SEB. Refer to [Single Event Effects Test Report](#) for more information.

## Electrical Specifications $V_S = \pm 18V$ , $V_{CM} = V_0 = 0V$ , $R_L = \text{Open}$ , $T_A = +25^{\circ}C$ , unless otherwise noted. **Boldface limits apply over the operating temperature range, $-55^{\circ}C$ to $+125^{\circ}C$ .**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$V_{OS}$	Offset Voltage	$V_{CM} = 0V$	-	20	300	$\mu V$
		$V_{CM} = V^+$ to $V^-$	-	80	<b>400</b>	$\mu V$
$TCV_{OS}$	Offset Voltage Temperature Coefficient	$V_{CM} = V^+ - 2V$ to $V^- + 2V$	-	0.5	-	$\mu V/^{\circ}C$
$\Delta V_{OS}$	Input Offset Channel-to-Channel Match	$V_{CM} = V^+$	-	77	<b>800</b>	$\mu V$
		$V_{CM} = V^-$	-	117	<b>800</b>	$\mu V$
$I_B$	Input Bias Current	$V_{CM} = 0V$	-	189	<b>370</b>	nA
		$V_{CM} = V^+$	-	200	<b>370</b>	nA
		$V_{CM} = V^-$	-	262	<b>650</b>	nA
		$V_{CM} = V^+ - 0.5V$	-	200	<b>370</b>	nA
		$V_{CM} = V^- + 0.5V$	-	257	<b>650</b>	nA
$I_{OS}$	Input Offset Current	$V_{CM} = V^+$ to $V^-$	<b>-17</b>	0	<b>17</b>	nA
$V_{CMIR}$	Common Mode Input Voltage Range		<b><math>V^-</math></b>	-	<b><math>V^+</math></b>	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V^-$ to $V^+$	-	112	-	dB
		$V_{CM} = V^-$ to $V^+$	<b>70</b>	-	-	dB
		$V_{CM} = V^+ - 0.5V$ to $V^- + 0.5V$	-	111	-	dB
		$V_{CM} = V^+ - 0.5V$ to $V^- + 0.5V$	<b>80</b>	-	-	dB
PSRR	Power Supply Rejection Ratio	$V^- = -18V$ ; $V^+ = 0.5V$ to $18V$ ; $V^+ = 18V$ ; $V^- = -0.5V$ to $-18V$	-	128	-	dB
			<b>88</b>	-	-	dB
$A_{VOL}$	Open-Loop Gain	$R_L = 10k\Omega$ to ground	-	125	-	dB
			<b>96</b>	-	-	dB
$V_{OH}$	Output Voltage High ( $V_{OUT}$ to $V^+$ )	$R_L = \text{No Load}$	-	78	<b>160</b>	mV
		$R_L = 10k\Omega$	-	118	<b>175</b>	mV
$V_{OL}$	Output Voltage Low ( $V_{OUT}$ to $V^-$ )	$R_L = \text{No Load}$	-	73	<b>160</b>	mV
		$R_L = 10k\Omega$	-	110	<b>175</b>	mV

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**Electrical Specifications**  $V_S = \pm 1.8V$ ,  $V_{CM} = V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted. **Boldface limits apply over the operating temperature range,  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .** (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$I_{SRC}$	Output Short Circuit Current	Sourcing; $V_{IN} = 0V$ , $V_{OUT} = -1.8V$	<b>10</b>	-	-	mA
$I_{SNK}$	Output Short Circuit Current	Sinking; $V_{IN} = 0V$ , $V_{OUT} = +1.8V$	<b>10</b>	-	-	mA
$I_S$	Supply Current/Amplifier	Unity gain	-	1.5	1.75	mA
			-	<b>1.95</b>	<b>2.4</b>	mA
<b>AC SPECIFICATIONS</b>						
GBW	Gain Bandwidth Product	$A_{CL} = 101$ , $R_L = 10k$	-	19	-	MHz
$e_n$	Voltage Noise Density	$f = 10kHz$	-	11.3	-	nV/ $\sqrt{Hz}$
$i_n$	Current Noise Density	$f = 10kHz$	-	0.312	-	pA/ $\sqrt{Hz}$
SR	Large Signal Slew Rate	$A_V = 1$ , $R_L = 10k\Omega$ , $V_O = 10V_{P-P}$	<b>60</b>	-	-	V/ $\mu s$

**Electrical Specifications**  $V_S = \pm 2.5V$ ,  $V_{CM} = V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted. **Boldface limits apply over the operating temperature range,  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$V_{OS}$	Offset Voltage	$V_{CM} = 0V$	-	20	300	$\mu V$
		$V_{CM} = V^+$ to $V^-$	-	80	<b>400</b>	$\mu V$
$TCV_{OS}$	Offset Voltage Temperature Coefficient	$V_{CM} = V^+ - 2V$ to $V^- + 2V$	-	0.5	-	$\mu V/^\circ C$
$\Delta V_{OS}$	Input Offset Channel-to-Channel Match	$V_{CM} = V^+$	-	79	<b>800</b>	$\mu V$
		$V_{CM} = V^-$	-	119	<b>800</b>	$\mu V$
$I_B$	Input Bias Current	$V_{CM} = 0V$	-	202	<b>340</b>	nA
		$V_{CM} = V^+$	-	182	<b>340</b>	nA
		$V_{CM} = V^-$	-	229	<b>580</b>	nA
		$V_{CM} = V^+ - 0.5V$	-	181	<b>340</b>	nA
		$V_{CM} = V^- + 0.5V$	-	224	<b>580</b>	nA
$I_{OS}$	Input Offset Current	$V_{CM} = V^+$ to $V^-$	<b>-17</b>	0	<b>17</b>	nA
$V_{CMIR}$	Common Mode Input Voltage Range		<b><math>V^-</math></b>	-	<b><math>V^+</math></b>	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V^-$ to $V^+$	-	92	-	dB
		$V_{CM} = V^-$ to $V^+$	<b>70</b>	-	-	dB
		$V_{CM} = V^+ - 0.5V$ to $V^- + 0.5V$	-	91	-	dB
		$V_{CM} = V^+ - 0.5V$ to $V^- + 0.5V$	<b>74</b>	-	-	dB
PSRR	Power Supply Rejection Ratio	$V^- = -2.5V$ ; $V^+ = 0.5V$ to $2.5V$ ; $V^+ = 2.5V$ ; $V^- = -0.5V$ to $-2.5V$	-	123	-	dB
			<b>80</b>	-	-	dB
$A_{VOL}$	Open-Loop Gain	$R_L = 10k\Omega$ to ground	-	118	-	dB
			<b>90</b>	-	-	dB
$V_{OH}$	Output Voltage High ( $V_{OUT}$ to $V^+$ )	$R_L = \text{No Load}$	-	53	<b>85</b>	mV
		$R_L = 10k\Omega$	-	53	<b>105</b>	mV
		$R_L = 600\Omega$	-	-	<b>400</b>	mV

# ISL70444SEH

**Electrical Specifications**  $V_S = \pm 2.5V$ ,  $V_{CM} = V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted. **Boldface limits apply over the operating temperature range,  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .** (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$V_{OL}$	Output Voltage Low ( $V_{OUT}$ to $V^-$ )	$R_L = \text{No Load}$	-	53	<b>85</b>	mV
		$R_L = 10k\Omega$	-	53	<b>105</b>	mV
		$R_L = 600\Omega$	-	-	<b>400</b>	mV
$I_S$	Supply Current/Amplifier	Unity gain	-	1.1	1.25	mA
			-	<b>1.6</b>	<b>1.8</b>	mA
<b>AC SPECIFICATIONS</b>						
GBW	Gain Bandwidth Product	$A_{CL} = 101$ , $R_L = 10k$	-	17	-	MHz
$e_n$	Voltage Noise Density	$f = 10kHz$	-	12.3	-	nV/ $\sqrt{\text{Hz}}$
$i_n$	Current Noise Density	$f = 10kHz$	-	0.313	-	pA/ $\sqrt{\text{Hz}}$
SR	Large Signal Slew Rate	$A_V = 1$ , $R_L = 10k\Omega$ , $V_O = 3V_{P-P}$	-	35	-	V/ $\mu\text{s}$

**Electrical Specifications**  $V_S = \pm 1.5V$ ,  $V_{CM} = V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted. **Boldface limits apply over the operating temperature range,  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$V_{OS}$	Offset Voltage	$V_{CM} = 0V$	-	51	300	$\mu\text{V}$
		$V_{CM} = V_+$ to $V^-$	-	80	<b>400</b>	$\mu\text{V}$
$\Delta V_{OS}$	Input Offset Channel-to-Channel Match	$V_{CM} = V^+$	-	79	<b>800</b>	$\mu\text{V}$
		$V_{CM} = V^-$	-	119	<b>800</b>	$\mu\text{V}$
$I_B$	Input Bias Current	$V_{CM} = 0V$	-	220	<b>330</b>	nA
		$V_{CM} = V^+$	-	180	<b>330</b>	nA
		$V_{CM} = V^-$	-	225	<b>565</b>	nA
		$V_{CM} = V^+ - 0.5V$	-	180	<b>330</b>	nA
		$V_{CM} = V^- + 0.5V$	-	223	<b>565</b>	nA
$I_{OS}$	Input Offset Current	$V_{CM} = V^+$ to $V^-$	<b>-17</b>	0	<b>17</b>	nA
$V_{CMIR}$	Common Mode Input Voltage Range		<b><math>V^-</math></b>	-	<b><math>V^+</math></b>	V
$V_{OH}$	Output Voltage High ( $V_{OUT}$ to $V^+$ )	$R_L = \text{No Load}$	-	26	<b>39</b>	mV
		$R_L = 10k\Omega$	-	30	<b>60</b>	mV
$V_{OL}$	Output Voltage Low ( $V_{OUT}$ to $V^-$ )	$R_L = \text{No Load}$	-	26	<b>39</b>	mV
		$R_L = 10k\Omega$	-	42	<b>60</b>	mV
$I_S$	Supply Current/Amplifier	Unity Gain	-	1.1	1.24	mA
			-	<b>1.57</b>	<b>1.8</b>	mA
<b>AC SPECIFICATIONS</b>						
GBW	Gain Bandwidth Product	$A_{CL} = 101$ , $R_L = 10k$	-	16	-	MHz
$e_n$	Voltage Noise Density	$f = 10kHz$	-	12	-	nV/ $\sqrt{\text{Hz}}$
$i_n$	Current Noise Density	$f = 10kHz$	-	0.312	-	pA/ $\sqrt{\text{Hz}}$

# ISL70444SEH

**Electrical Specifications**  $V_S = \pm 18V$ ,  $V_{CM} = V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ C$ , unless otherwise noted. **Boldface limits apply over a total ionizing dose of 300krad(SI) with exposure of a high dose rate of 50 to 300rad(SI)/s and over a total ionizing dose of 50krad(SI) with exposure at a low dose rate of <10mrad(SI)/s.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$V_{OS}$	Offset Voltage	$V_{CM} = V^+$ to $V^-$	-	-	<b>400</b>	$\mu V$
$\Delta V_{OS}$	Input Offset Channel-to-Channel Match	$V_{CM} = V^+$	-	-	<b>800</b>	$\mu V$
		$V_{CM} = V^-$	-	-	<b>800</b>	$\mu V$
$I_B$	Input Bias Current	$V_{CM} = V^+$	-	-	<b>650</b>	nA
		$V_{CM} = V^-$	<b>-650</b>	-	-	nA
$I_{OS}$	Input Offset Current	$V_{CM} = V^+$ to $V^-$	<b>-17</b>	-	<b>17</b>	nA
$V_{CMIR}$	Common Mode Input Voltage Range		<b>V<sup>-</sup></b>	-	<b>V<sup>+</sup></b>	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V^-$ to $V^+$	-	-	-	dB
		$V_{CM} = V^-$ to $V^+$	<b>70</b>	-	-	dB
		$V_{CM} = V^+ - 0.5V$ to $V^- + 0.5V$	-	-	-	dB
		$V_{CM} = V^+ - 0.5V$ to $V^- + 0.5V$	<b>80</b>	-	-	dB
PSRR	Power Supply Rejection Ratio	$V^- = -18V$ ; $V^+ = 0.5V$ to $18V$ ; $V^+ = 18V$ ; $V^- = -0.5V$ to $-18V$	-	-	-	dB
			<b>88</b>	-	-	dB
$A_{VOL}$	Open-Loop Gain	$R_L = 10k\Omega$ to ground	-	-	-	dB
			<b>96</b>	-	-	dB
$V_{OH}$	Output Voltage High ( $V_{OUT}$ to $V^+$ )	$R_L = \text{No Load}$	-	-	<b>160</b>	mV
		$R_L = 10k\Omega$	-	-	<b>175</b>	mV
$V_{OL}$	Output Voltage Low ( $V_{OUT}$ to $V^-$ )	$R_L = \text{No Load}$	-	-	<b>150</b>	mV
		$R_L = 10k\Omega$	-	-	<b>165</b>	mV
$I_{SRC}$	Output Short Circuit Current	Sourcing; $V_{IN} = 0V$ , $V_{OUT} = -18V$	<b>10</b>	-	-	mA
$I_{SNK}$	Output Short Circuit Current	Sinking; $V_{IN} = 0V$ , $V_{OUT} = +18V$	<b>10</b>	-	-	mA
$I_S$	Supply Current/Amplifier	Unity gain	-	-	<b>2.4</b>	mA
SR	Large Signal Slew Rate	$AV = 1$ , $R_L = 10k\Omega$ , $V_O = 10V_{P-P}$	<b>60</b>			V/ $\mu s$

**Electrical Specifications**  $V_S = \pm 2.5V$ ,  $V_{CM} = V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ C$ , unless otherwise noted. **Boldface limits apply a total ionizing dose of 300krad(SI) with exposure of a high dose rate of 50 to 300rad(SI)/s and over a total ionizing dose of 50krad(SI) with exposure at a low dose rate of <10mrad(SI)/s.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$V_{OS}$	Offset Voltage	$V_{CM} = V^+$ to $V^-$	-	-	<b>400</b>	$\mu V$
$\Delta V_{OS}$	Input Offset Channel-to-Channel Match	$V_{CM} = V^+$	-	-	<b>800</b>	$\mu V$
		$V_{CM} = V^-$	-	-	<b>800</b>	$\mu V$
$I_B$	Input Bias Current	$V_{CM} = V^+$	-	-	<b>650</b>	nA
		$V_{CM} = V^-$	<b>-650</b>	-	-	nA
$I_{OS}$	Input Offset Current	$V_{CM} = V^+$ to $V^-$	<b>-17</b>	-	<b>17</b>	nA
$V_{CMIR}$	Common Mode Input Voltage Range		<b>V<sup>-</sup></b>	-	<b>V<sup>+</sup></b>	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V^-$ to $V^+$	-	-	-	dB
		$V_{CM} = V^-$ to $V^+$	<b>70</b>	-	-	dB
		$V_{CM} = V^+ - 0.5V$ to $V^- + 0.5V$	-	-	-	dB
		$V_{CM} = V^+ - 0.5V$ to $V^- + 0.5V$	<b>74</b>	-	-	dB

# ISL70444SEH

**Electrical Specifications**  $V_S = \pm 2.5V$ ,  $V_{CM} = V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ C$ , unless otherwise noted. **Boldface limits apply a total ionizing dose of 300krad(SI) with exposure of a high dose rate of 50 to 300rad(SI)/s and over a total ionizing dose of 50krad(SI) with exposure at a low dose rate of <10mrad(SI)/s. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
PSRR	Power Supply Rejection Ratio	$V^- = -2.5V$ ; $V^+ = 0.5V$ to $2.5V$ ; $V^+ = 2.5V$ ; $V^- = -0.5V$ to $-2.5V$	-	-	-	dB
			<b>80</b>	-	-	dB
$A_{VOL}$	Open-Loop Gain	$R_L = 10k\Omega$ to ground	-	-	-	dB
			<b>90</b>	-	-	dB
$V_{OH}$	Output Voltage High ( $V_{OUT}$ to $V^+$ )	$R_L = \text{No Load}$	-	-	<b>85</b>	mV
		$R_L = 10k\Omega$	-	-	<b>105</b>	mV
		$R_L = 600\Omega$	-	-	<b>400</b>	mV
$V_{OL}$	Output Voltage Low ( $V_{OUT}$ to $V^-$ )	$R_L = \text{No Load}$	-	-	<b>85</b>	mV
		$R_L = 10k\Omega$	-	-	<b>105</b>	mV
		$R_L = 600\Omega$	-	-	<b>400</b>	mV
$I_S$	Supply Current/Amplifier	Unity gain	-	-	<b>1.8</b>	mA

**Electrical Specifications**  $V_S = \pm 1.5V$ ,  $V_{CM} = V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ C$ , unless otherwise noted. **Boldface limits apply a total ionizing dose of 300krad(SI) with exposure of a high dose rate of 50-300rad(SI)/s and over a total ionizing dose of 50krad(SI) with exposure at a low dose rate of <10mrad(SI)/s.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$V_{OS}$	Offset Voltage	$V_{CM} = V^+$ to $V^-$	-	-	<b>400</b>	$\mu V$
$\Delta V_{OS}$	Input Offset Channel-to-Channel Match	$V_{CM} = V^+$	-	-	<b>800</b>	$\mu V$
		$V_{CM} = V^-$	-	-	<b>800</b>	$\mu V$
$I_B$	Input Bias Current	$V_{CM} = V^+$	-	-	<b>650</b>	nA
		$V_{CM} = V^-$	<b>-650</b>	-	-	nA
$I_{OS}$	Input Offset Current	$V_{CM} = V^+$ to $V^-$	<b>-17</b>	-	<b>17</b>	nA
$V_{CMIR}$	Common Mode Input Voltage Range		<b><math>V^-</math></b>	-	<b><math>V^+</math></b>	V
$V_{OH}$	Output Voltage High ( $V_{OUT}$ to $V^+$ )	$R_L = \text{No Load}$	-	-	<b>160</b>	mV
		$R_L = 10k\Omega$	-	-	<b>175</b>	mV
$V_{OL}$	Output Voltage Low ( $V_{OUT}$ to $V^-$ )	$R_L = \text{No Load}$	-	-	<b>150</b>	mV
		$R_L = 10k\Omega$	-	-	<b>165</b>	mV
$I_S$	Supply Current/Amplifier	Unity gain	-	-	<b>1.8</b>	mA

NOTE:

- Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.



## Typical Performance Curves Unless otherwise specified, $V_S \pm 18V$ , $V_{CM} = 0$ , $V_O = 0V$ , $T_A = +25^\circ C$ .

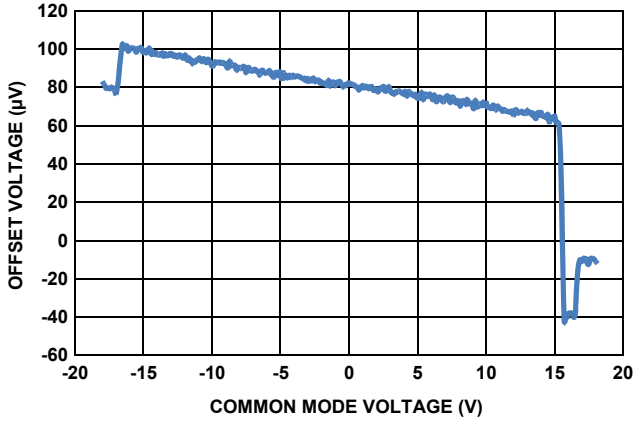


FIGURE 3. OFFSET VOLTAGE vs COMMON MODE VOLTAGE

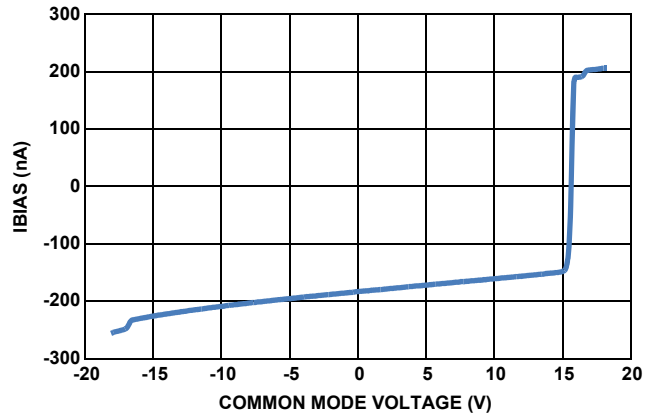


FIGURE 4. IBIAS vs COMMON MODE VOLTAGE

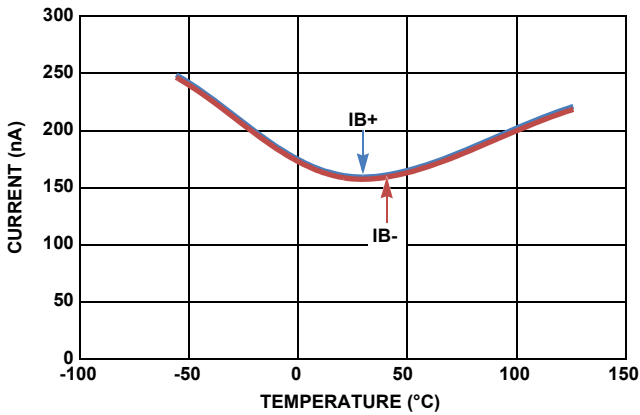


FIGURE 5. IBIAS vs TEMPERATURE ( $V_S = \pm 18V$ )

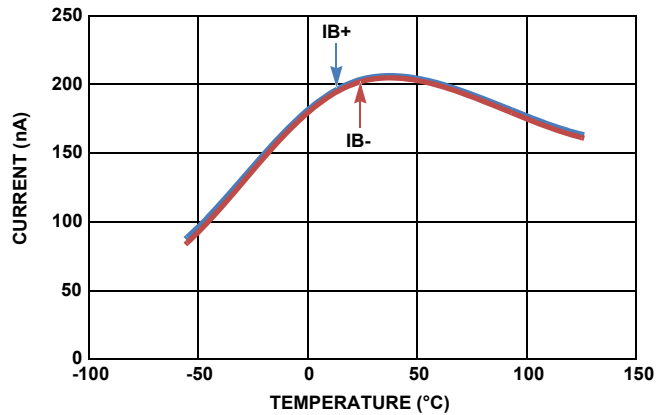


FIGURE 6. IBIAS vs TEMPERATURE ( $V_S = \pm 2.5V$ )

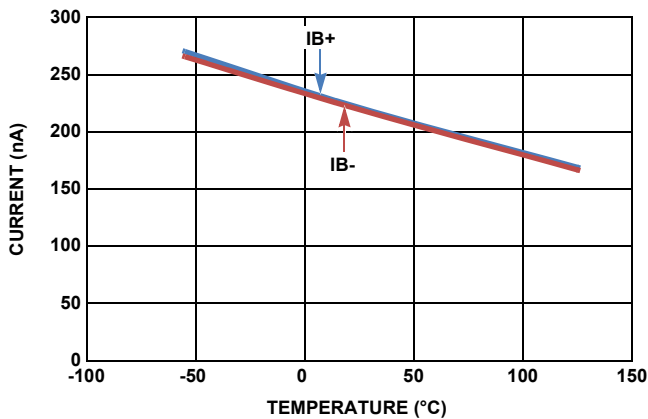


FIGURE 7. IBIAS vs TEMPERATURE, ( $V_S = \pm 1.5V$ )

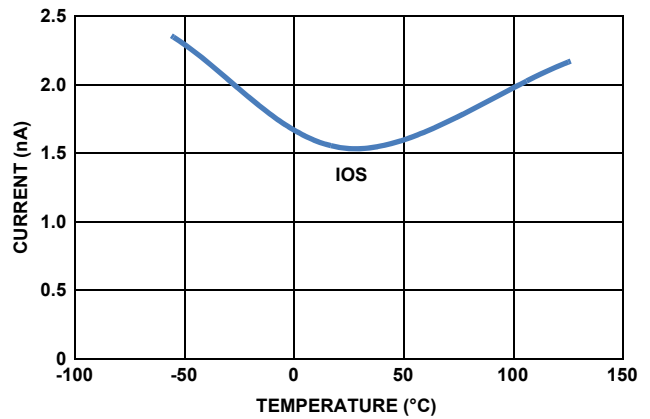


FIGURE 8. IOS vs TEMPERATURE ( $V_S = \pm 18V$ )

## Typical Performance Curves Unless otherwise specified, $V_S \pm 18V$ , $V_{CM} = 0$ , $V_O = 0V$ , $T_A = +25^\circ C$ . (Continued)

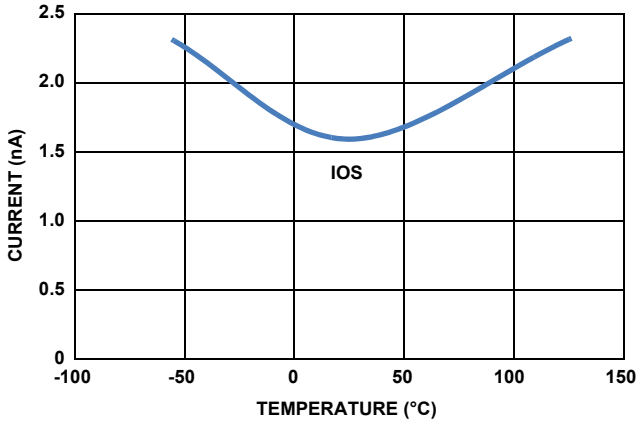


FIGURE 9. IOS vs TEMPERATURE ( $V_S = \pm 2.5V$ )

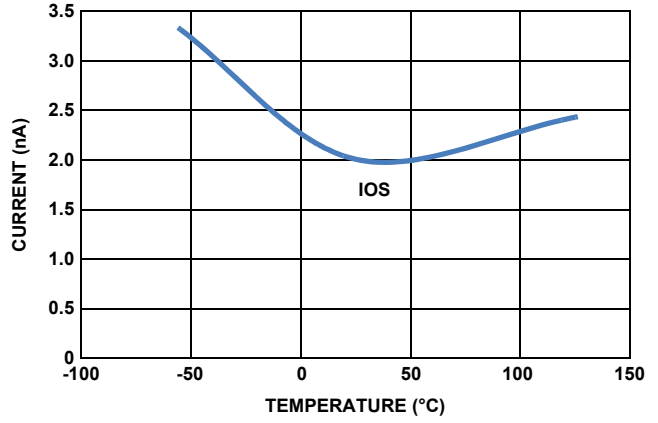


FIGURE 10. IOS vs TEMPERATURE ( $V_S = \pm 1.5V$ )

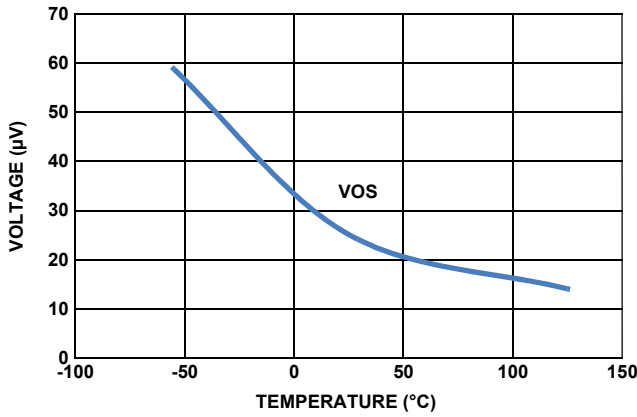


FIGURE 11. VOS vs TEMPERATURE ( $V_S = \pm 18V$ )

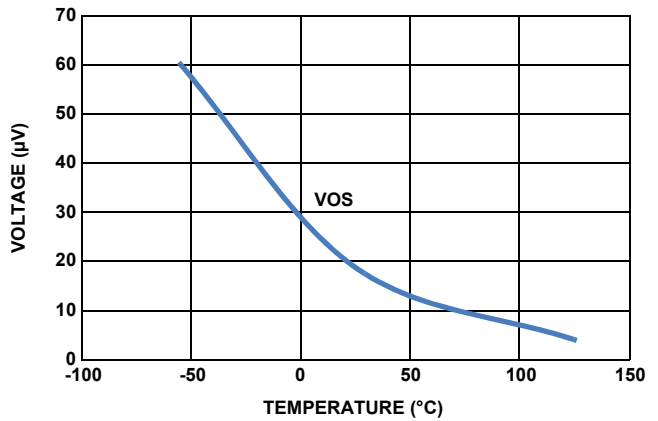


FIGURE 12. VOS vs TEMPERATURE ( $V_S = \pm 2.5V$ )

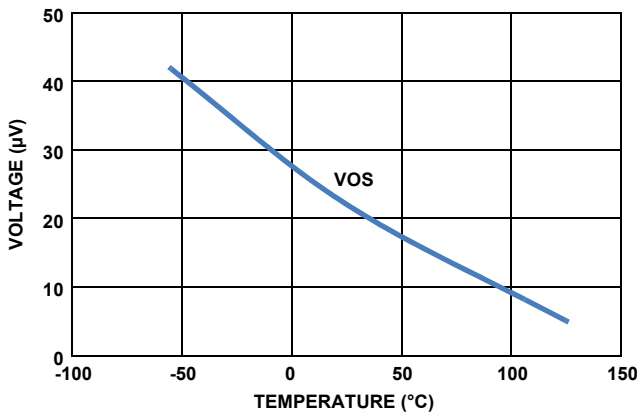


FIGURE 13. VOS vs TEMPERATURE ( $V_S = \pm 1.5V$ )

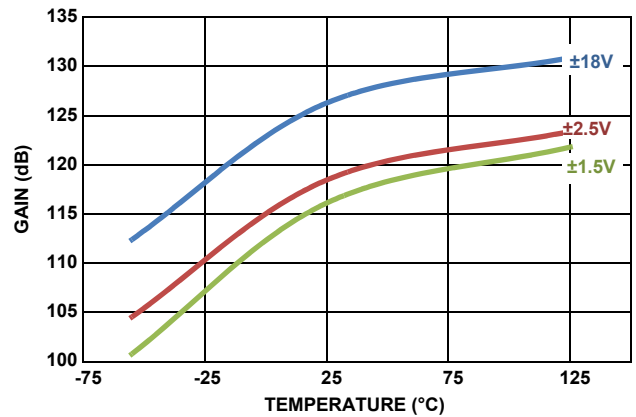


FIGURE 14. AVOL vs TEMPERATURE vs SUPPLY VOLTAGE

## Typical Performance Curves Unless otherwise specified, $V_S \pm 18V$ , $V_{CM} = 0$ , $V_O = 0V$ , $T_A = +25^\circ C$ . (Continued)

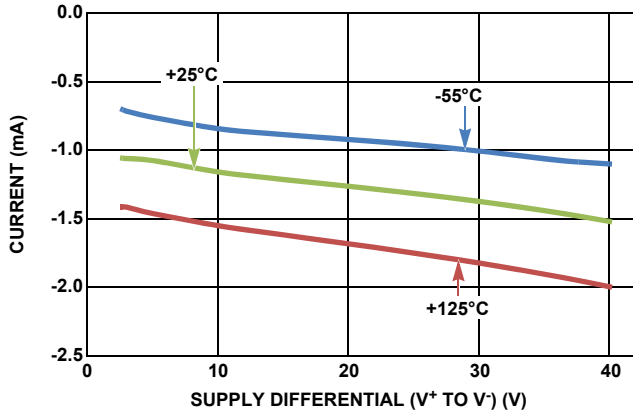


FIGURE 15. NEGATIVE SUPPLY CURRENT vs SUPPLY VOLTAGE

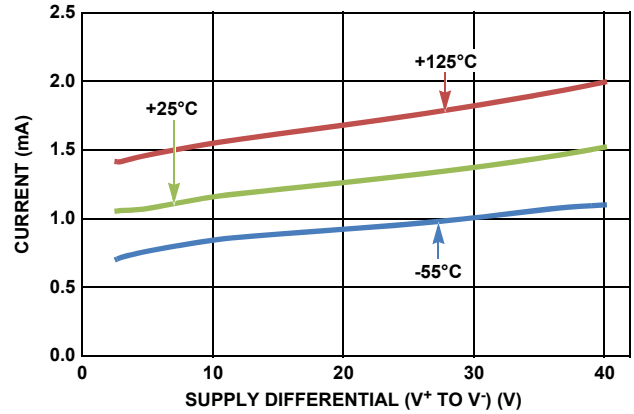


FIGURE 16. POSITIVE SUPPLY CURRENT vs SUPPLY VOLTAGE

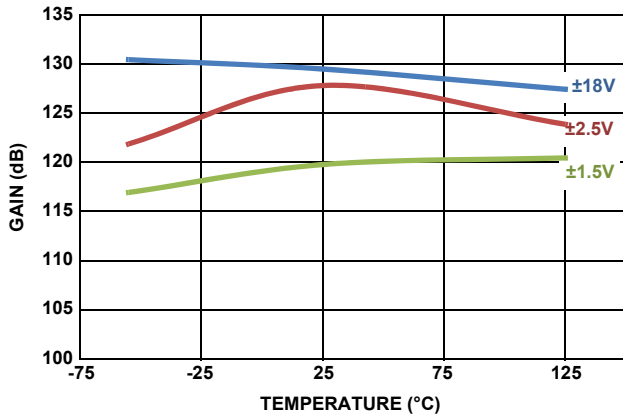


FIGURE 17. PSRR+ vs TEMPERATURE vs SUPPLY VOLTAGE

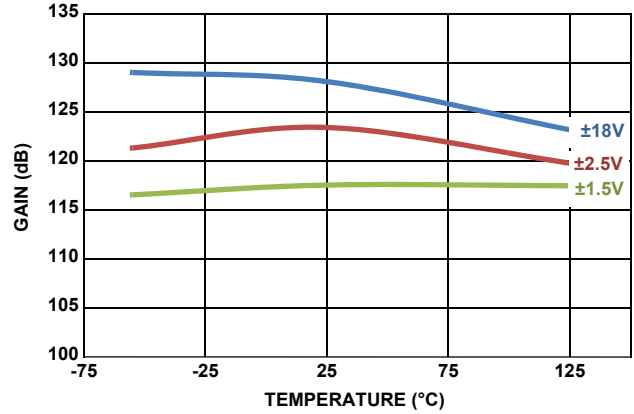


FIGURE 18. PSRR- vs TEMPERATURE vs SUPPLY VOLTAGE

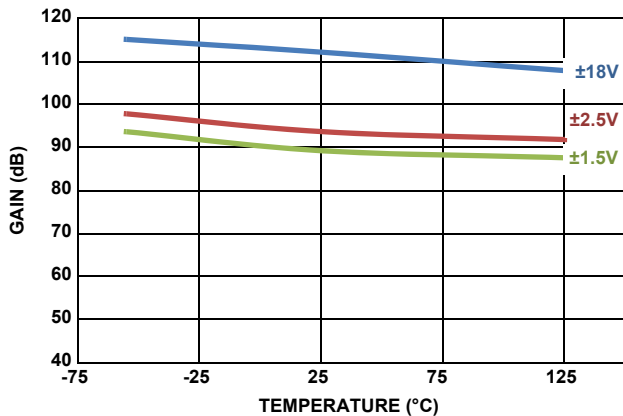


FIGURE 19. CMRR vs TEMPERATURE vs SUPPLY VOLTAGE

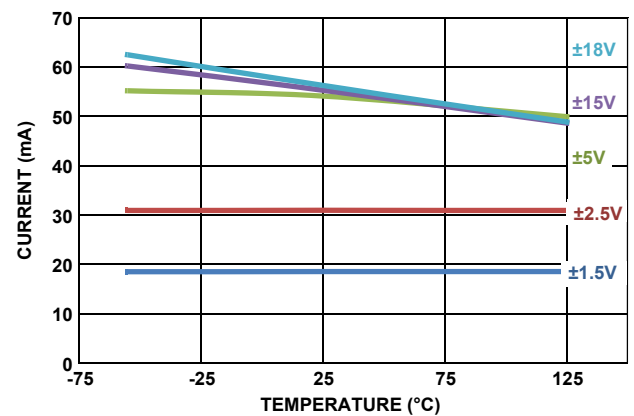


FIGURE 20. SHORT CIRCUIT CURRENT vs TEMPERATURE

## Typical Performance Curves Unless otherwise specified, $V_S = \pm 18V$ , $V_{CM} = 0$ , $V_O = 0V$ , $T_A = +25^\circ C$ . (Continued)

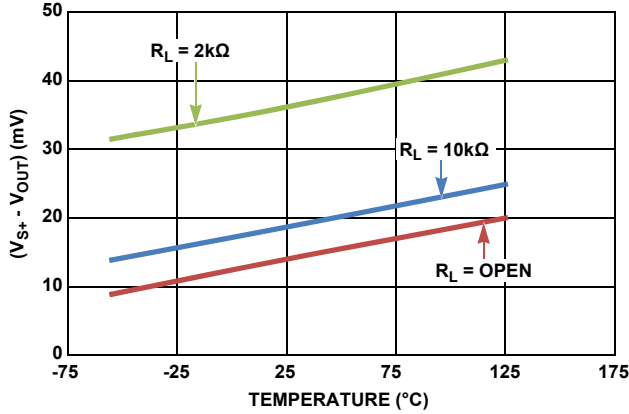


FIGURE 21. ( $V_S = \pm 1.5V$ ) VOH vs TEMPERATURE

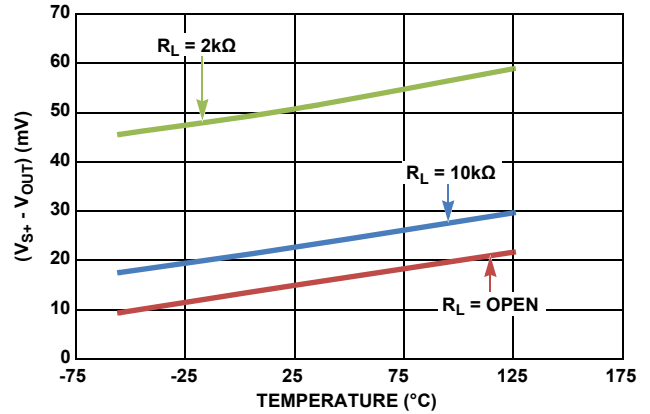


FIGURE 22. ( $V_S = \pm 2.5V$ ) VOH vs TEMPERATURE

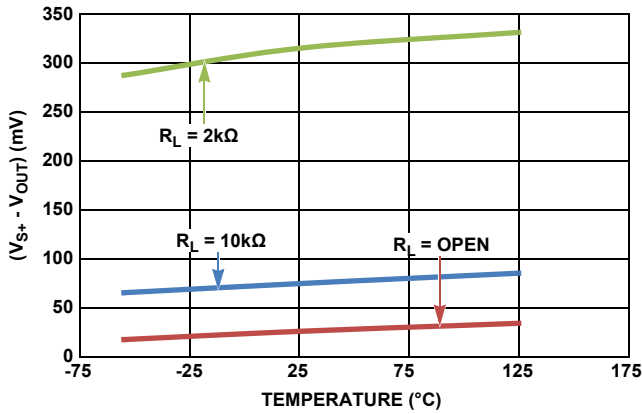


FIGURE 23. ( $V_S = \pm 18V$ ) VOH vs TEMPERATURE

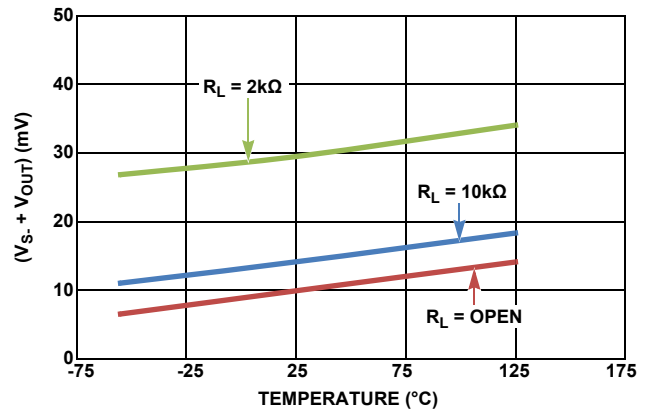


FIGURE 24. ( $V_S = \pm 1.5V$ ) VOL vs TEMPERATURE

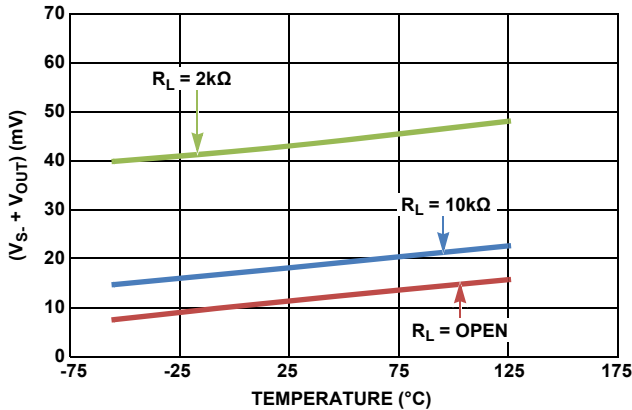


FIGURE 25. ( $V_S = \pm 2.5V$ ) VOL vs TEMPERATURE

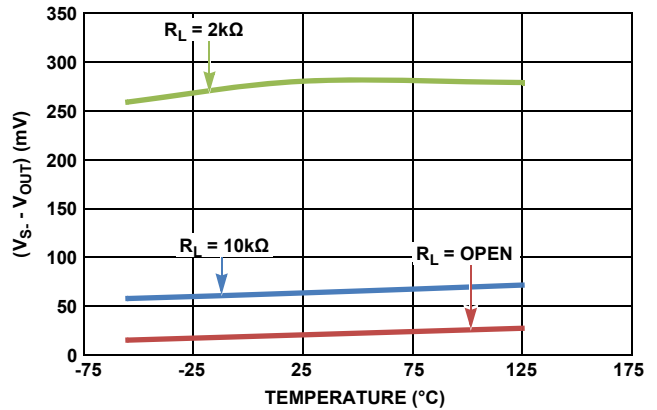


FIGURE 26. ( $V_S = \pm 18V$ ) VOL vs TEMPERATURE

## Typical Performance Curves Unless otherwise specified, $V_S \pm 18V$ , $V_{CM} = 0$ , $V_O = 0V$ , $T_A = +25^\circ C$ . (Continued)

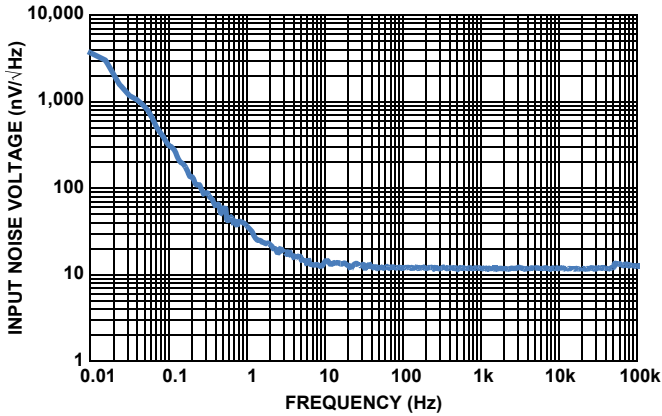


FIGURE 27. INPUT NOISE VOLTAGE SPECTRAL DENSITY ( $V_S = \pm 18V$ )

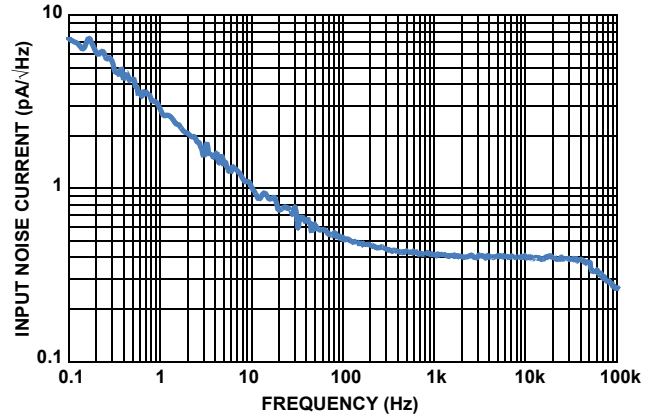


FIGURE 28. INPUT NOISE CURRENT SPECTRAL DENSITY ( $V_S = \pm 18V$ )

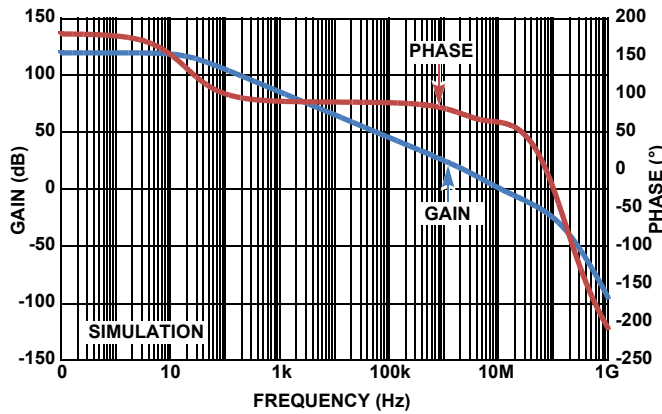


FIGURE 29. OPEN LOOP FREQUENCY RESPONSE ( $C_L = 0.01pF$ )

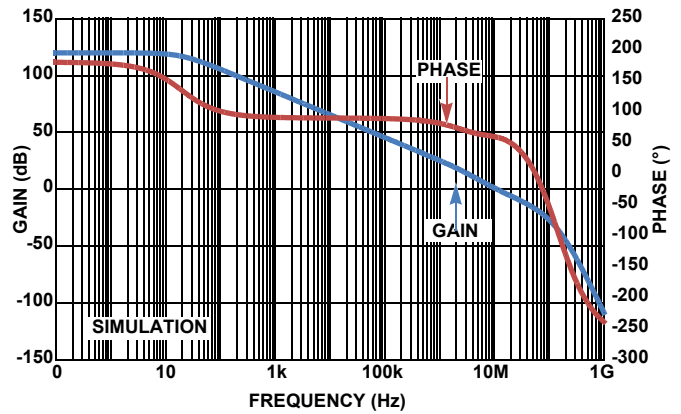


FIGURE 30. OPEN LOOP FREQUENCY RESPONSE ( $C_L = 10pF$ )

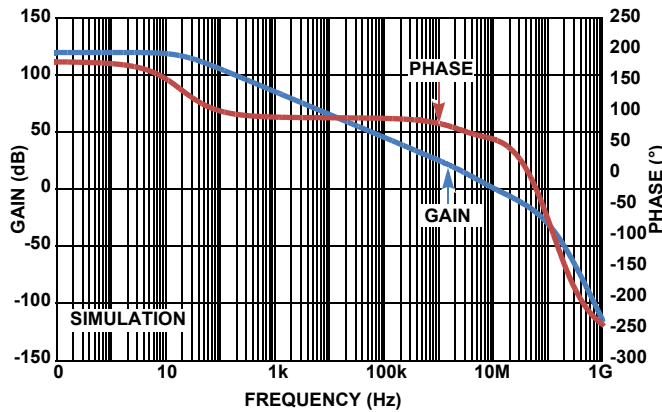


FIGURE 31. OPEN LOOP FREQUENCY RESPONSE ( $C_L = 22pF$ )

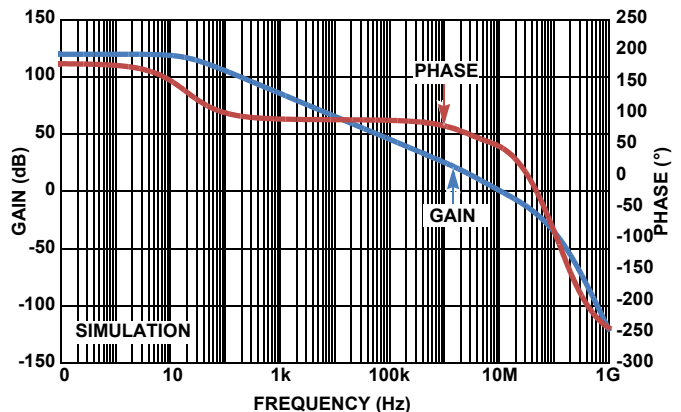


FIGURE 32. OPEN LOOP FREQUENCY RESPONSE ( $C_L = 47pF$ )

## Typical Performance Curves Unless otherwise specified, $V_S \pm 18V$ , $V_{CM} = 0$ , $V_O = 0V$ , $T_A = +25^\circ C$ . (Continued)

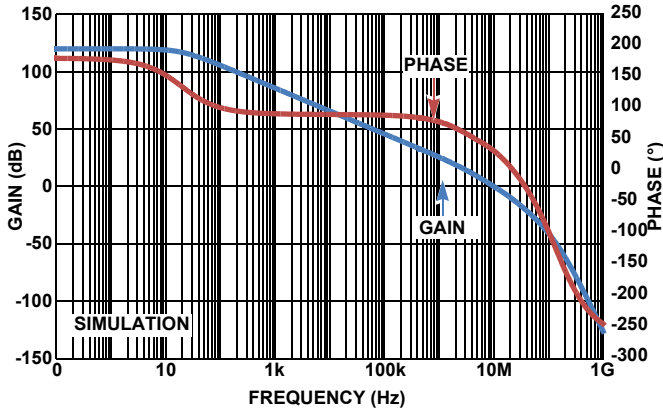


FIGURE 33. OPEN LOOP FREQUENCY RESPONSE ( $C_L = 100pF$ )

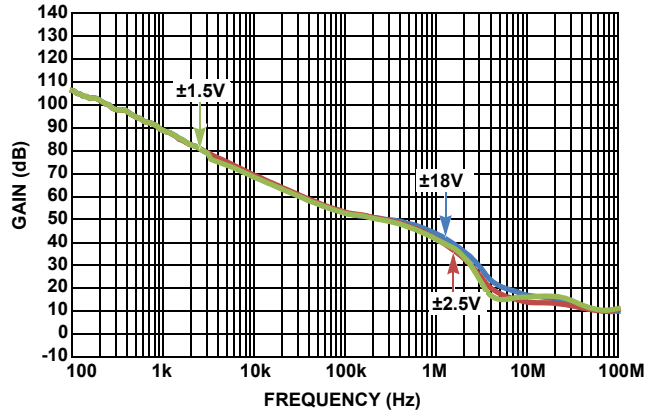


FIGURE 34. CMRR vs FREQUENCY

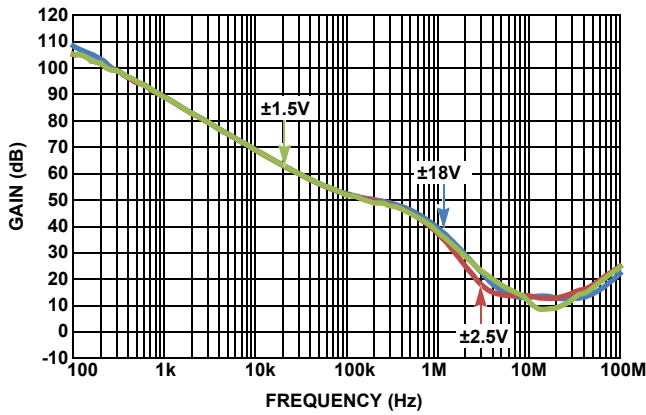


FIGURE 35. PSRR vs FREQUENCY

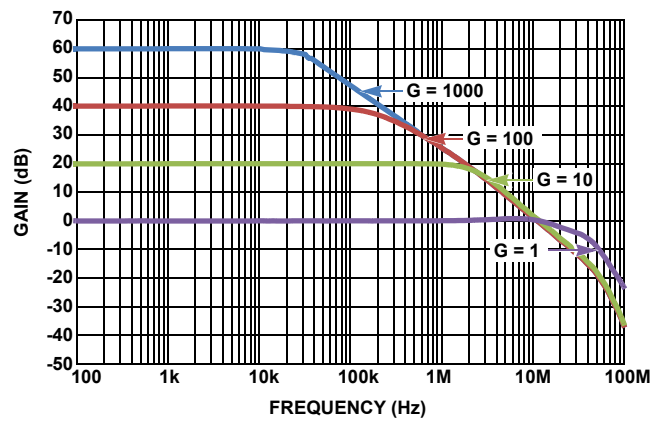


FIGURE 36. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

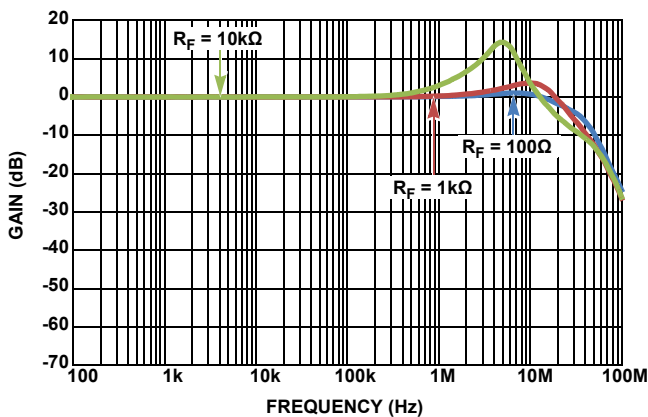


FIGURE 37. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE ( $R_F$ )

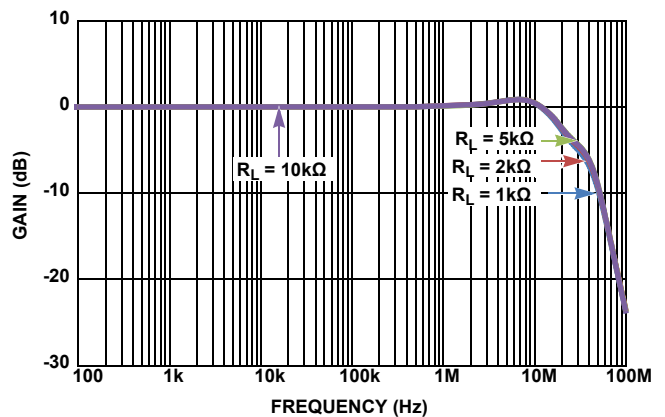


FIGURE 38. FREQUENCY RESPONSE vs LOAD RESISTANCE

## Typical Performance Curves Unless otherwise specified, $V_S = \pm 18V$ , $V_{CM} = 0$ , $V_O = 0V$ , $T_A = +25^\circ C$ . (Continued)

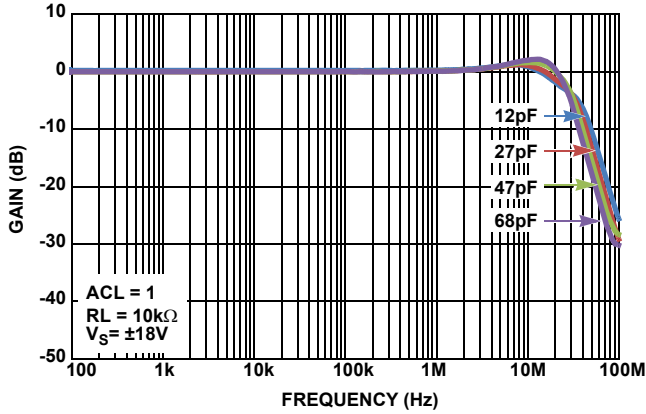


FIGURE 39. UNITY GAIN RESPONSE vs LOAD CAPACITANCE

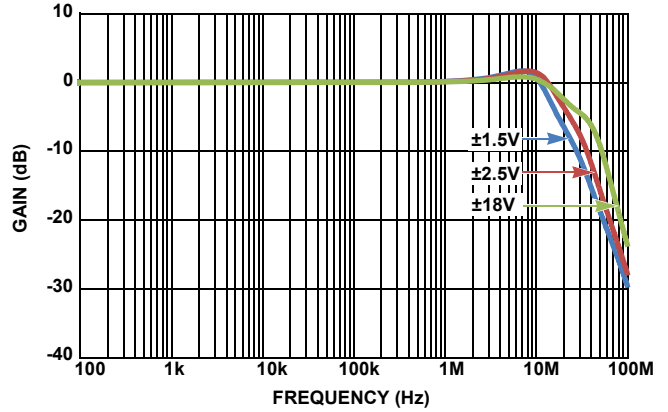


FIGURE 40. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

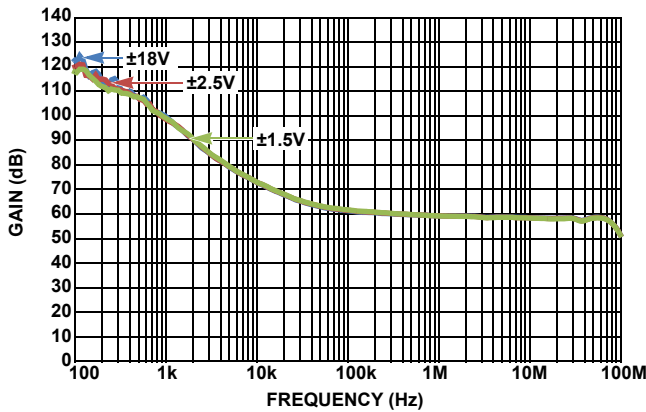


FIGURE 41. CROSTALK REJECTION

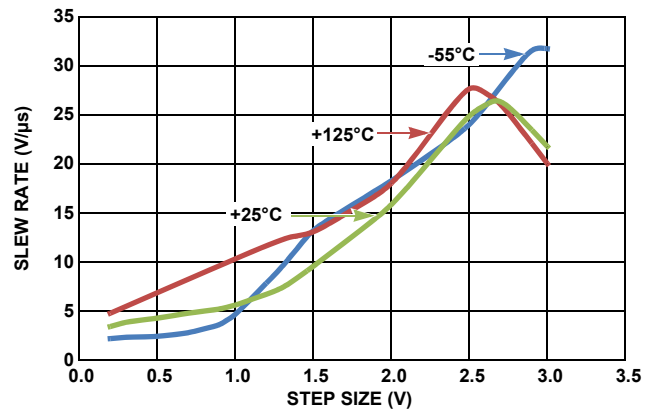


FIGURE 42. SLEW RATE vs STEP SIZE vs TEMPERATURE ( $V_S = \pm 1.5V$ )

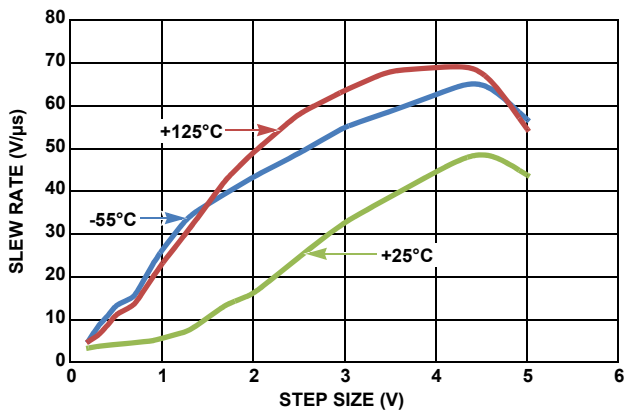


FIGURE 43. SLEW RATE vs STEP SIZE vs TEMPERATURE ( $V_S = \pm 2.5V$ )

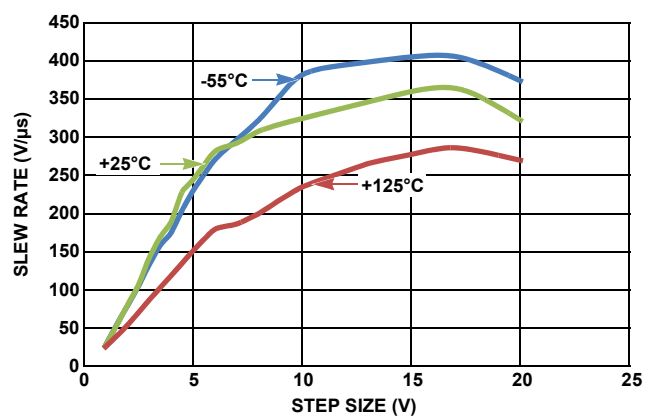


FIGURE 44. SLEW RATE vs STEP SIZE vs TEMPERATURE ( $V_S = \pm 18V$ )

## Typical Performance Curves Unless otherwise specified, $V_S \pm 18V$ , $V_{CM} = 0$ , $V_O = 0V$ , $T_A = +25^\circ C$ . (Continued)

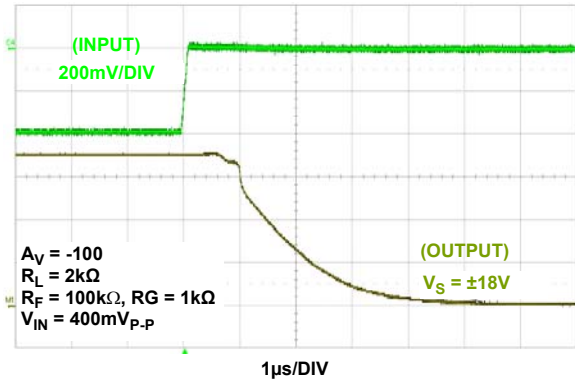


FIGURE 45. SATURATION RECOVERY ( $V_S = \pm 18V$ )

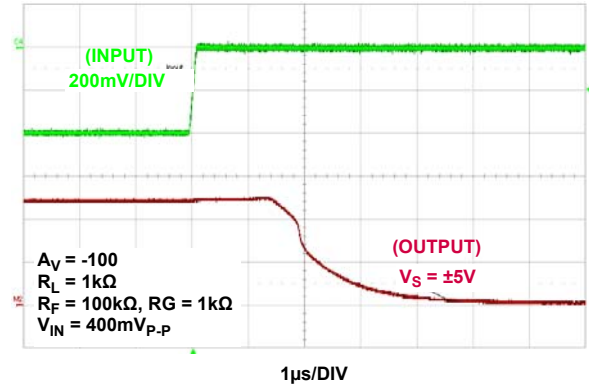


FIGURE 46. SATURATION RECOVERY ( $V_S = \pm 5V$ )

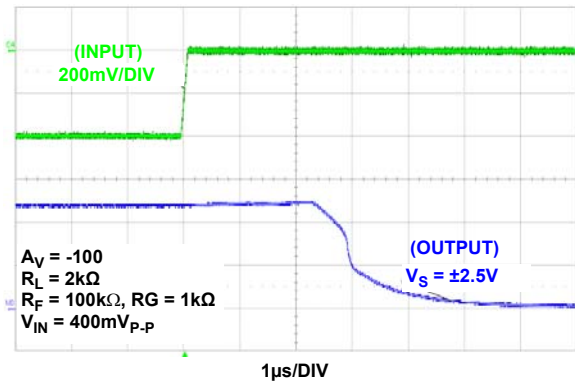


FIGURE 47. SATURATION RECOVERY ( $V_S = \pm 2.5V$ )

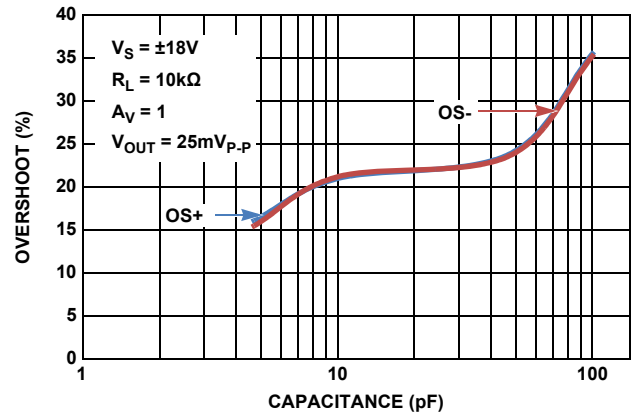


FIGURE 48. OVERSHOOT (%) vs LOAD CAPACITANCE

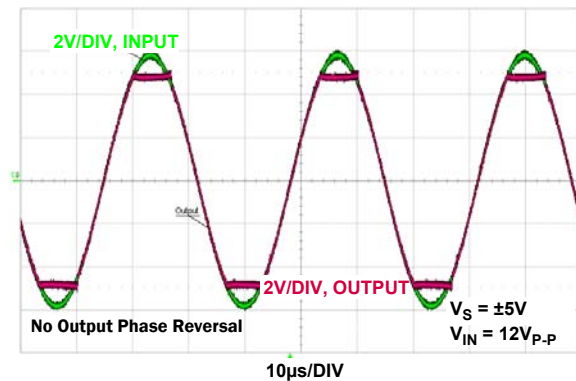


FIGURE 49. INPUT OVERDRIVE RESPONSE



**Post High Dose Rate Radiation Characteristics** Unless otherwise specified,  $V_S \pm 18V$ ,  $V_{CM} = 0$ ,  $V_O = 0V$ ,  $T_A = +25^\circ C$ . This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

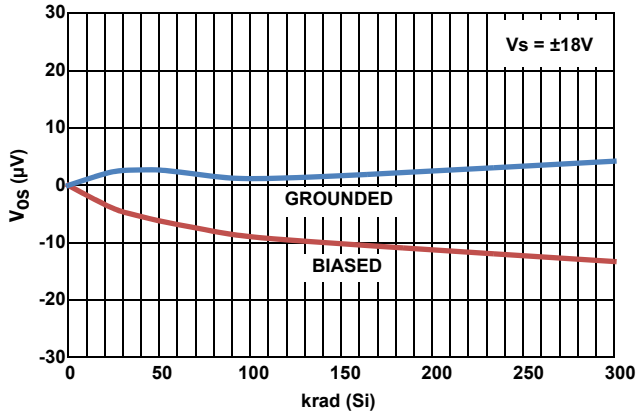


FIGURE 50.  $V_{OS}$  SHIFT vs HIGH DOSE RATE RADIATION

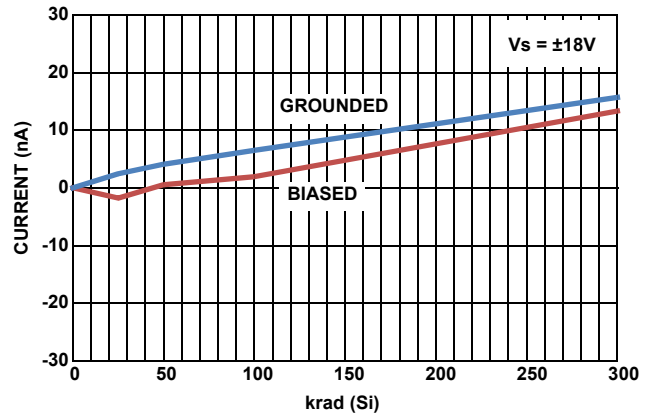


FIGURE 51.  $I_{BIAS}$  SHIFT vs HIGH DOSE RATE RADIATION

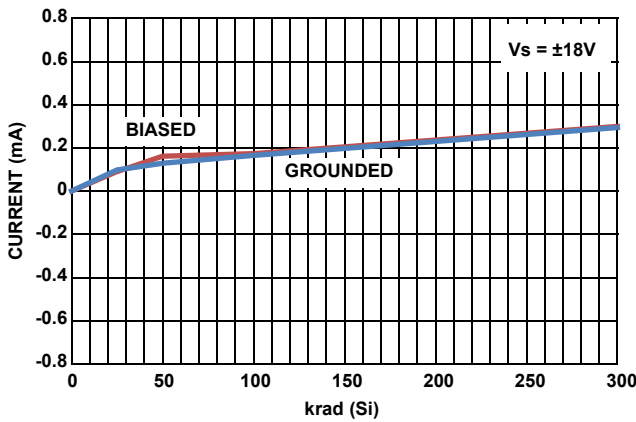


FIGURE 52.  $I^-$  SHIFT vs HIGH DOSE RATE RADIATION

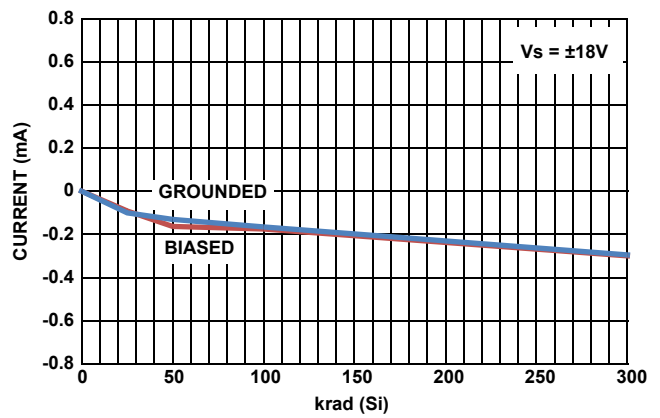


FIGURE 53.  $I^+$  SHIFT vs HIGH DOSE RATE RADIATION

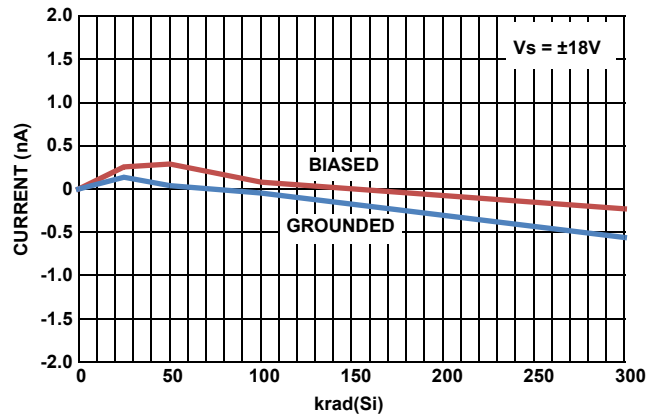


FIGURE 54.  $I_{OS}$  SHIFT vs HIGH DOSE RATE RADIATION

**Post Low Dose Rate Radiation Characteristics** Unless otherwise specified,  $V_S \pm 18V$ ,  $V_{CM} = 0$ ,  $V_O = 0V$ ,  $T_A = +25^\circ C$ . This data is typical mean test data post radiation exposure at a low dose rate of  $<10\text{mrad}(\text{Si})/\text{s}$ . This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

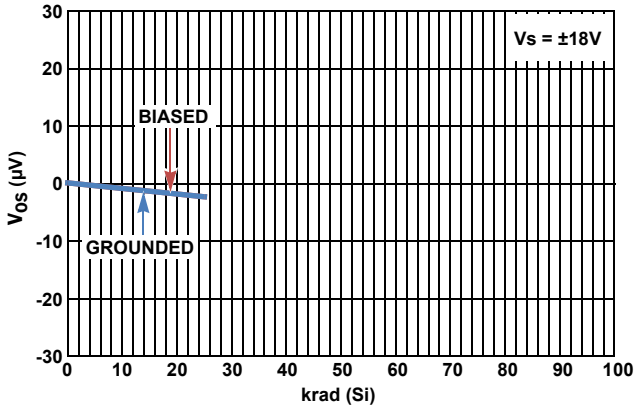


FIGURE 55.  $V_{OS}$  SHIFT vs LOW DOSE RATE RADIATION

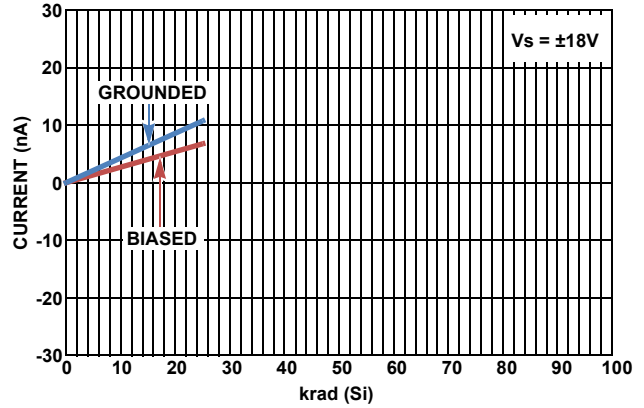


FIGURE 56.  $I_{BIAS}$  SHIFT vs LOW DOSE RATE RADIATION

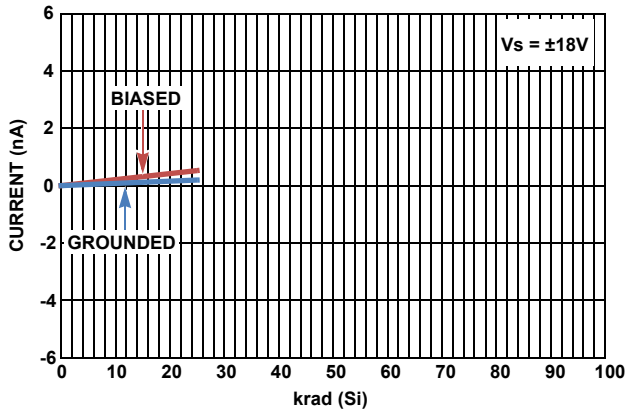


FIGURE 57.  $I_{OS}$  SHIFT vs LOW DOSE RATE RADIATION

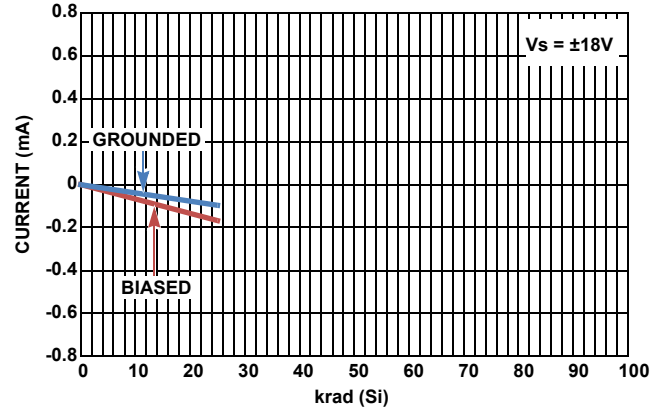


FIGURE 58.  $I^+$  SHIFT vs LOW DOSE RATE RADIATION

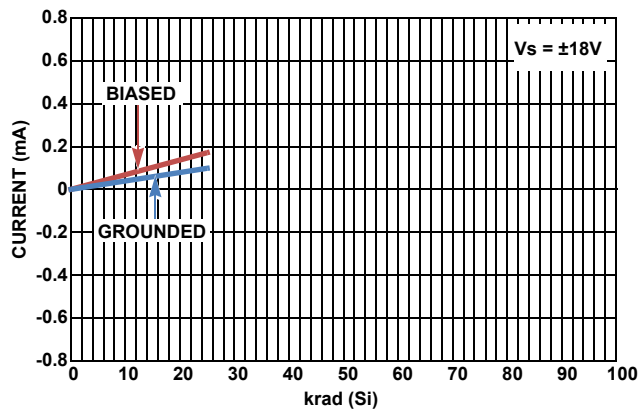


FIGURE 59.  $I^-$  SHIFT vs LOW DOSE RATE RADIATION

## Applications Information

### Functional Description

The ISL70444SEH contains four high speed and low power op amps designed to take advantage of its full dynamic input and output voltage range with rail to rail operation. By offering low power, low offset voltage, and low temperature drift coupled with its high bandwidth and enhanced slew rates upwards of 50V/μs, these op amps are ideal for applications requiring both high DC accuracy and AC performance. The ISL70444SEH is manufactured in Intersil's PR40 silicon-on-insulator process, which makes this device immune to Single Event Latch-up and provides excellent radiation tolerance. This makes it the ideal choice for high reliability applications in harsh radiation-prone environments.

### Operating Voltage Range

The devices are designed to operate with a split supply rail from ±1.35V to ±20V or a single supply rail from 2.7V to 40V. The ISL70444SEH is fully characterized in production for supply rails of 5V (±2.5V) and 36V (±18V). The Power Supply Rejection Ratio is typically 120dB over the full operating voltage range. The worst case common mode rejection ratio over temperature is within 1.5V to 2V of each rail. When  $V_{CM}$  is inside that range, the CMRR performance is typically >110dB with ±18V supplies. The minimum CMRR performance over the -55°C to +125°C temperature range and radiation is >70dB over the full common mode input range for power supply voltages from ±2.5V (5V) to ±18V (36V).

### Input Performance

The slew enhanced front end is a block that is placed in parallel with the main input stage and functions based on the input differential.

### Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series connected 600Ω current limiting resistors and an anti-parallel diode pair across the inputs.

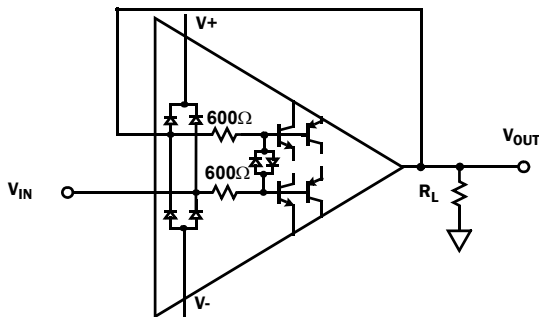


FIGURE 60. INPUT ESD DIODE CURRENT LIMITING, UNITY GAIN

### Output Short Circuit Current Limiting

The output current limit has a worst case minimum limit of ±8mA but may reach as high as ±100mA. The op amp can withstand a short circuit to either rail for a short duration (<1 second) as long as the maximum operating junction temperature is not violated. This applies to only one amplifier at a given time. Continued use of the device in these conditions may degrade the long term reliability of the part and is not recommended. Figure 20 shows the typical short circuit currents that can be expected. The ISL70444SEH's current limiting circuitry will automatically lower the current limit of the device if short circuit conditions carry on for extended periods in time in an effort to protect itself from malfunction, however extended operation in this mode will degrade the output rail-to-rail performance by increasing the  $V_{OH}/V_{OL}$  levels.

### Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL70444SEH is immune to output phase reversal, even when the input voltage is 1V beyond the supplies. This is illustrated in Figure 49.

### Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature ( $T_{JMAX}$ ) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} \times PD_{MAXTOTAL} \quad (EQ. 1)$$

where:

- $PD_{MAXTOTAL}$  is the sum of the maximum power dissipation of each amplifier in the package ( $PD_{MAX}$ )
- $PD_{MAX}$  for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad (EQ. 2)$$

where:

- $T_{MAX}$  = Maximum ambient temperature
- $\theta_{JA}$  = Thermal resistance of the package
- $PD_{MAX}$  = Maximum power dissipation of 1 amplifier
- $V_S$  = Total supply voltage
- $I_{qMAX}$  = Maximum quiescent supply current of 1 amplifier
- $V_{OUTMAX}$  = Maximum output voltage swing of the application

## Unused Channel Configuration

The ISL70444SEH is a quad op amp. If the application does not require the use of all four op amps, the user must configure the unused channels to prevent it from oscillating. Any unused channels will oscillate if the input and output pins are floating. This results in higher-than-expected supply currents and possible noise injection into any active channels being used. The proper way to prevent oscillation is to short the output to the inverting input, and ground the positive input (Figure 61).

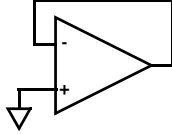


FIGURE 61. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

# ISL70444SEH

## Die Characteristics

### Die Dimensions

2410 $\mu$ m x 3175 $\mu$ m (80mils x 101mils)  
Thickness: 483 $\mu$ m  $\pm$  25 $\mu$ m (19mils  $\pm$  1 mil)

### Interface Materials

#### GLASSIVATION

Type: Nitrox  
Thickness: 15k $\text{\AA}$

#### TOP METALLIZATION

Type: AlCu (99.5%/0.5%)  
Thickness: 30k $\text{\AA}$

#### BACKSIDE FINISH

Silicon

#### PROCESS

PR40

## Assembly Related Information

### SUBSTRATE POTENTIAL

Floating

### ADDITIONAL INFORMATION

#### WORST CASE CURRENT DENSITY

$< 2 \times 10^5$  A/cm<sup>2</sup>

#### TRANSISTOR COUNT

730

### Weight of Packaged Device

0.5952 Grams (Typical)

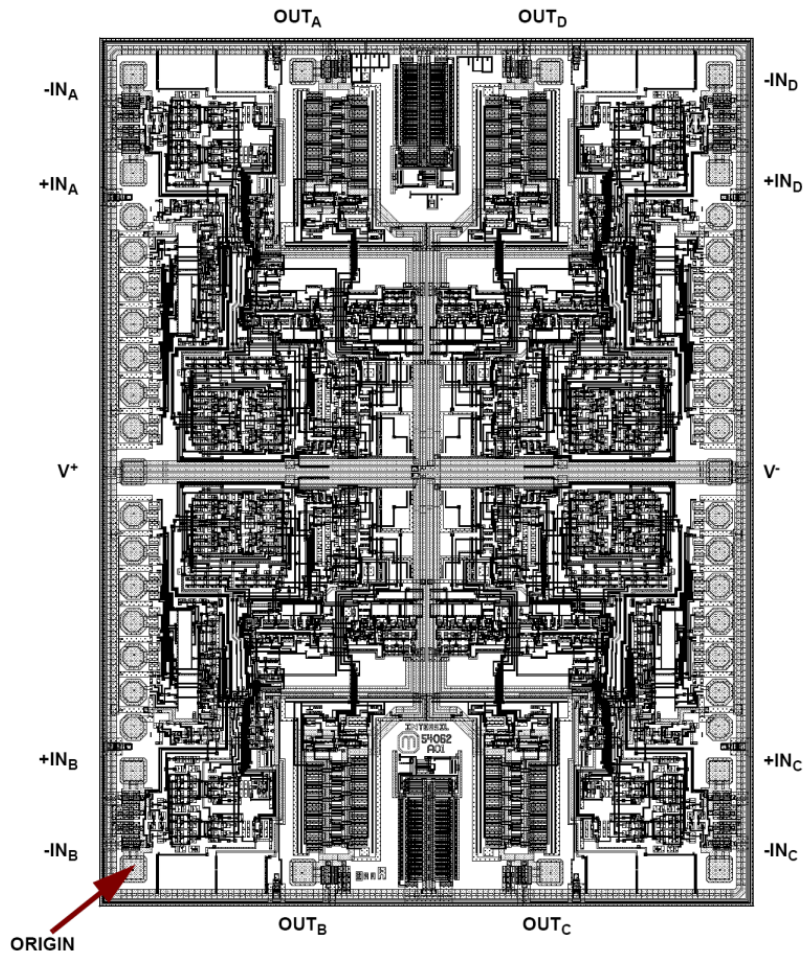
### Lid Characteristics

Finish: Gold

Potential: Unbiased, tied to E-pad under package

Case Isolation to Any Lead:  $20 \times 10^9 \Omega$  (min)

## Metallization Mask Layout



# ISL70444SEH

TABLE 1. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (μm)	Y (μm)	dX (μm)	dY (μm)	BOND WIRES PER PAD
OUT <sub>B</sub>	2	599.0	-11.5	70	70	1
OUT <sub>C</sub>	3	1472.0	-11.5	70	70	1
-IN <sub>C</sub>	4	2071.0	0.0	70	70	1
+IN <sub>C</sub>	12	2071.0	347.5	70	70	1
V <sup>-</sup>	20	2071.0	1406.5	70	70	1
+IN <sub>D</sub>	21	2071.0	2465.5	70	70	1
-IN <sub>D</sub>	22	2071.0	2813.0	70	70	1
OUT <sub>D</sub>	23	1472.0	2824.5	70	70	1
OUT <sub>A</sub>	24	599.0	2824.5	70	70	1
-IN <sub>A</sub>	25	0.0	2813.0	70	70	1
+IN <sub>A</sub>	33	0.0	2465.5	70	70	1
V <sup>+</sup>	41	0.0	1406.5	70	70	1
+IN <sub>B</sub>	42	0.0	347.5	70	70	1
-IN <sub>B</sub>	1	0.0	0.0	70	70	1

NOTE:

8. Origin of coordinates is the centroid of pad 42, "IN-B".

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
June 14, 2013	FN8411.1	Changed Radiation tolerance High dose rate from 100krad(Si) to 300krad(Si) on page 1 features and in Electrical Spec Table conditions on pages 7 and 8. Added SR spec for V <sub>S</sub> = ±18V to Electrical Spec Table on page 7. Removed Max limit of 300 for V <sub>OS</sub> Offset Voltage in V <sub>S</sub> = ±18V, V <sub>S</sub> = ±2.5V and V <sub>S</sub> = ±1.5V Spec tables.
May 23, 2013	FN8411.0	Initial Release.

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For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at [www.intersil.com](http://www.intersil.com). You may report errors or suggestions for improving this datasheet by visiting [www.intersil.com/en/support/ask-an-expert.html](http://www.intersil.com/en/support/ask-an-expert.html). Reliability reports are also available from our website at <http://www.intersil.com/en/support/qualandreliability.html#reliability>

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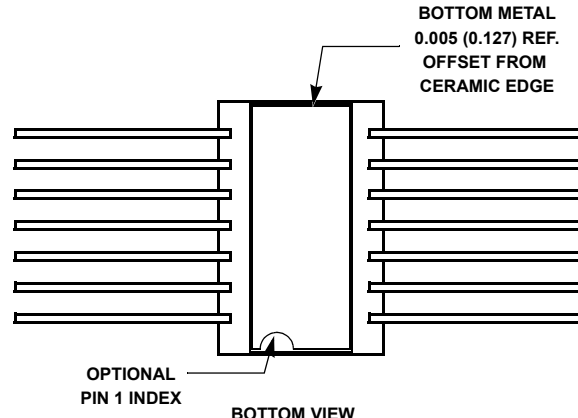
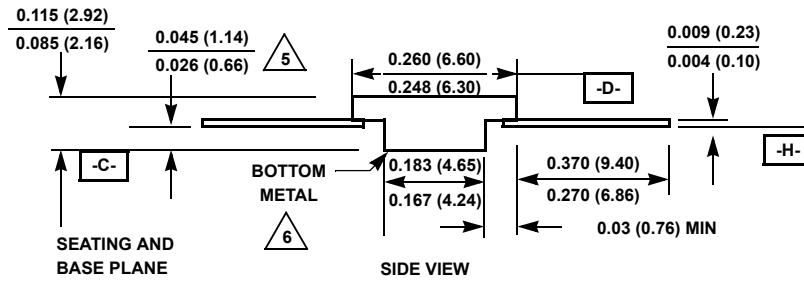
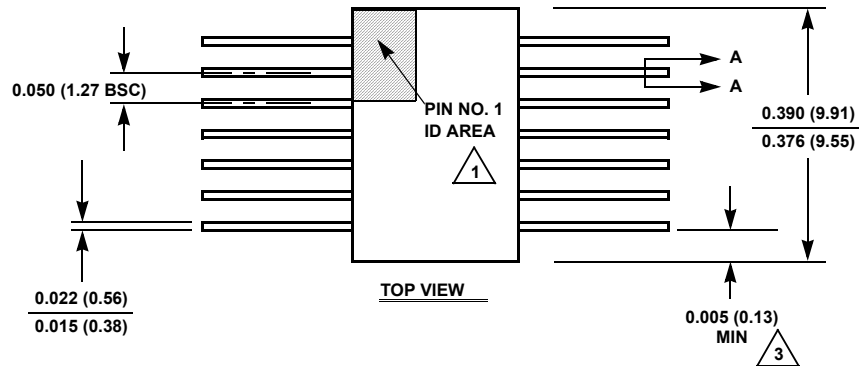
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## Package Outline Drawing

### K14.C

14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 0, 9/12



#### NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Measure dimension at all four corners.
4. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
5. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
6. The bottom of the package is a solderable metal surface.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Dimensions: INCH (mm). Controlling dimension: INCH.

