2Mx32 5V FLASH MODULE *ADVANCED**

FEATURES

- Access Time of 90, 120, 150nS
- Packaging:
  - 66-pin, PGA Type, 1.185 inch square, Hermetic Ceramic HIP (Package 401).
  - 68 lead, 40mm Low Profile CQFP (Package 502), 3.5mm (0.140 inch)
  - 68 lead, Hermetic CQFP (G2), 22.4mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3)
- Sector Architecture
  - 32 equal size sectors of 64KBytes per each 2Mx8 chip
  - Any combination of sectors can be erased. Also supports full chip erase.
- Minimum 100,000 Write/Erase Cycles Minimum (0°C to 70°)
- Organized as 2Mx32
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write. 5V ± 10% Supply.
- Low Power CMOS
- $\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- $\overline{\text{RESET}}$ pin resets internal state machine to the read mode.
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation, Seperate Power and Ground Planes to improve noise immunity

* *This data sheet describes a product that may or may not be under development, and is subject to change or cancellation without notice.*

Note: Programming information available upon request.

FIG. 1 PIN CONFIGURATION FOR WF2M32-XHX5

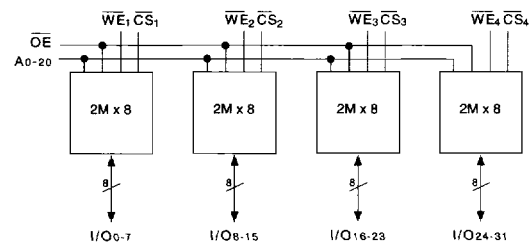
TOP VIEW

1	12	23		34	45	56
I/O8	$\overline{\text{WE2}}$	I/O15		I/O24	Vcc	I/O31
I/O9	$\overline{\text{CS2}}$	I/O14		I/O25	$\overline{\text{CS4}}$	I/O30
I/O10	GND	I/O13		I/O26	$\overline{\text{WE4}}$	I/O29
A14	I/O11	I/O12		A7	I/O27	I/O28
A16	A10	$\overline{\text{OE}}$		A12	A4	A1
A11	A9	A17		A20	A5	A2
A0	A15	$\overline{\text{WE1}}$		A13	A6	A3
A18	Vcc	I/O7		A8	$\overline{\text{WE3}}$	I/O23
I/O0	$\overline{\text{CS1}}$	I/O6		I/O16	$\overline{\text{CS3}}$	I/O22
I/O1	A19	I/O5		I/O17	GND	I/O21
I/O2	I/O3	I/O4		I/O18	I/O19	I/O20
11	22	33		44	55	66

PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-20}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground

BLOCK DIAGRAM



$\overline{\text{RESET}}$ internally tied to Vcc in the HIP package for this pin configuration. See Alternate Pin Configuration with $\overline{\text{RESET}}$ tied to pin 12 for system control of reset (Fig. 11, page 13)

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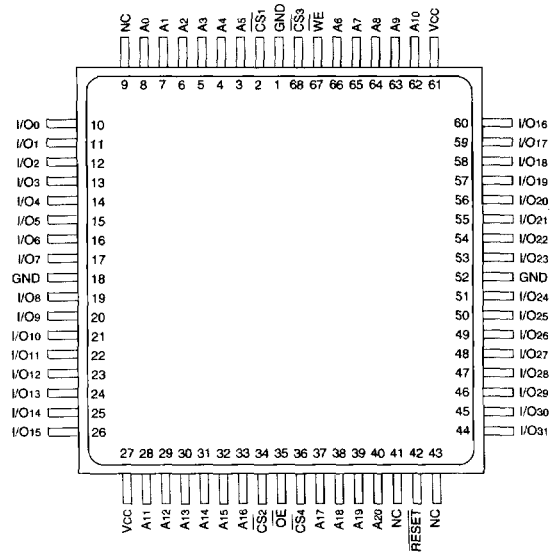
FIG. 2 PIN CONFIGURATION FOR WF2M32-XG4TX5

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-20	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
$\overline{RESET}$	Reset
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

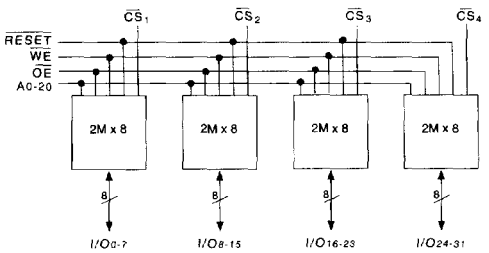
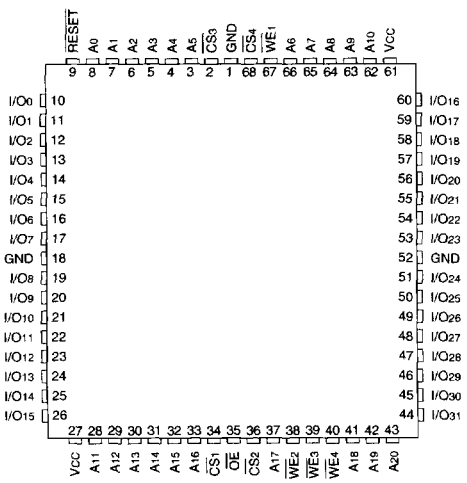
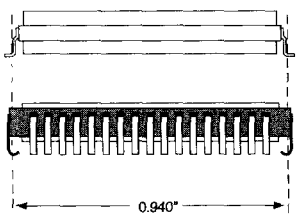


FIG. 3 PIN CONFIGURATION FOR WF2M32-XG2X5

TOP VIEW



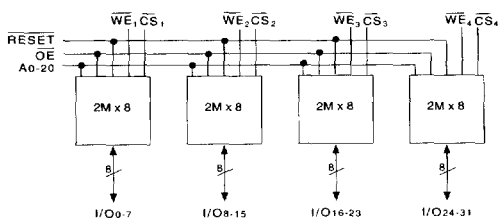


The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-20	Address Inputs
$\overline{WE}$1-4	Write Enables
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
$\overline{RESET}$	Reset

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-2.0 to +7.0	V
Power Dissipation	P_T	8	W
Storage Temperature	Tstg	-65 to +125	°C
Short Circuit Output Current	Ios	100	mA

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	-	+0.8	V
Operating Temperature (Mil.)	T_A	-55	-	+125	°C
Operating Temperature (Ind.)	T_A	-40	-	+85	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		pF
HIP (PGA)			20	
HIP (Alternate pinout)			50	
CQFP G4T			50	
CQFP G2			20	
G2 (Alternate pinout)			50	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LOx32}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		160	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}		240	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = 5.5, $\overline{CS}$ = V_{IH}, f = 5MHz, $\overline{RESET}$ = V_{CC} ± 0.3V		4.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 12.0 mA, V_{CC} = 4.5		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85xVcc		V
Low V_{CC} Lock-Out Voltage	V_{LKO}		3.2	4.2	V

NOTES:

1. The Icc current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with OE at $\overline{V_{IH}}$.
2. Icc active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		nS
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		nS
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		50		50		nS
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		nS
Data Setup Time	t_{DVWH}	t_{DS}	45		50		50		nS
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		nS
Address Hold Time	t_{WLAX}	t_{AH}	45		50		50		nS
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		nS
Duration of Byte Programming Operation	t_{WHWH1}			1		1		1	mS
Sector Erase	t_{WHWH2}			15		15		15	Sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		µS
Vcc Setup Time	t_{VCS}		50		50		50		µS
Chip Programming Time				100		100		100	Sec
Output Enable Hold Time (1)		t_{OEH}	10		10		10		nS
Chip Erase Time				480		480		480	Sec
$\overline{RESET}$ Pulse Width (2)		t_{RP}	500		500		500		nS

1. For Toggle and Data Polling.
2. $\overline{RESET}$ internally tied to Vcc for the default pin configuration in the HIP package.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	90		120		150		nS
Address Access Time	t_{AVQV}	t_{ACC}		90		120		150	nS
Chip Select Access Time	t_{ELQV}	t_{CE}		90		120		150	nS
Output Enable to Output Valid	t_{GLQV}	t_{OE}		40		50		55	nS
Chip Select High to Output High Z (1)	t_{EHQZ}	t_{DF}		20		30		35	nS
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		30		35	nS
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		nS
RST Low to Read Mode (1,2)		t_{Ready}		20		20		20	µS

1. Guaranteed by design, not tested.
2. $\overline{RESET}$ internally tied to Vcc for the default pin configuration in the HIP package.

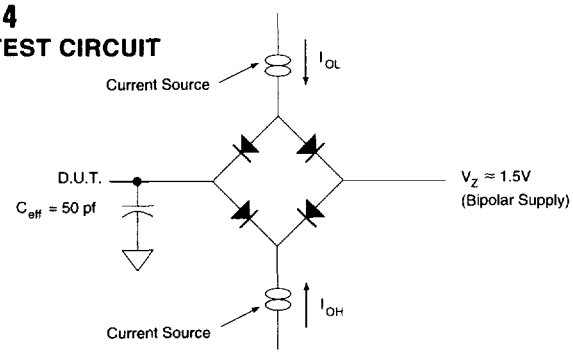
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		nS
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		nS
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		nS
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		nS
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		nS
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		nS
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		nS
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		nS
Duration of Byte Programming Operation	t_{WHWH1}			1		1		1	mS
Sector Erase Time	t_{WHWH2}			15		15		15	Sec
Read Recovery Time	t_{GHEL}		0		0		0		µS
Chip Programming Time				100		100		100	Sec
Chip Erase Time				480		480		480	Sec
Output Enable Hold Time (1)		t_{OEH}	10		10		10		nS

1. For Toggle and Data Polling.

FIG. 4
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 .
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 5
RESET TIMING DIAGRAM

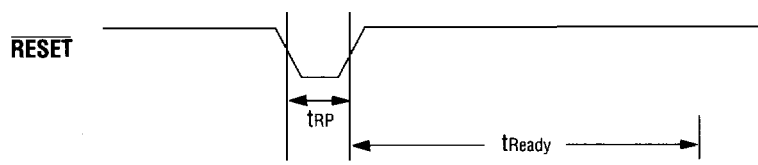


FIG. 6
AC WAVEFORMS FOR READ OPERATIONS

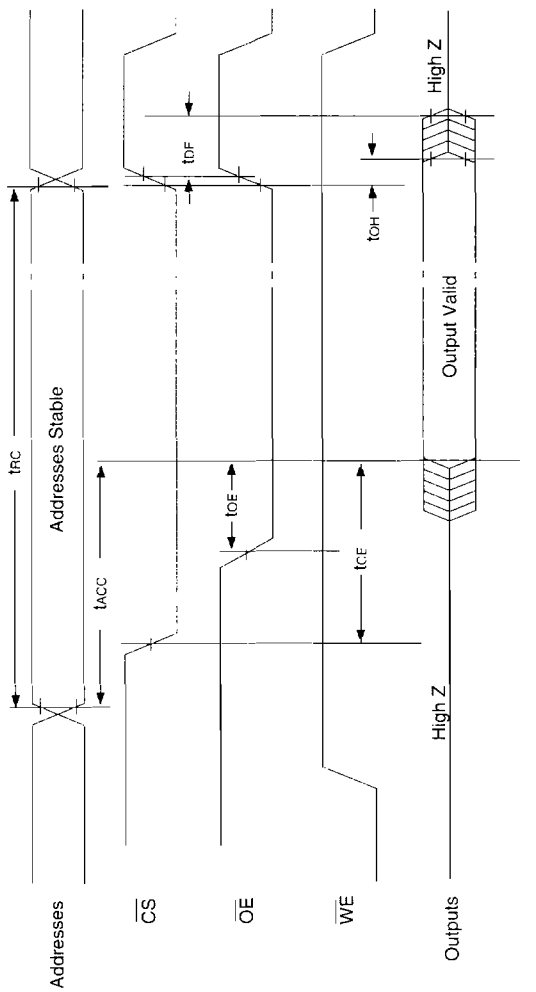
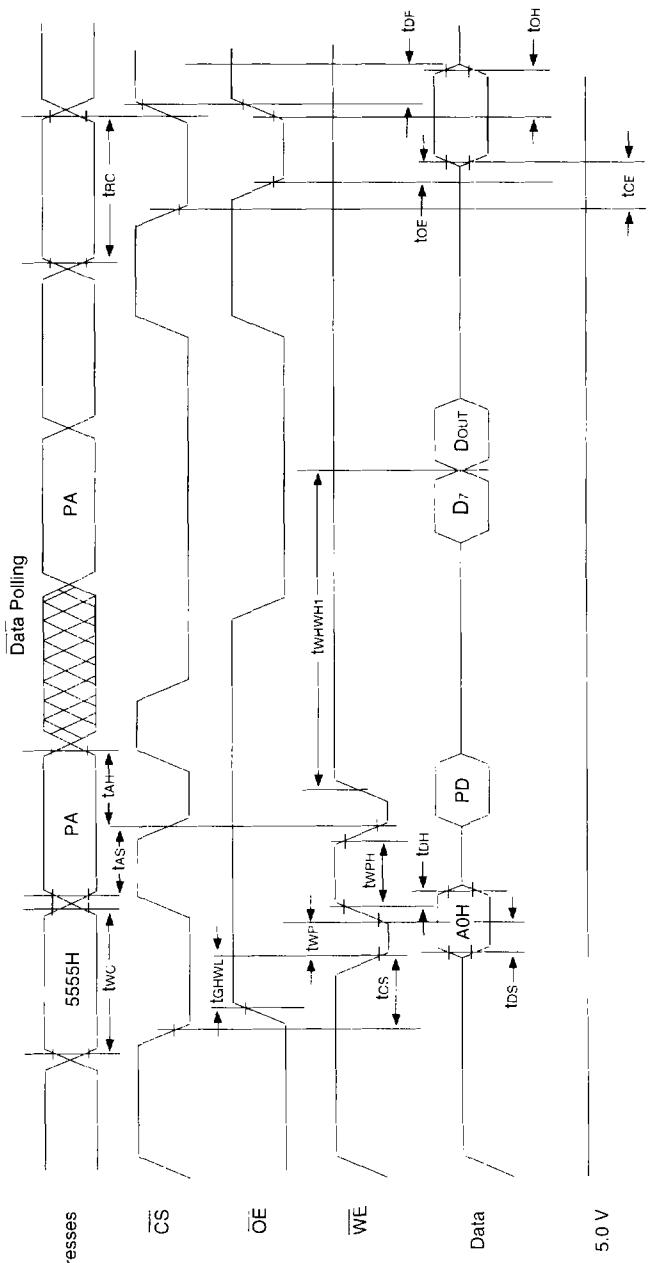


FIG. 7
WRITE/ERASE/PROGRAM OPERATION, $\overline{WE}$ CONTROLLED



NOTES:
1. PA is the address of the memory location to be programmed
2. PD is the data to be programmed at byte address.
3. $\overline{D_7}$ is the output of the complement of the data written to each chip
4. D_{OUT} is the output of the data written to the device
5. Figure indicates last two bus cycles of four bus cycle sequence

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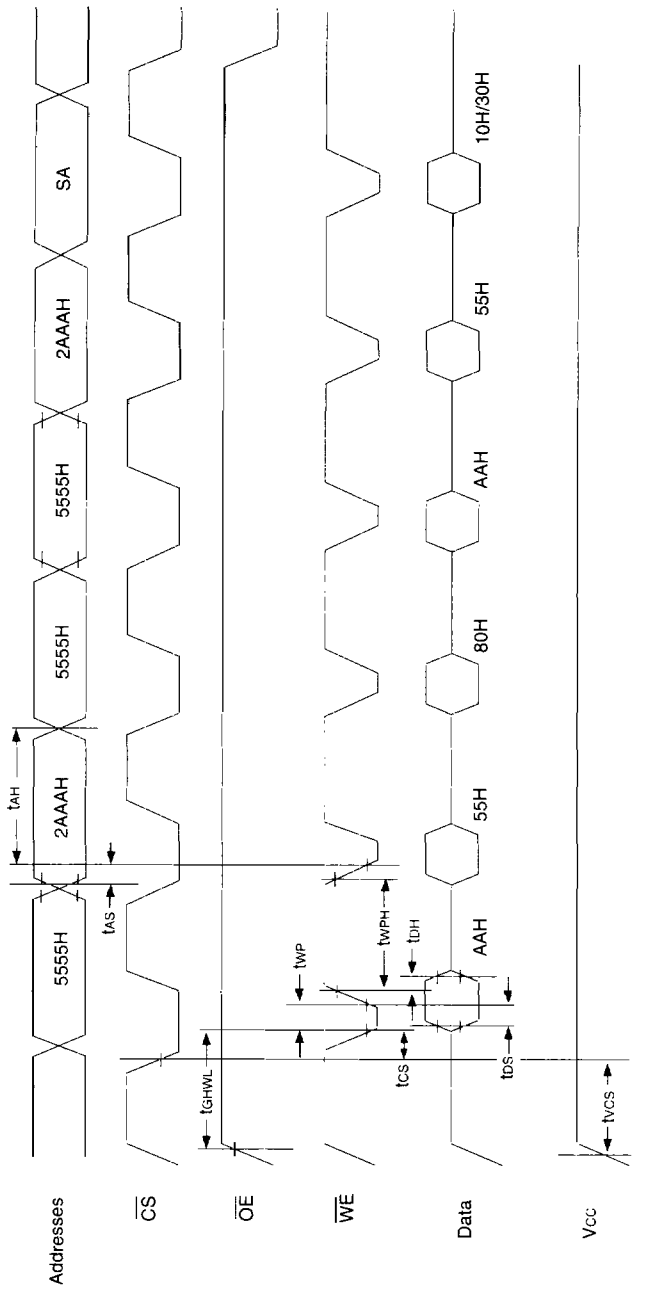
FIG. 8
AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTE:
1 SA is the sector address for Sector Erase

FIG. 9
AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS

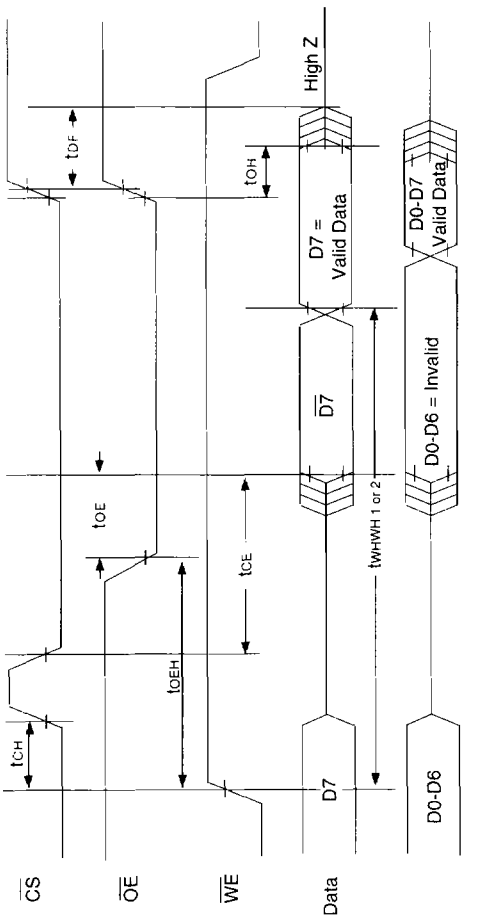
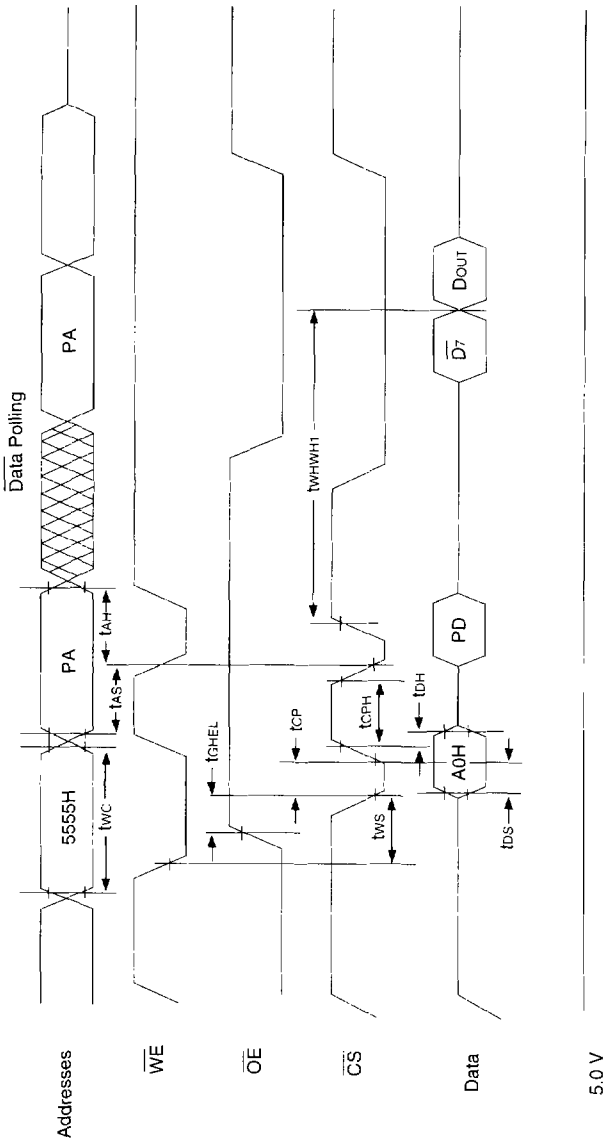


FIG. 10
ALTERNATE $\overline{CS}$ CONTROLLED PROGRAMMING OPERATION TIMINGS



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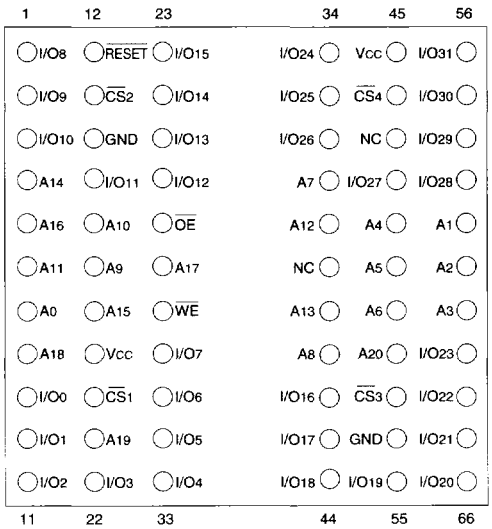
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

FIG. 11 ALTERNATE PIN CONFIGURATION FOR WF2M32I-XHX5

TOP VIEW



PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-20}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground
$\overline{RESET}$	Reset

BLOCK DIAGRAM

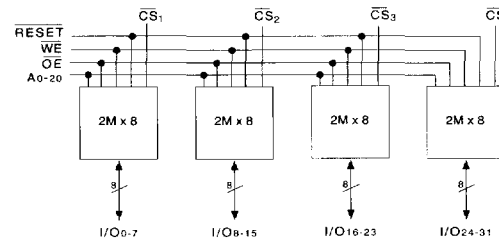
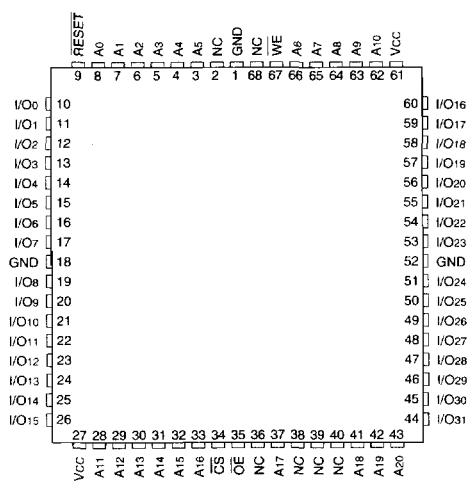
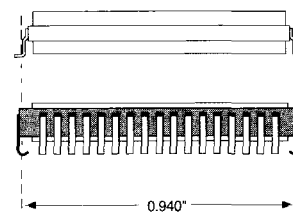


FIG. 12 ALTERNATE PIN CONFIGURATION FOR WF2M32U-XG2X5

TOP VIEW





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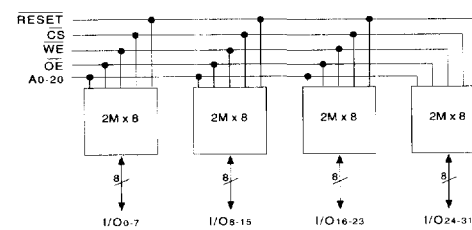
I/O_{0-31}	Data Inputs/Outputs
A_{0-20}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground
$\overline{RESET}$	Reset

BLOCK DIAGRAM



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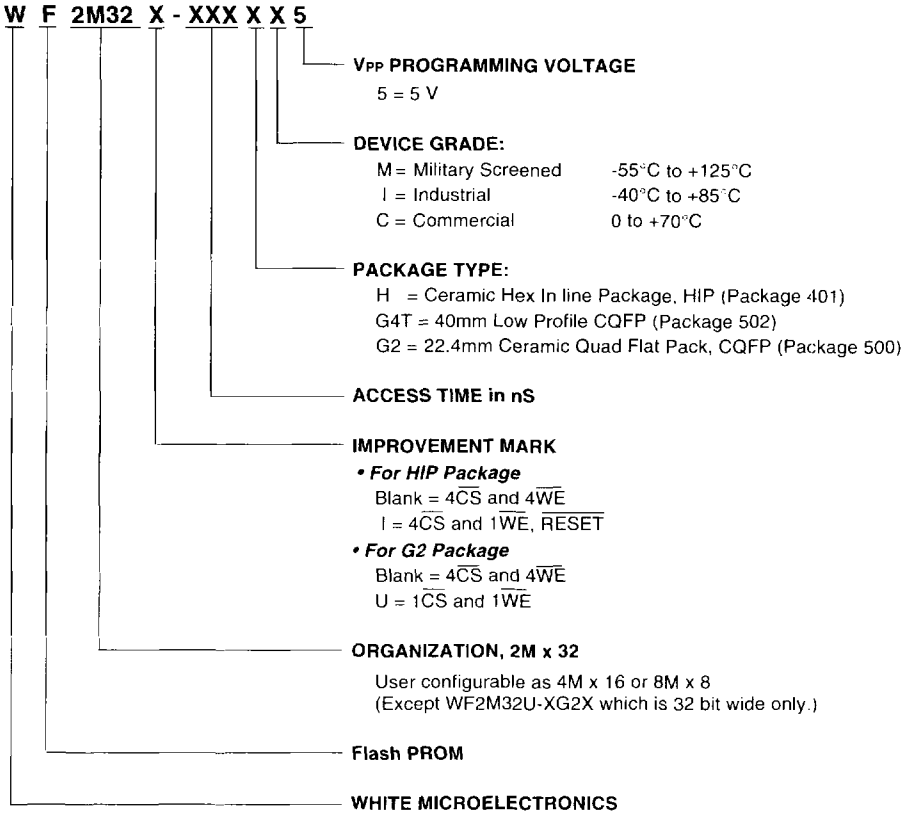
ORDERING INFORMATION



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