SPARC Technology Business

Preliminary

STP5010A

November 1994

50 MHz SuperSPARC MBus Module™

DATA SHEET — SuperSPARC Only MBus Module

DESCRIPTION

The STP5010A is one of the members of the SuperSPARC based MBus module products. The STP5010A is designed with the latest high performance superscalar SuperSPARC (STP1020A) microprocessor. This module is aimed at low end applications, and is designed without the External Cache subsystem. The SuperSPARC integrates integer and floating point execution units, memory management unit (MMU), large level-1 instruction and data caches (total of 36 KBytes of cache memory), and the MBus interface to integrate with rest of the system. Along with the SuperSPARC CPU, the STP5010A module also consists of a voltage regulator module that maintains the supply voltage within the required tolerance.

Features

- High performance SuperSPARC CPU module with 50 MHz operating frequency
- Implements 50 MHz MBus
- Cache coherency support for multi-processing
- On-board voltage regulator module
- MBus compliant module design
- Fully tested CPU module
- 3.3 in x 5.776 in (8.38 cm x 14.67 cm) form factor
- MBus is implemented on 100-pin Fujitsu / AMP Microstrip connector

Benefits

- Delivers 69 SpecInt92, 79 SpecFp92, and 136 Dhrystone MIPS
- Provides 25% improvement over 40 MHz MBus
- Allows a wide range of scalable systems to be built
- Eliminates complicated external voltage regulator
- Removes Customer's CPU subsystem Design Cycle
- Reduces customers Testing Operations, allows faster Time to Market
- Small Foot Print. Same as SBus form factor
- High performance impedance controlled connector

TYPICAL STP5010A APPLICATIONS

The STP5010A is intended for use in a broad range of applications from uniprocessor desktop machines to large multiprocessor servers. A variety of high performance embedded applications can also be built around STP5010A module and take advantage of its flexibility, scalability, and ease of design. A block diagram of a system with STP5010A interfacing directly with the rest of the system is shown in *Figure 1.*

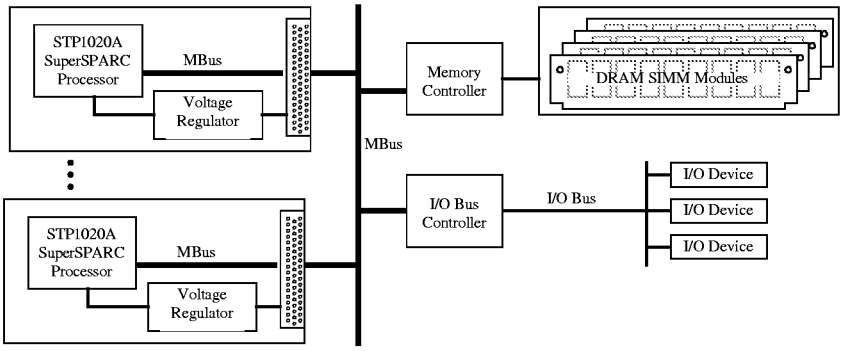


Figure 1. Typical STP5010A Uniprocessor / Multiprocessor MBus System

MBUS DESCRIPTION

MBus is a SPARC International standard bus designed to function as a processor-independent bus between one or more processors and memory. It is a 64-bit multiplexed high-performance bus. It is fully synchronous with all the transfers controlled by an MBus clock. It supports block transfers in sizes up to 128 bytes. All transactions on the MBus are arbitrated by an external arbiter. The arbitration algorithm is not included in the MBus definition to allow flexibility in system design. MBus is defined for uniprocessor and multiprocessor systems. The uniprocessor form of MBus is termed "Level1", and the multiprocessor version is called "Level2". The STP5010A can operate in either Level1 or Level2.

PCB BOARD

The PCB construction is designed to minimize impedance mismatches between boards in a system. The specification is 50 ohm ±10% impedance on all signal layers, and the signal propagation speed is 180 ps/ inch with a tolerance of 20 ps/ inch. The MCLK0 signal is an input to the module and it has a trace length of 12.8 inches on the module. This is the length between the MBus connector and the STP1020A MCLK pin. Adhering to the MBus specification, this trace is intentionally laid out to provide a minimum offset of 2ns (maximum offset of 2.6ns) between the MBus connector and the STP1020A MCLK pin. The module has a form factor of 83.82mm (3.3") x 146.70mm (5.776").

MBUS CONNECTOR

The MBus connector is a high performance impedance controlled (50 ohm ±10%) connector. The connector has 100 signal pins and 20 additional pins (5 blades) for power and ground. The MBus connector has high reliability and can be installed easily. It has excellent electrical performance, i.e., transmission line characteristics with low capacitance and inductance. The connector also has two separate power and three separate ground blades with 1 nH inductance. The suppliers of this connector are Fujitsu (part number: FCN-264P100-G/ C) and AMP (part number: 121497-4). Mating connector to be used on the system board is also available Fujitsu and AMP (part number: 121340-4).

Following is the MBus signal pin definitions for the connector.

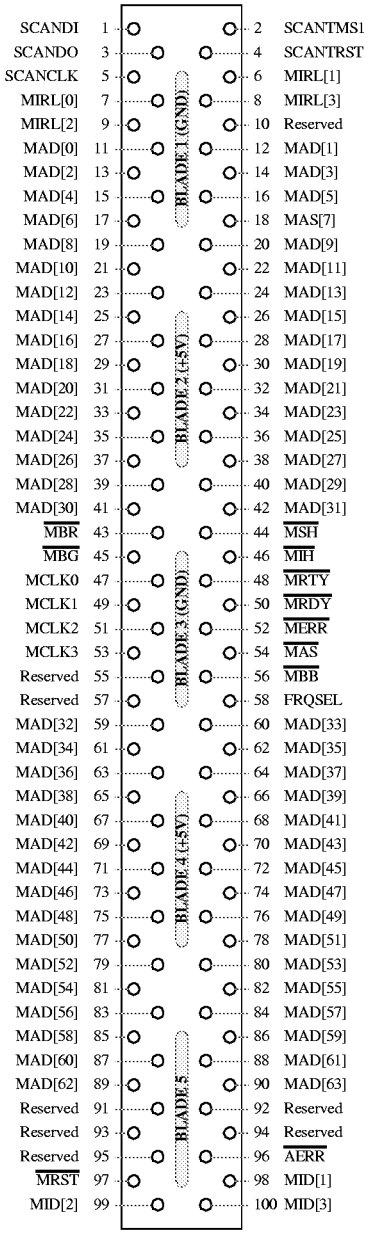


Figure 2. MBus Connector Pinout

STP5010A MODULE SIGNAL DESCRIPTIONS

Signal	Type	Description
$\overline{\text{AERR}}$ [1]	O	In error mode, the STP5010A will perform an automatic watchdog reset. Error mode is entered when any exception is taken with traps disabled (PSR.ET=0). This signal is driven only when asserted; otherwise, it is in tri-state. H = Normal operation. L = Error Mode.
FRQSEL	O	This signal, along with a jumper setting on the motherboard, is used by the Sun Microsystems SS20 system to determine the MBus speed. This signal is pulled low on the module. This allows the module to run at 50 MHz when the jumper on the mother board is set to 40/50 mode. In SS10s this module will run at 40 MHz.
MCLK[3:0]	I	MBus clock generated on the on the motherboard. MCLK0 mostly used.
MAD[63:00]	I/O	Multiplexed Command / Data.
$\overline{\text{MAS}}$	I/O	MBus address strobe. Asserted by the bus master when an MBus command word (containing address and control information) is on MAD63-MAD00. H = No command word. L = MBus command word on MAD63-MAD0.
$\overline{\text{MBB}}$	I/O	MBus busy. Asserted when there is any active transaction on MBus. H = MBus free. L = MBus busy.
$\overline{\text{MBG}}$	I	MBus grant. This is a dedicated (not bussed) signal from the MBus arbiter to this bus master. H = Not granted. The STP5010A may not initiate an MBus transaction. L = Granted. The STP5010A may initiate an MBus transaction as soon as MBus is free.
$\overline{\text{MBR}}$	O	MBus request. This is a dedicated (not bussed) signal from the STP5010A to the MBus arbiter. H = No request. L = Requesting to initiate a transaction on MBus.
$\overline{\text{MERR}}$	I	MBus error. Encoded along with $\overline{\text{MRDY}}$ and $\overline{\text{MRTY}}$ to indicate acknowledge type (the type of error response).
MID[3:1]	I	MBus Module ID. The identifier of this MBus device. Usually hardwired by the system. MID3 is the Most Significant Bit (MSB).

$\overline{\text{MERR}}$	$\overline{\text{MRDY}}$	$\overline{\text{MRTY}}$	Description
H	H	H	Idle Cycle
H	H	L	Relinquish and Retry
H	L	H	Valid Data Transfer
H	L	L	Reserved
L	H	H	Bus Error (ERROR1)
L	H	L	Timeout Error (ERROR2)
L	L	H	Uncorrectable Error (ERROR3)
L	L	L	Retry

STP5010A MODULE SIGNAL DESCRIPTIONS

Signal	Type	Description
$\overline{\text{MIH}}$	I/O	Memory inhibit. Asserted by a snooping cache when it notices a coherent read of cache block it owns. Memory responds to this signal by ignoring the request. H = No memory inhibit. L = Inhibit memory. The snooping cache which asserted $\overline{\text{MIH}}$ will respond with the data in place of memory.
MIRL[3:0]	I	Interrupt request level. This field specifies the level of the highest priority interrupt request that is currently pending. If MIRL3-MIRL0 = 0000, no interrupts are pending. Level 15 (MIRL3-MIRL0 = 1111) is a NMI (Non Maskable Interrupt) Level 14 Highest maskable interrupt Level 1 Lowest maskable interrupt Level 0 No interrupts are pending
$\overline{\text{MRDY}}$	I/O	MBus ready. Encoded along with $\overline{\text{MERR}}$ and $\overline{\text{MRTY}}$ to indicate acknowledgment type (the type of error response). See table in $\overline{\text{MERR}}$ description.
$\overline{\text{MRTY}}$	I	MBus retry. Encoded along with $\overline{\text{MERR}}$ and $\overline{\text{MRDY}}$ to indicate acknowledgment type (the type of error response). See table in $\overline{\text{MERR}}$ description.
$\overline{\text{MSH}}$ [1]	I/O	Memory shared. Asserted by a snooping cache when it notices a coherent read of a cache block it is caching. Both caches will mark the data as shared. H = No sharing. L = Shared data.
$\overline{\text{MRST}}$	I	Reset In. This causes an external reset for the STP5010A. At power-on, $\overline{\text{RSTIN}}$ must be held low for at least 100 ms to all allow the PLL to stabilize. If the PLL is known to be stable, $\overline{\text{RSTIN}}$ may be asserted for as short as 8 cycles. Any time V_{CC} is not within specification both SCANTMS2 (pin 4) and $\overline{\text{MRST}}$ (pin 97) must be asserted to avoid internal and external driver fights. Both internal and external driver fights might damage the chips. H = Normal operation. L = The STP5010A is externally reset.
Reserved	NA	These pins are not used by the module. Leave these pins floating.
SCANCLK	I	JTAG test clock input.
SCANDI	I	JTAG test data input.
SCANDO	O	JTAG test data output.
SCANTMS1	I	JTAG test mode select input.
$\overline{\text{SCANTRST}}$	I	JTAG test reset input.

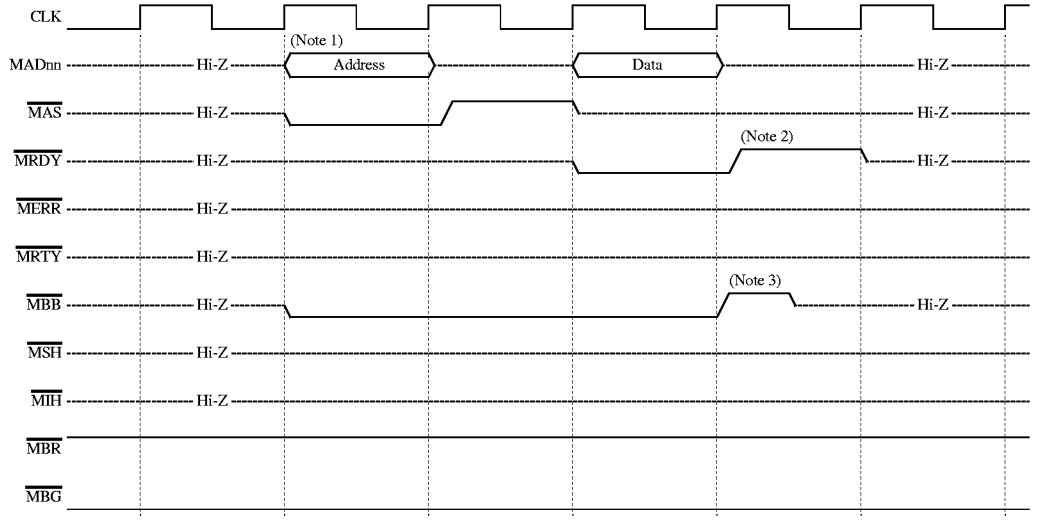
1. These pins have an open drain.

MBUS TIMING

The MBus read, write and invalidate operations are explained in the following section.

MBus Single Read

The single read cycle transfers a byte, half-word, word, or a double-word. Big-endian word ordering is used (the least significant bytes in a word appear on the high bits of the bus according to SPARC standard). *Figure 3* shows an MBus single read operation.

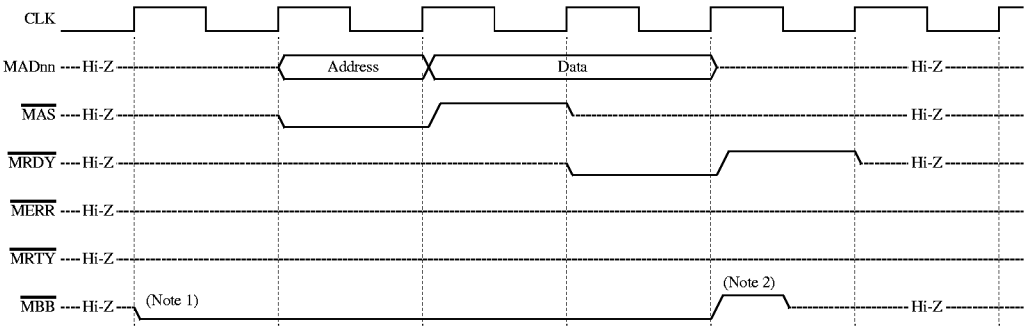


Notes: 1. MADnn lines are held to their previously driven state by system bus holders.
2. Control lines ($\overline{MAS}$, $\overline{MRDY}$, $\overline{MERR}$, $\overline{MRTY}$) are driven inactive for one clock before being released.
3. $\overline{MBB}$ is driven high for half clock cycle before being released.

Figure 3. MBus Single Read

MBus Single Write

Single write operations are queued in the store buffer. As soon as the module receives a bus grant, the transactions will be issued on the bus. The processor will not wait during this time, unless the buffer fills. Bytes, half-words, words, and double words may all be stored, with big-endian ordering. Any errors are reported as deferred data store errors. *Figure 4* shows an MBus single write operation.



Notes: 1. $\overline{\text{MBB}}$ is driven active one cycle before MAS during write and CI cycles.
2. $\overline{\text{MBB}}$ is driven inactive for half clock cycle before being released.

Figure 4. MBus Single Write

MBus Burst Read

Figure 5 shows a 32-byte burst read operation. A read operation can be performed on any size of data transfer that is specified by the SIZE bits. Read transactions support wrapping (critical-word- first ordering). Transactions involving fewer than eight bytes will have undefined data on the unused bytes.

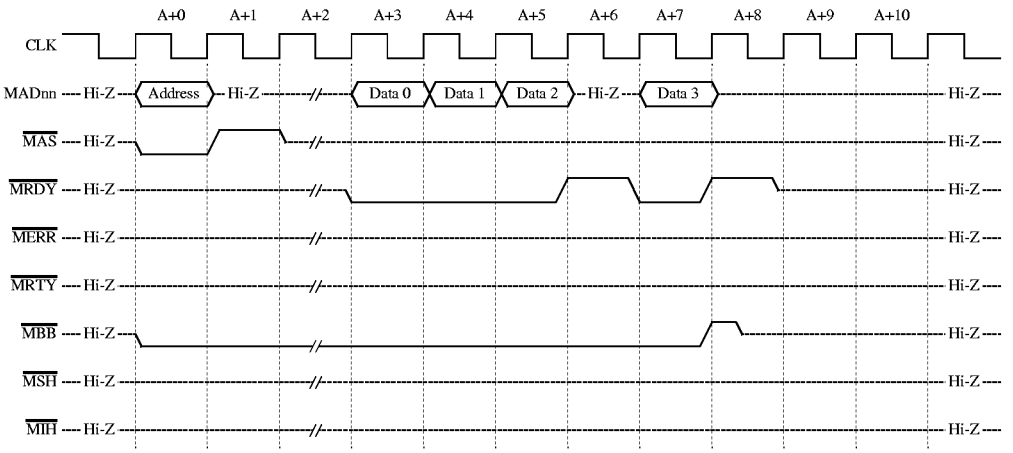
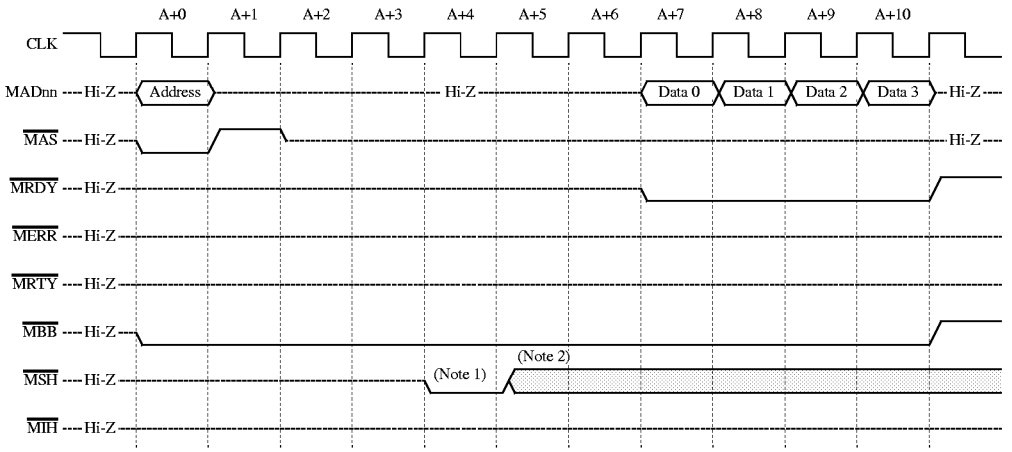


Figure 5. MBus Burst Read

MBus Coherent Read

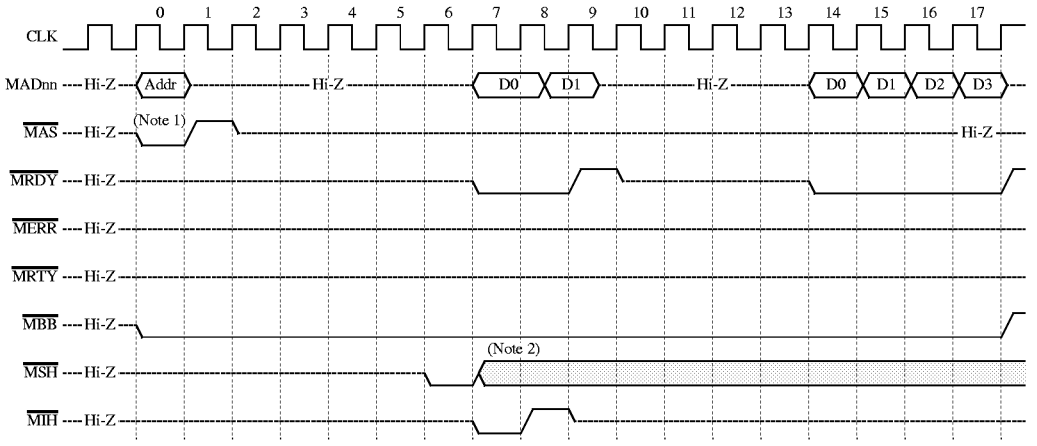
Coherent Read (CR) transactions are used to read data from the current owner. The owner may be memory or another cache. CR will be used for all on-board data cache load misses and all on-board instruction cache misses. If another cache owns the data, it will respond by asserting the $\overline{\text{MIH}}$ signal and providing the data. All CR transactions use critical-word-first ordering. The double-word that is needed first will be the starting address of the transaction. Double-words from memory must be returned in modulo 32-byte address order. Once the needed data arrives, the processor will use it immediately. *Figure 6* shows an MBus coherent read of shared data. Any processor that has a valid cached copy of data referenced by CR transactions must assert the $\overline{\text{MSH}}$ signal to indicate that the information is shared. The module can accept the assertion of $\overline{\text{MSH}}$ at any time until receipt of the first data word. If the data is owned by another cache, the module will ignore any data ready responses until four cycles beyond the assertion of $\overline{\text{MIH}}$. This allows memory controllers to begin transmitting data sooner. Memory control-

lers must not respond with data until a time equal to the maximum $\overline{MIH}$ assertion delay for any cache in the system. *Figure 7* shows an MBus coherent read of owned data.



Notes: 1. $\overline{MSH}$ may occur from A+2 to A+7.
2. $\overline{MSH}$ is an open drain signal. It is not driven inactive. The system pull-up resistor returns it to an inactive level.

Figure 6. MBus Coherent Read of Shared Data



Notes: 1. Device is not the Master.
2. $\overline{MSH}$ is an open drain signal. It is not driven inactive. The system pull-up resistor returns it to an inactive level.

Figure 7. MBus Coherent Read of Owned Data

MBus Coherent Invalidate

A Coherent Invalidate (CI) operation can only be performed on a block (32 bytes). All CI operations will be snooped by all snooping caches. If a Coherent Invalidate operation hits in a cache, that copy will be invalidated immediately, regardless of its state. Memory is responsible for the acknowledgment of the CI transaction. *Figure 8* shows a CI operation.

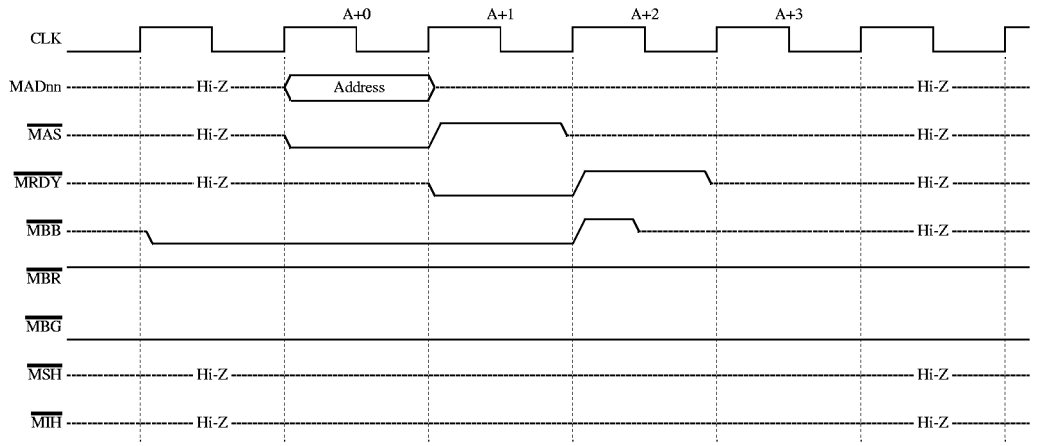


Figure 8. MBus Coherent Invalidate

Coherent Read and Invalidate

Since the MBus supports a write-invalidate type of cache-consistency protocol, a special Coherent Read and Invalidate (CRI) transaction that combines a CR transaction with the CI transaction was included to reduce the number of MBus Coherent transactions,. Caches that are performing CR transactions with the knowledge that they intend to immediately modify the data can issue this transaction.

Each CRI transaction will be snooped by all system caches. If the address hits and the cache does not own the block, that cache immediately invalidate its copy of this block, no matter what state the data was in. If the address hits and the cache owns the block, the block will assert $\overline{\text{MIH}}$ and supply the data. When the data has been successfully supplied, the cache will then invalidate its copy of this block.

$\overline{\text{MSH}}$ is not driven during the CRI transaction.

Coherent Write and Invalidate

A Coherent Write and Invalidate transaction combines a block write transaction with a CI transaction.

Each Coherent Write and Invalidate transaction will be snooped by all system caches. If the address hits, caches will invalidate their copies of this block, no matter what state the data was in. Neither $\overline{\text{MIH}}$ nor $\overline{\text{MSH}}$ is asserted for Coherent Write and Invalidate transactions. *Figure 9* shows a Coherent Write and Invalidate operation.

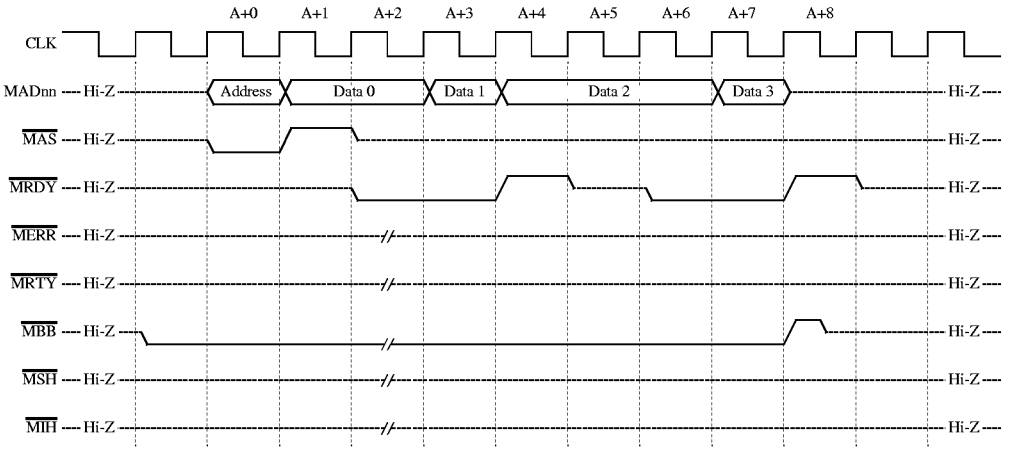


Figure 9. MBus Coherent Write and Invalidate

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

Symbol	Parameter	Rating	Units
V_{CC}	Supply voltage range	0 to 6	V
V_I	Input voltage range	-0.5 to V_{CC} + 0.5	V
V_O	Output voltage range	-0.5 to V_{CC} + 0.5	V
I_{IK}	Input clamp current ($V_I < 0$ or $V_I > V_{CC}$)	±20	mA
I_{OK}	Output clamp current ($V_O < 0$ or $V_O > V_{CC}$)	±50	mA
	Current into any output in the low state	96	mA
T_{STG}	Storage temperature	-65 to 150	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions "is not implied. Exposure to absolute -maximum-rated conditions may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{CC}	Supply voltage		4.75	5.0	5.25	V
V_{SS}	Ground		–	0	–	V
V_{IH}	Input high voltage		2.0	–	V_{CC} + 0.3	V
V_{IL}	Input low voltage		-0.3	–	0.8	V
I_{OH}	Output high current		–	–	-2.0	mA
I_{OL}	Output low current	All outputs except $\overline{MSH}$	–	–	2.2	mA
		$\overline{MSH}$	–	–	8.0	mA
T_A	Operating ambient temperature		0	–	40 [1]	°C

1. Maximum ambient temperature indicates that the maximum junction temperature T_J of 85°C is not exceeded in a part that is consuming the maximum power of 12.1 Watts (STP1020A only) with air flow of 300LFPM at 10,000 feet altitude.

Power Consumption

The SuperSPARC module has an on-board regulator and it can operate with a 5.0 V ± 5% power supply. The output of the regulator is 5.0 V ± 50mV. The worst case power consumption by the module is 11.25 Watts at 40 MHz, and 15.13 Watts for 50 MHz. The I_{CC} given in the DC Characteristics is measured at the input to the module. The power consumptions is dependent of the software running. The typical power consumption will be close to 75% of the maximum consumption.

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage [1]	I_{OH} = Max, V_{CC} = Min	2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = Max, V_{CC} = Max	–	–	0.4	V
I_{CC}	Supply current	V_{CC} = 5.25V, f=50 MHz $t_{w(VCLK)}$ or $t_{W(CLK)}$ = Min	2.9	–	3.2 [2]	A
I_{CCQ}	Quiescent power supply current	V_{CC} = Max, V_I = V_{SS} or V_{CC}	–	425	–	mA
I_{OZ}	High-impedance output current	V_{CC} = Max, V_O = 2.4V	–	–	20	µA
		V_{CC} = Max, V_O = 0.4V	–	–	-20	µA
I_I	Input current	V_I = V_{SS} to V_{CC}, Inputs with pullups	–	–	250	µA
		V_I = V_{SS} to V_{CC}, All other inputs	–	–	50	µA
C_I	Input capacitance [3]		–	10	–	pF
C_O	Output capacitance		–	15	–	pF

1. Open drain pins $\overline{\text{AERR}}$ and $\overline{\text{MSH}}$ not driven high.
2. The module power includes the power of the STP1020A and the regulator inefficiency (15.13 Watts / 4.75 = 3.19A).
3. This specification is provided as an aid to board design. This specification is not assured during manufacturing testing.

Timing Specifications

This section provides the timing specifications of the MBus. All Mbus signals are TTL level signals. The signals should be measured at 0.8V for high-to-low transition, and at 2.0V for low-to-high transition. The threshold for clock is 1.5V for the purposes of making timing measurements and calculations. For timing purpose the Mbus signal are grouped in the following manner.

Bussed control signals: $\overline{\text{MBB}}$, $\overline{\text{MAS}}$, $\overline{\text{MERR}}$, $\overline{\text{MRTY}}$, $\overline{\text{MRDY}}$, $\overline{\text{MIH}}$, $\overline{\text{MSH}}$.

Address/ Data lines: MAD<63:00>.

Point to Point control signals: $\overline{\text{MBR}}$, $\overline{\text{MBG}}$.

MID[3:1] are static signal and have no specified timing. MIRL[3:0], AERR are asynchronous signals. $\overline{\text{MSH}}$ and $\overline{\text{AERR}}$ are open drain signals.

AC Characteristics: Module Timing - Setup and Hold

Symbol	Parameter	Signals	50 MHz MCLK		Unit
			Min	Max	
t_{su}(MAD)	MBus MAD lines setup to CLK	MAD63-MAD0	3.8	–	ns
t_{su}(MC)	MBus bused setup to CLK	$\overline{\text{MAS}}$, $\overline{\text{MERR}}$, $\overline{\text{MRTY}}$, $\overline{\text{MRDY}}$, $\overline{\text{MBB}}$, $\overline{\text{MSH}}$, $\overline{\text{MIH}}$	4.0	–	ns
t_{su}(MIRL)	MBus IRL[3:0] setup to CLK	IRL[3:0]	5.0	–	ns
t_{su}(MBG)	MBus point-to-point setup to CLK	$\overline{\text{MBG}}$	4.8	–	ns
t_{h}(MAD)	MBus MAD lines hold from CLK	MAD63-MAD0	3.5	–	ns
t_{h}(MC)	MBus bused hold from CLK	$\overline{\text{MAS}}$, $\overline{\text{MRDY}}$, $\overline{\text{MBB}}$, $\overline{\text{MERR}}$, $\overline{\text{MRTY}}$, $\overline{\text{MSH}}$, $\overline{\text{MIH}}$	3.5	–	ns
t_{h}(MIRL)	MBus IRL[3:0] hold from CLK	IRL[3:0]	3.5	–	ns
t_{h}(MBG)	MBus Point-to-point hold from CLK	$\overline{\text{MBG}}$	3.5	–	ns

AC Characteristics: Module Timing - Switching Characteristics [1] [2]

Symbol	Parameter	50 MHz MCLK		Unit
		Min	Max	
t_p(MAD)	Propagation delay, CLK to MBus MAD63-MAD0	–	15.2	ns
t_p(MC)	Propagation delay, CLK to MBus control $\overline{MAS}$, $\overline{MRDY}$, $\overline{MBB}$, $\overline{MIH}$, $\overline{MSH}$	–	14.2	ns
t_p(MBR)	Propagation delay, CLK to MBus point-to-point $\overline{MBR}$	–	15.9	ns
t_{oh}(MAD)	Output hold time, CLK to MBus MAD63-MAD0	3.5	–	ns
t_{oh}(MC)	Output hold time, CLK to MBus control $\overline{MIH}$	3.5	–	ns
	Output hold time, CLK to MBus control $\overline{MAS}$, $\overline{MRDY}$, $\overline{MBB}$, $\overline{MSH}$	3.5	–	ns
t_{oh}(MBR)	Output hold time, CLK to MBus point-to-point $\overline{MBR}$	3.6	–	ns

1. Specification based on a lumped capacitive load of 50pf.
2. Timing specifications based on Spice simulations.

Clock Timing [1]

Symbol	Parameter	Min	Typ	Max	Unit
t_w(MBUS CLK)	MBus CLK pulse duration (50 Mhz)	20	–	–	ns
	MBus CLK duty cycle	25	50	75	%
t_w (SCAN CLK)	SCAN CLK pulse duration (10 MHz)	100	–	–	ns
	SCAN CLK duty cycle	–	50	–	%

1. This is for the PLL enabled. If the PLL is disabled, the part supports a fully static design. The timing parameters are not assured, since this is not tested.

JTAG and Miscellaneous Timing - Setup and Hold

Symbol	Parameter	Signal	10 MHz		Unit
			Min	Max	
t_{su}(SCAN TRST)	Setup to VCLK	$\overline{\text{SCANTRST}}$ (synchronous) [1]	20	–	ns
t_{su}(SCAN DI)	JTAG setup to SCAN CLK	SCANDI	20	–	ns
t_{su}(SCANTMS)	JTAG setup to SCAN CLK	SCANTMS	20	–	ns
t_h(SCAN TRST)	Hold from VCLK	$\overline{\text{SCANTRST}}$ (synchronous) [1]	20	–	ns
t_h(SCAN DI)	JTAG hold from SCAN CLK	SCANDI	20	–	ns
t_h(SCANTMS)	JTAG hold from SCAN CLK	SCANTMS	20	–	ns

1. SCAN RESET can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

JTAG and Miscellaneous Timing - Switching Characteristics

Symbol	Parameter	10 MHz		Unit
		Min	Max	
t_p(SCANDO)	SCAN CLK (falling edge) to SCANDO	2.5	25	ns

MECHANICAL SPECIFICATIONS

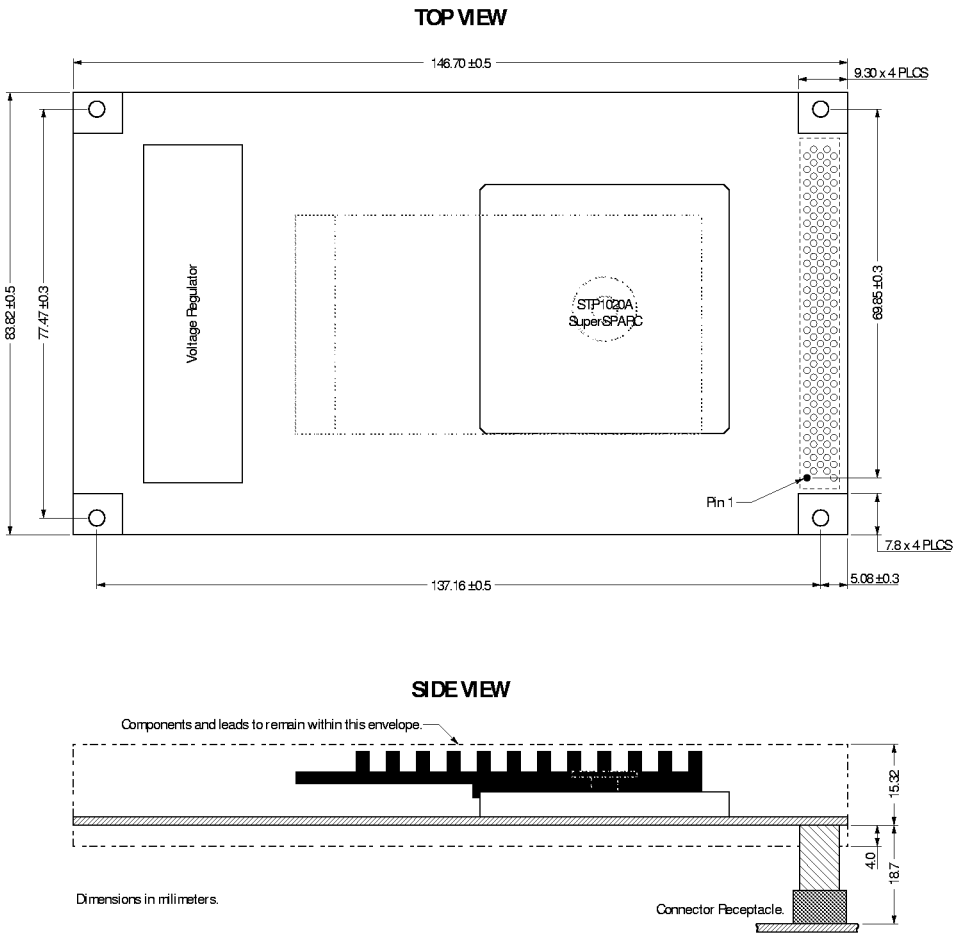
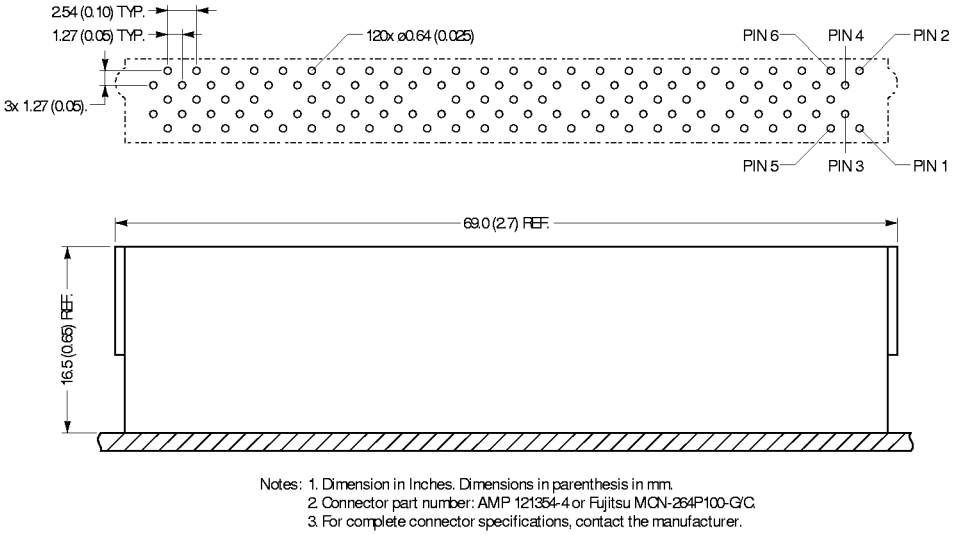


Figure 10. CPU Module Dimensions



Notes: 1. Dimension in Inches. Dimensions in parenthesis in mm.
2. Connector part number: AMP 121354-4 or Fujitsu MCN-264P100-G/C.
3. For complete connector specifications, contact the manufacturer.

Figure 11. CPU Module Connector (Detail Drawing)

ENVIRONMENTAL, SHOCK, & VIBRATION SPECIFICATION

Parameter	Specification
Operating Humidity	5% to 95% RH
Nonoperating Humidity	95% RH
Operating Altitude	63kPa, 10 C to 40 C
Nonoperating Altitude	17.3kPa, 0 C
Operating Shock	6 G, 11 msec, half-sine, 10 impacts/face
Nonoperating Shock	35 G, 11 msec, half-sine, 3 impacts/face
Operating Vibration	0.3 G peak, 2 sweeps of 5 to 500 to 5 Hz
Nonoperating Vibration	1.2 G peak, 2 sweeps of 5 to 500 to 5 Hz

The following additional test are performed during Engineering Qualification.

Parameter	Specification
Operating Temp. Soak Test	-5 C to 75 C, 20 C/min., 8 hrs. at each extreme.
Nonoperating Temp Soak Test	-40 C to 125 C, 20 C/min., 8 hrs at each extreme.
Operating Temp. Cycle Test	Twenty cycles of 0 to 60 °C, 20 °C / min., with ten minutes of dwell at 0 °C and 60 °C respectively.
Non-operating Temp. Cycle Test	Twenty cycles of -40 to 90 °C, 20m°C/min, with ten minutes of dwell at -40 °C and 90 °C respectively.
Non Operating Tri-Axial Random Vibration 20 to 2 kHz bandwidth	- 25 GRMS measured at center of test board for 10 minutes at 40, 25 and 85 °C
Operating Tri-axial Random Vibration 20 to 2 kHz bandwidth	- 25 GRMS measured at center of test board for 10 minutes at 0, 25 and 60 °C
Power Cycling tests	Apply voltage for 5 seconds on and 5 seconds off during twenty cycles of 0 to 60 °C, 20 °C/min., with five minutes of dwell at 0, 25 and 60 °C respectively.
Solder Reliability Tests	Non powered temperature cycling of 0 to 100 °C, 20 °C per minute change rate, 10 minute dwells at 0 °C and 100 °C, for 1000 cycles.

Note: The temperature and vibration, values and methodologies are derived from a combination of industrial component manufacture tests, Mil-Std 883 tests, IEC Tests, and from tests performed in Sun's Stress Lab.

Thermal Resistance vs. Air Flow [1] [2]

Symbol	Air Flow (ft./min)				
	100	**200**	**300**	**400**	**500**
θ_{CA} (°C/W)	5.6	4.0	3.1	2.5	2.2

1. T_J can be calculated by: $T_J = T_A + P_d(0.6 + \theta_{CA})$. Maximum T_J is 85°C.
2. The above θ_{CA} values are with pin-fin-type heat-sink.

ORDERING INFORMATION

Part Number	Speed	Description
STP5010AMBUS-50	50 MHz	50 MHz MBus module with STP1020A and a Voltage Regulator