H0438A

HUGHES AIRCRAFT COMPANY

Serial Input LCD Driver

MICROELECTRONICS CENTER

DESCRIPTION

Hughes H0438A is a CMOS/LSI circuit which drives an LCD display, usually under microprocessor control. The device acts as a smart peripheral, driving up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.

The H0438A can drive any standard or custom parallel drive LCD display whether it be field effect or dynamic scattering, 7, 9, 14 or 16 segment characters, decimals, leading + or −, or special symbols. Several H0438A's can be cascaded. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the LCDφ input, which controls the frequency of an internal oscillator.

The H0438A can also be used as a column driver in a multiplexed LCD display. In this application, timing and refresh must be supplied externally.

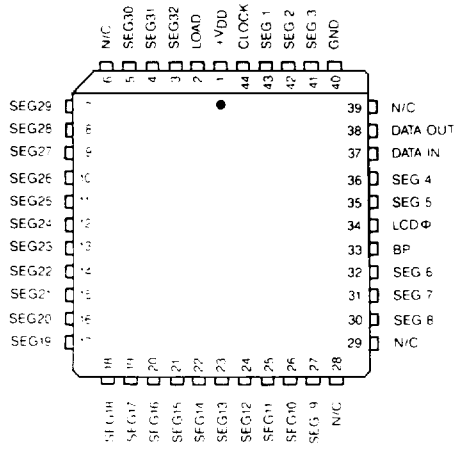
Hughes H0438A is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix), leadless chip carrier (L suffix), or surface mount quad package (Q suffix). Devices in chip form (H suffix) are available upon request. Commercial (HC prefix), Industrial (HI prefix) and Military (HB prefix) versions are available. The device designation, for example, of an industrial grade 0438A in a surface mount quad package is: HI0438A-Q.

FEATURES

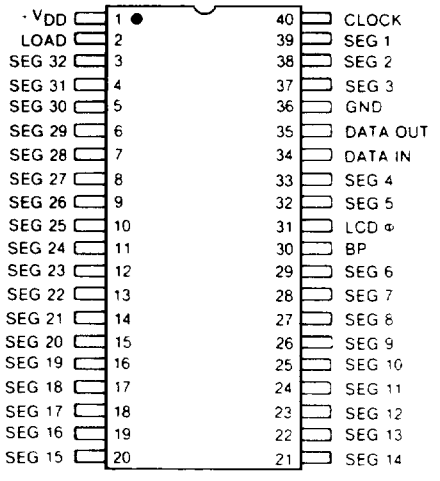
- Drives up to 32 LCD segments of arbitrary configuration
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and T²L compatible inputs
- Cascadable
- On-chip oscillator
- Requires only 3 control lines

PIN CONFIGURATION

Surface Mount Q Package



Dip Packages



ABSOLUTE MAXIMUM RATINGS

V_{DD} ..... −.3 to +13V
Inputs (Clk, Data In, Load) ..... V_{SS} −0.3V to V_{DD} + 0.3V
LCDφ Input ..... −.3V to + V_{DD} + .3V
Power Dissipation 250mW
Operating Temperature
  Plastic Package ..... −40 to +85°C
  Ceramic Package ..... −55 to +125°C
Storage Temperature ..... −65 to +150°C

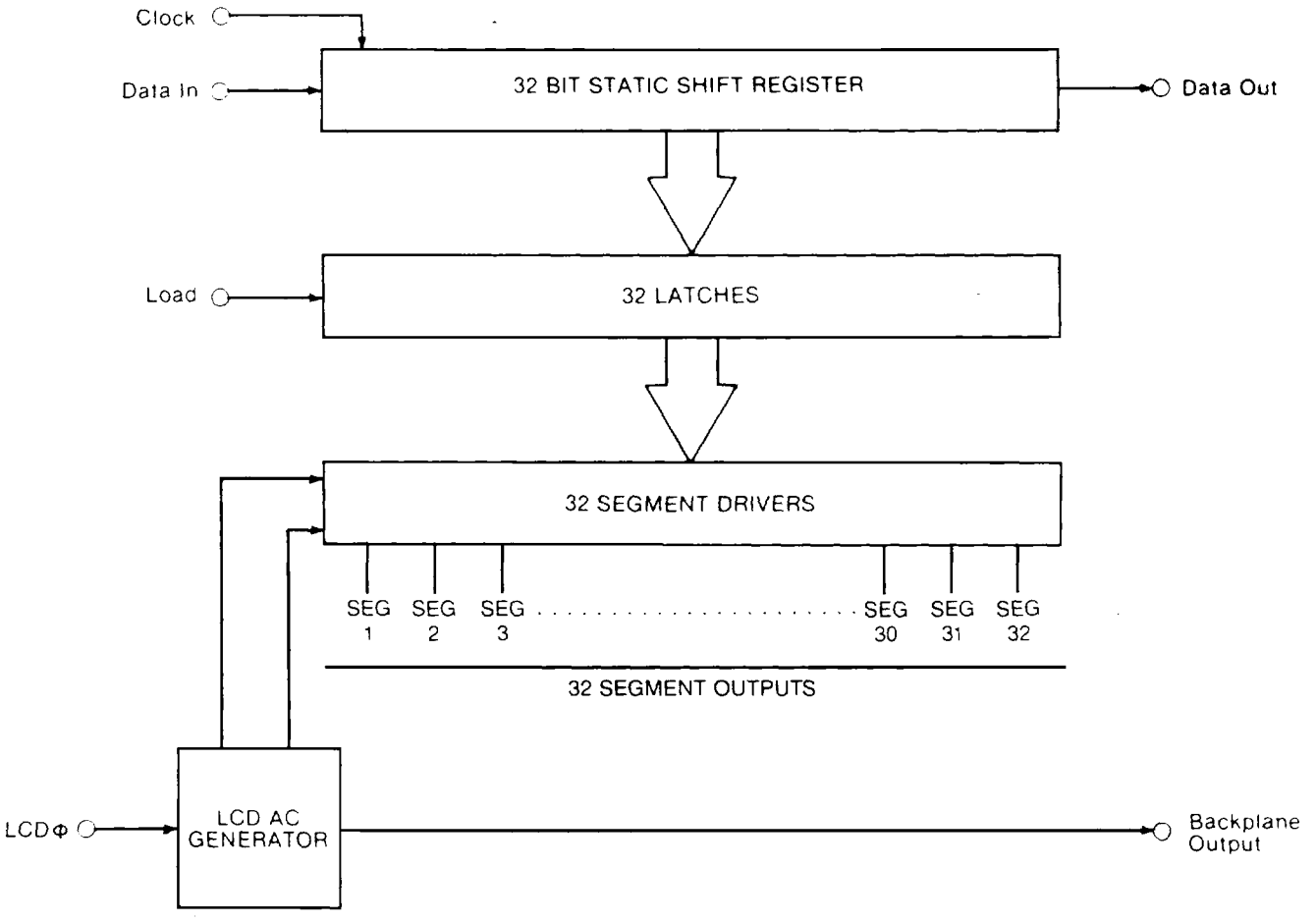
NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at T_A = −55 to 125°C, V_{DD} = 5v unless otherwise stated, C_L = 50pF

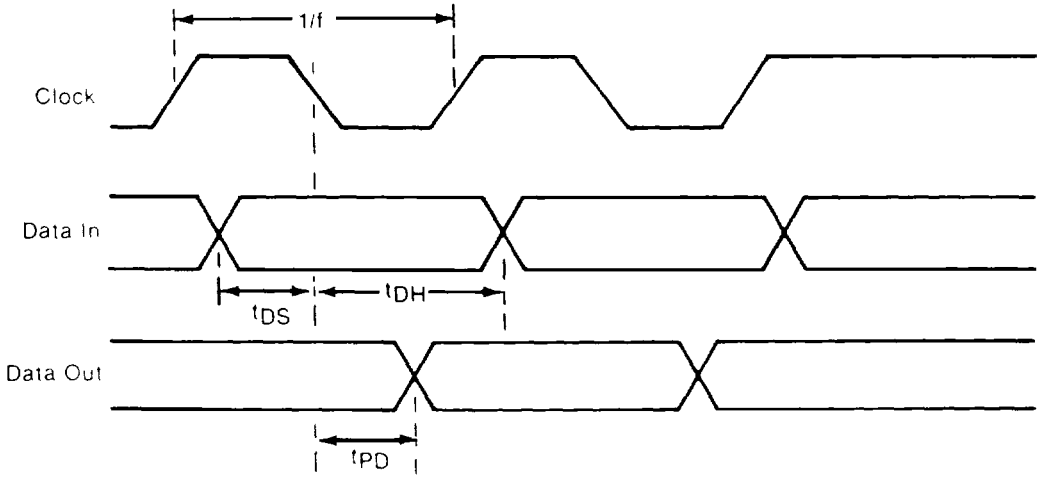
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	10	V
Supply Current [2]	I_{DD1}	LCDφ Osc < 15 KHz ,V_{DD} = 5v		60	µA
		V_{DD} = 12v		600	µA
Quiescent Current [2]	I_Q	V_{DD} = 5v		40	µA
		V_{DD} = 10v		265	µA
Input High Level (Clock, Data, Load)	V_{IH}		0.5V_{DD}	V_{DD}	V
Input Low Level (Clock, Data, Load)	V_{IL}		V_{DD} -1.3	0.2V_{DD}	V
Input Current [2] (Clock, Data, Load)	I_L	V_{DD} = 5v		20	µA
Input Capacitance [1] (Clock, Data, Load)	C_I			5	pf
Segment Output Impedance [2]	R_{ON}	I_L = 10µA		60	KΩ
Backplane Output Impedance [2]	R_{ON}			4	KΩ
Data-Out Output Impedance [2]	R_{ON}			4	KΩ
Clock Rate	f	50% Duty Cycle, V_{DD} = 10v	DC	1.0	MHz
Data Set-up Time	t_{DS}	Data change to Clk falling edge, V_{DD} = 10v	210		ns
Data Hold Time	t_{DH}	V_{DD} = 10v	70		ns
Load Pulse Width	t_{PW}	V_{DD} = 10v	245		ns
Data Out Prop. Delay	t_{PD}	C_L = 50pf. V_{DD} = 10v		700	ns
LCDφ Input High Level [2]	V_{IN}		0.9V_{DD}		V
LCDφ Input Low Level [2]	V_{IL}			0.1V_{DD}	V
LCDφ Input Current Level [2]	I_L	Driven		20	µA
LCDφ Capacitor (external) [1]	C_O	30 HZ		40 (approx)	pf
LCDφ Resistor (internal) [1]	R_O			1	MΩ

NOTE 1: Design assured but not tested.
NOTE 2: Parameters guaranteed by other tests at −55°C.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATING NOTES

1. The shift register loads, shifts, and outputs on the falling edge of Clock.
2. A logic 1 on Data In causes a segment to be visible.
3. A logic 1 on Load causes a parallel load of the data in the shift register into latches that control the segment drivers. The Load control is level sensitive and not edge sensitive.
4. If LCDφ is driven, it is in phase with the Backplane Output.
5. To cascade units, either connect Backplane of one circuit to LCDφ of all other circuits (thus one capacitor provides frequency control for all circuits) or connect LCDφ of all circuits to a common driving signal. If the former is chosen, tie just one Backplane to the LCD and use a different Backplane output to drive the LCDφ inputs. Either the data can be loaded to all circuits in parallel or Data Out can be connected to Data In to form a long serial shift register.
6. The supply voltage of the H0438A is equal to half the peak driving voltage of the LCD. If the H0438A supply voltage is less than the swing of the controlling logic signals, the positive supply leads of the logic circuitry and the H0438A should be tied in common, not the ground (or negative) supply leads. Be careful that input level specifications are met.
7. The LCDφ pin can be used in two modes, driven or oscillating. If LCDφ is driven, the circuit will sense this condition and pass the LCDφ input to the Backplane output. If the LCDφ pin is allowed to oscillate, its frequency is inversely proportional to capacitance (see Figure 1) and the LCD driving waveforms have a frequency 2^8 slower than the oscillator itself. The frequency is nearly independent of supply voltage. If LCDφ is oscillating, it is important to keep coupling capacitance to backplane and segments as low as possible. Similarly, it is recommended that the load capacitance on LCDφ be as large as is practical.
8. There are two obvious signal races to be avoided in this circuit, (1) changing Data In when Clock is falling, and (2) changing Load when Clock is falling.
9. The number of a segment corresponds to how many clock pulses have occurred since its data was present at the input. For example, the data on Seg 19 was input 19 clock pulses earlier.
10. It is acceptable to tie the Load line high. In this case the latches are transparent. Also, remote control would only require two signal lines, Clock and Data In.

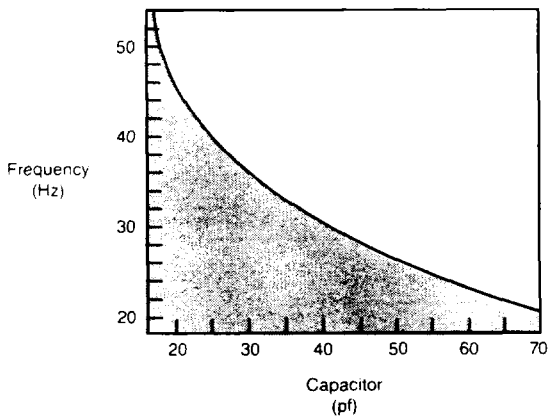


Figure 1

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