

Receiving Dual-Band Mixer

Description

The CXG1081TN is a receiving dual-band mixer MMIC. This IC is designed using the Sony's GaAs J-FET process.

Features

- High conversion gain $G_c = 9.5$ to 10.0 dB (Typ.)
- Low noise figure $NF = 4.6$ to 4.7 dB (Typ.)
- Single 2.7V power supply operation
- Low LO input power operation $PLO = -15$ dBm
- Single CTL pin achieved by the built-in inverter circuit
- 10-pin small package

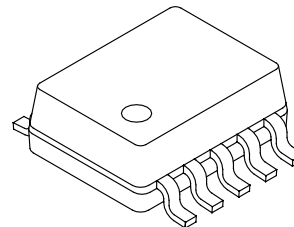
Applications

800MHz Japan digital cellular telephones (PDC)

Structure

GaAs J-FET MMIC

16 pin TSSOP (Plastic)



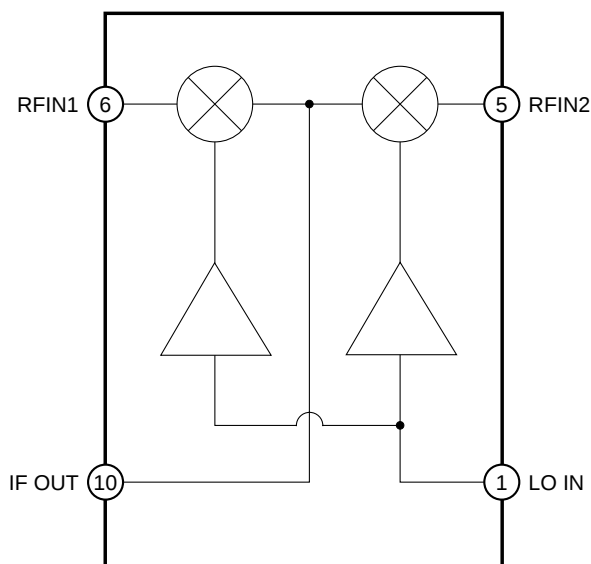
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	4.5	V
• Input power	P_{IN}	+5	dBm
• Current consumption	I_{DD} (Mixer block)	15	mA
• Operating temperature	T_{opr}	-35 to +85	°C
• Storage temperature	T_{stg}	-65 to +150	°C

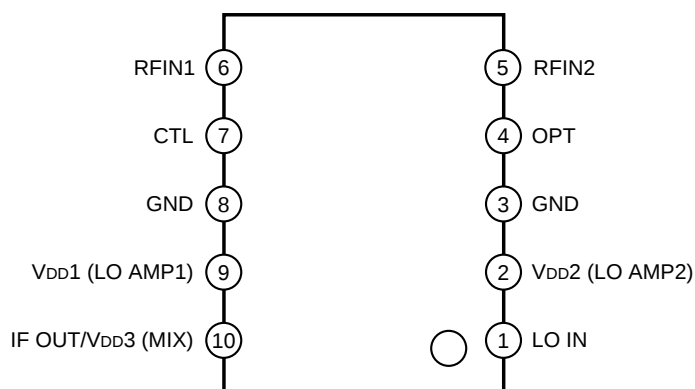
Recommended Operating Conditions

• Supply voltage	V_{DD}	2.7 to 3.3	V
• Control voltage	V_{CTL} (H)	2.4 to 3.3	V
	V_{CTL} (L)	0 to 0.3	V

Block Diagram



Pin Configuration



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Electrical Characteristics

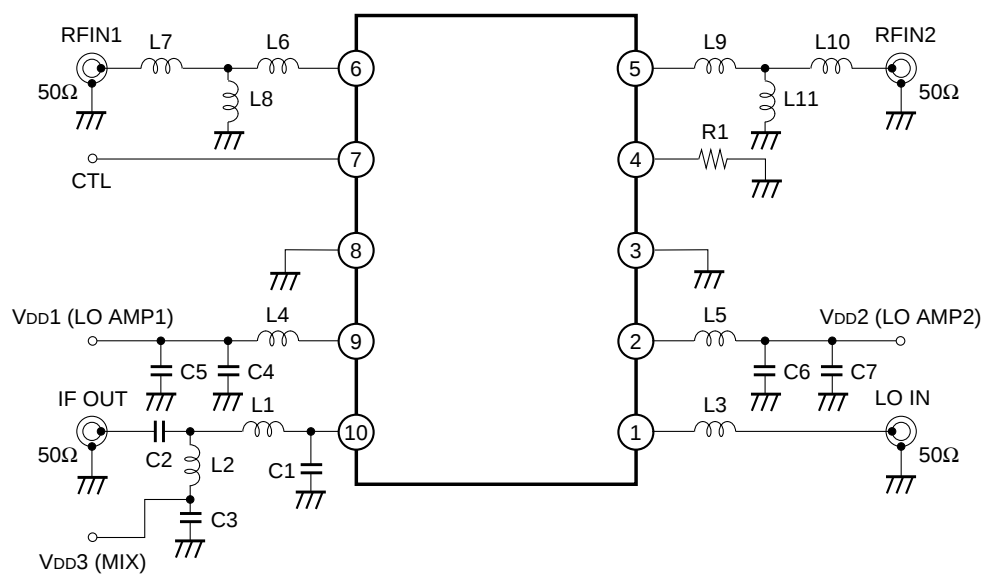
Conditions: $V_{DD} = 2.7V$, $V_{CTL} (H) = 2.7V$, $V_{CTL} (L) = 0V$, $f_{RF1} = 870MHz$, $f_{RF2} = 820MHz$,

$f_{LO} = f_{RF} - 130MHz$, $P_{LO} = -15dBm$, unless otherwise specified

($T_a = 25^{\circ}C$)

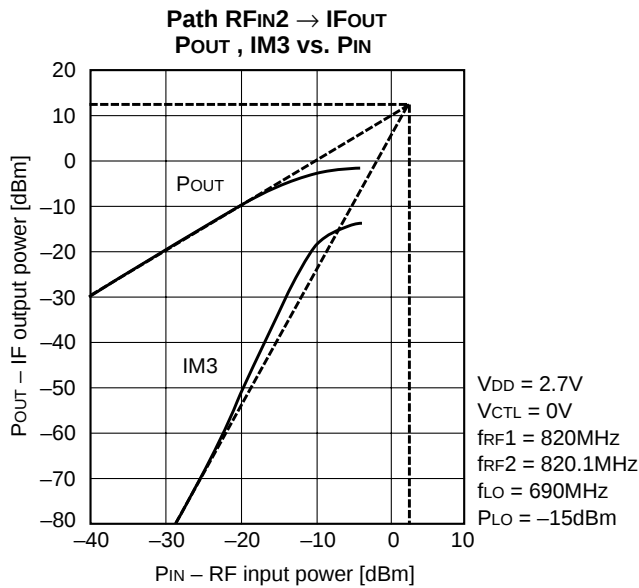
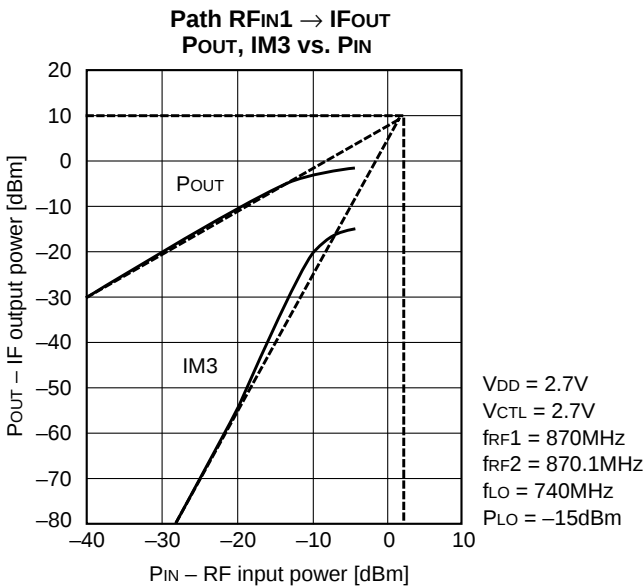
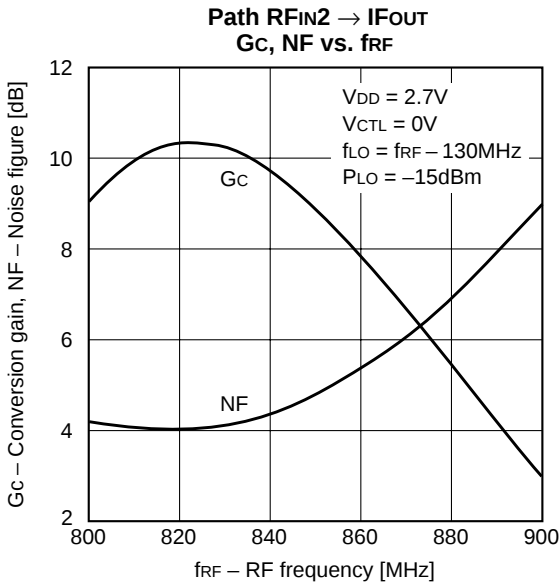
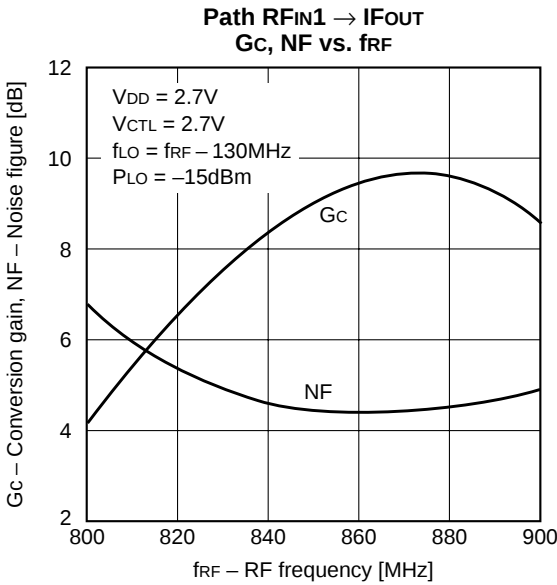
Item	Symbol	Path	V_{CTL}	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD}	V_{DD1}, V_{DD2} $V_{DD3} \rightarrow GND$	H	—	5.7	7.3	mA	When no signal
			L					
Control current	I_{CTL}	CTL $\rightarrow$ GND	H	—	35	70	μA	
		CTL $\rightarrow$ GND	L	-1	0	—		
Conversion gain	G_C	$RF_{IN1} \rightarrow IF_{OUT}$	H	8	9.5	11.5	dB	When a small signal
			L	—	-17	-12		
		$RF_{IN2} \rightarrow IF_{OUT}$	H	—	-19	-14		
			L	8	10	11.5		
Noise figure	NF	$RF_{IN1} \rightarrow IF_{OUT}$	H	—	4.6	6.5	dB	
		$RF_{IN2} \rightarrow IF_{OUT}$	L	—	4.7	6.5		
Input IP3	IIP3	$RF_{IN1} \rightarrow IF_{OUT}$	H	0	-2.5	—	dBm	P _{RF} = -25dBm, offset = 100kHz Conversion by the IM3 suppression ratio for two-wave input
		$RF_{IN2} \rightarrow IF_{OUT}$	L	0.5	3	—		
LO to RF leak level	P_{LK}	$LO_{IN} \rightarrow RF_{IN1}$	H	—	-29	-23	dBm	$f_{LO} = 740MHz$
		$LO_{IN} \rightarrow RF_{IN2}$	L	—	-29	-23		$f_{LO} = 690MHz$

Note) The values shown above are the specified values on the Sony's recommended evaluation board.

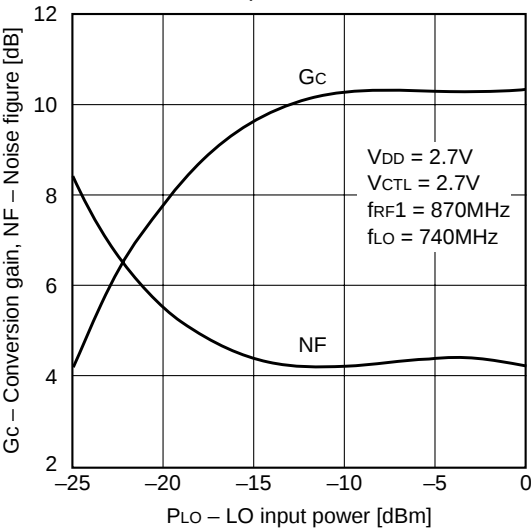


L1	120nH	L11	15nH
L2	82nH	C1	6pF
L3	27nH	C2	1000pF
L4	33nH	C3	1000pF
L5	39nH	C4	100pF
L6	27nH	C5	1000pF
L7	15nH	C6	100pF
L8	18nH	C7	1000pF
L9	33nH	R1	470Ω
L10	8.2nH		

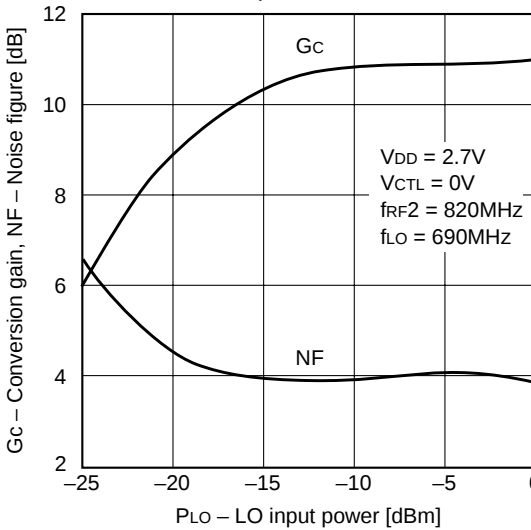
Example of Representative Characteristics (Ta = 25°C)



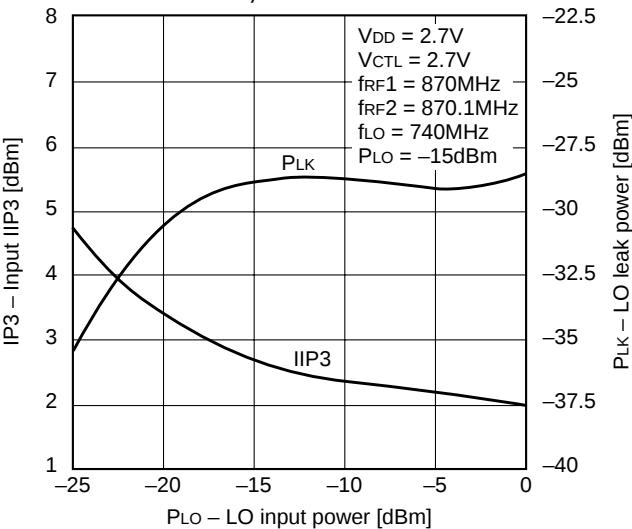
Path RFin1 → IFout
Gc, NF vs. PLO



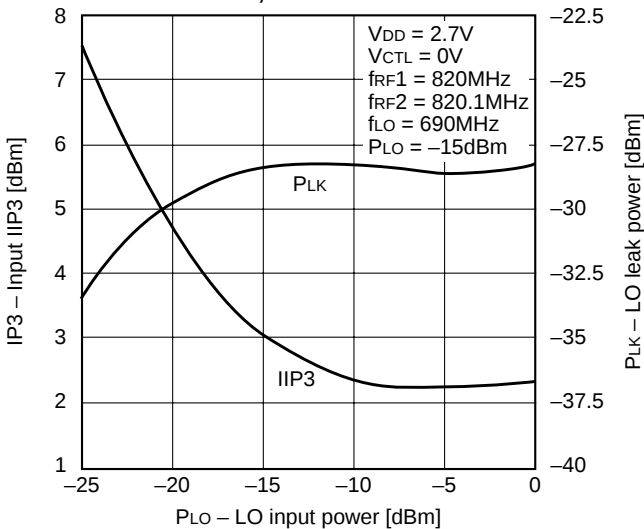
Path RFin2 → IFout
Gc, NF vs. PLO



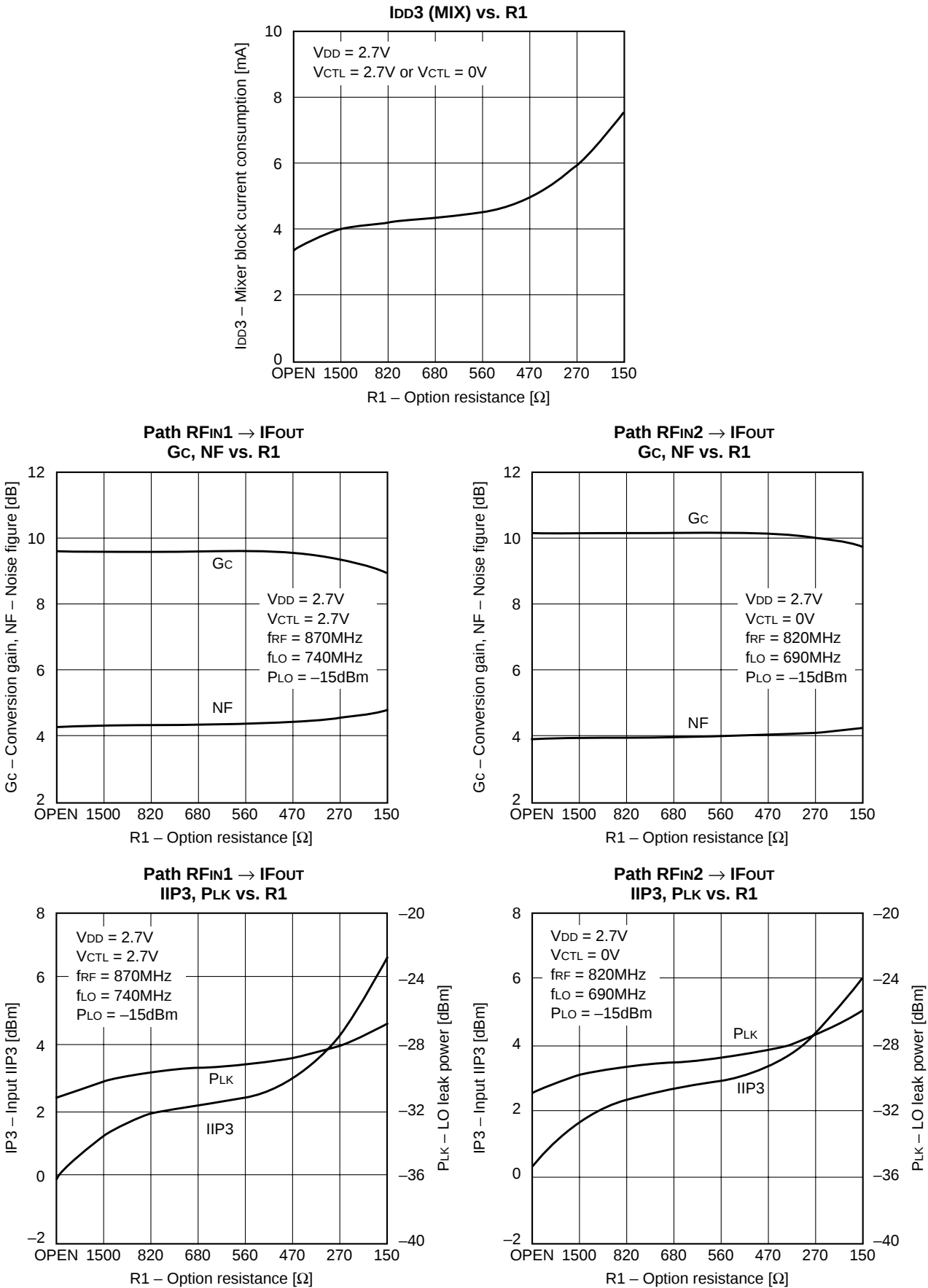
Path RFin1 → IFout
IIP3, PLK vs. PLO



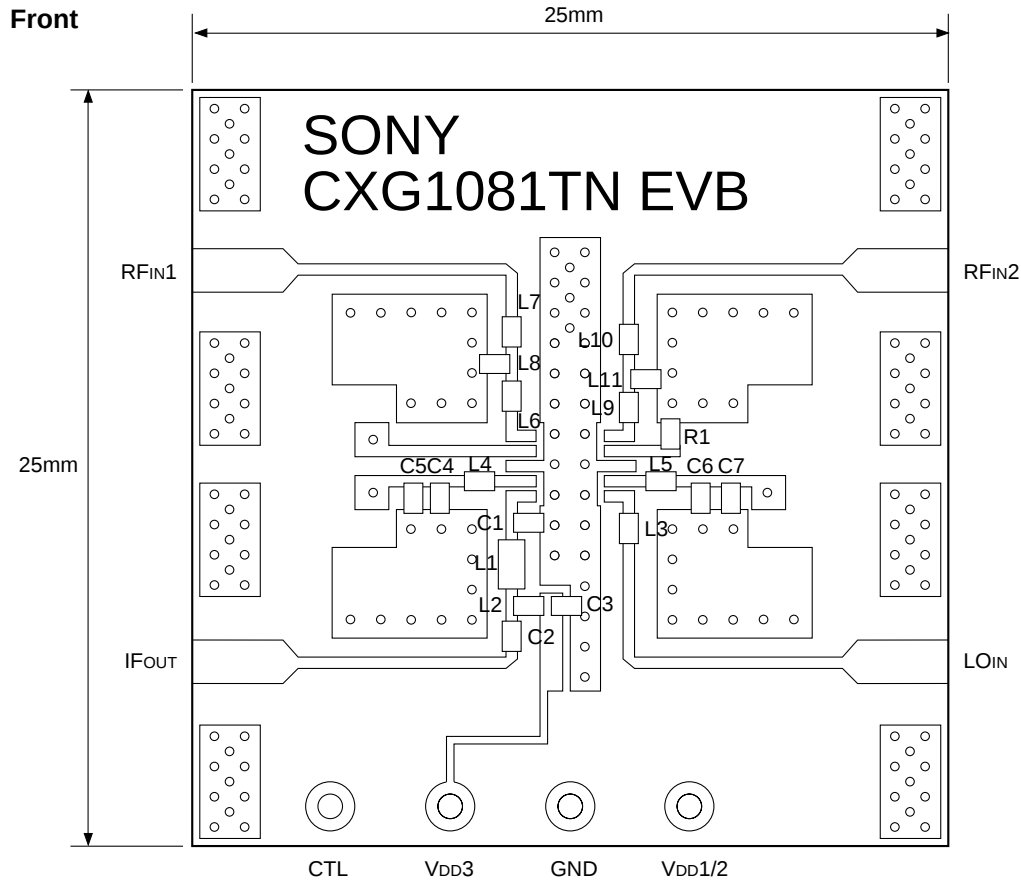
Path RFin2 → IFout
IIP3, PLK vs. PLO



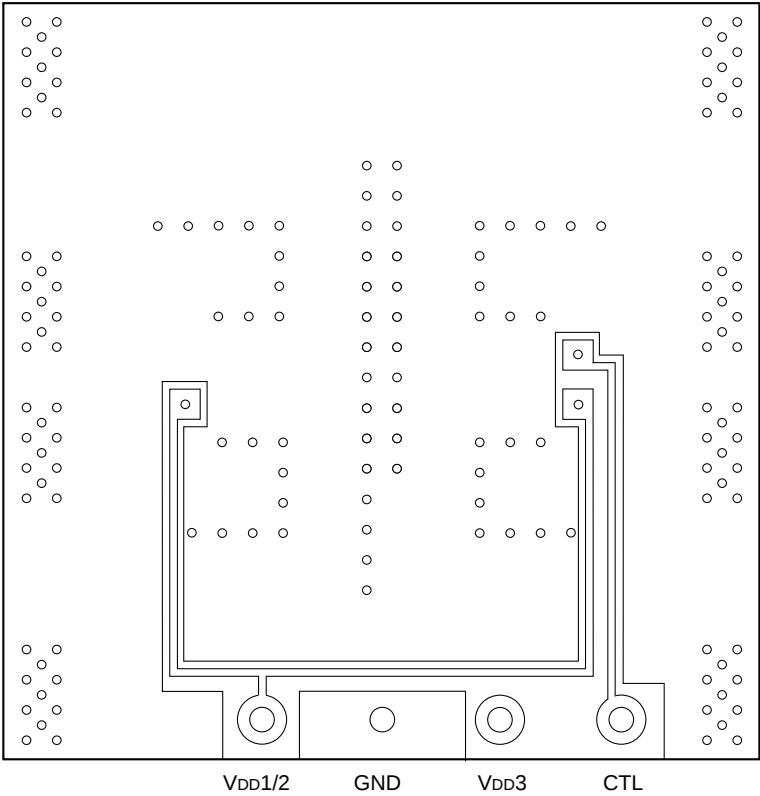
Example of Characteristics for Option Resistance R1 Changed (Ta = 25°C)



Recommended Evaluation Board



Back

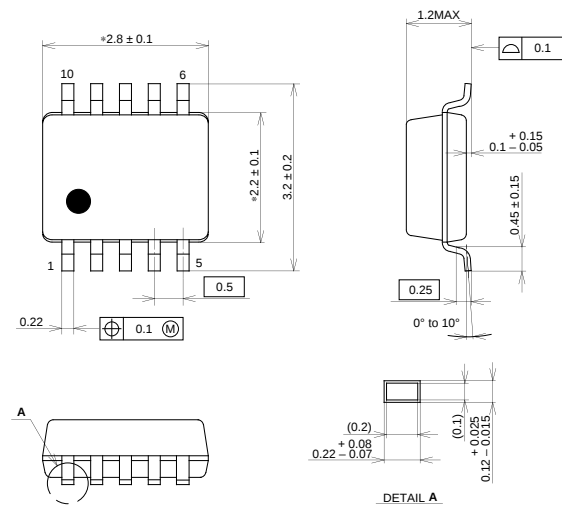


Glass fabric-base 4-layer epoxy board (thickness: 0.2mm × 2), total thickness: 0.8mm
GND for the whole 2nd and 3rd layers

Package Outline

Unit: mm

10PIN TSSOP(PLASTIC)



NOTE: "*" Dimensions do not include mold protrusion.

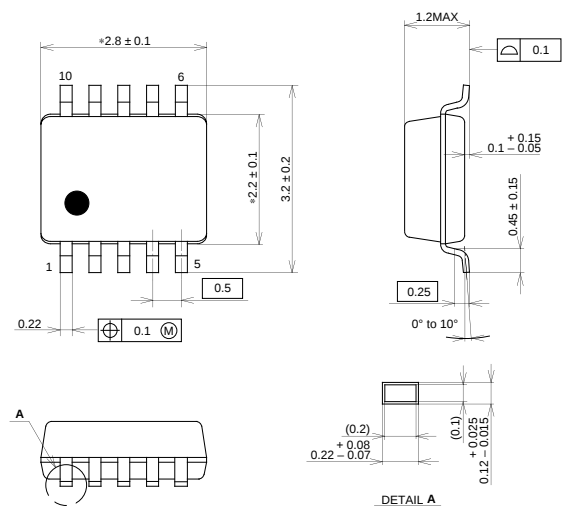
PACKAGE STRUCTURE

SONY CODE	TSSOP-10P-L01
EIAJ CODE	
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02g

Kokubu Ass'y

10PIN TSSOP(PLASTIC)



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PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02g

LEAD PLATING SPECIFICATIONS	
ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm