

High Input Voltage 8A PWM Converter With Adj. Soft Start

Features

- **Adjustable Output Voltage from +0.8V to +12V**
 - 0.8V Reference Voltage
 - $\pm 1\%$ Accuracy over Temperature
- **Operates from An Input Battery Voltage Range of +2.7V to +28V**
- **Power-On-Reset Monitoring on VCC pin**
- **Excellent line and load transient responses**
- **PFM mode for increased light load efficiency**
- **Programmable PWM Frequency from 100kHz to 1000kHz**
- **Integrated 30mW at VCC=5V N-Channel MOSFET For High Side**
- **Integrated 9mW at VCC=5V N-Channel MOSFET For Low Side**
- **Integrated Bootstrap Forward P-CH MOSFET**
- **External Adjustable Soft-Start and Soft-Stop**
- **Selectable Forced PWM or automatic PFM/PWM mode**
- **Power Good Monitoring**
- **70% Under-Voltage Protection**
- **125% Over-Voltage Protection**
- **Current-Limit Protection**
 - Using Sense Low-Side MOSFET's RDS(ON)
- **Over-Temperature Protection**
- **TQFN-23 4mmx4mm package**
- **Lead Free and Green Device Available (RoHS Compliant)**

General Description

The APW8713 is a 8A, synchronous, step-down converter with integrated 30m Ω N-channel High-Side MOSFET and 9m Ω Low-Side MOSFET. The APW8713 steps down high voltage to generate low-voltage chipset or RAM supplies in notebook computers.

The APW8713 provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Mode (PFM), the APW8713 provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. In PWM Mode, the converter works nearly at constant frequency for low-noise requirements.

The APW8713 is equipped with accurate current-limit, output under-voltage, and output over-voltage protections, perfect for various applications. A Power-On-Reset function monitors the voltage on VCC to prevent wrong operation during power-on. The APW8713 has external adjustable soft-start and built-in an integrated output discharge method for soft stop. A soft-start ramps up the output voltage with programmable timing to reduce the start-up current. A soft-stop function actively discharges the output capacitors.

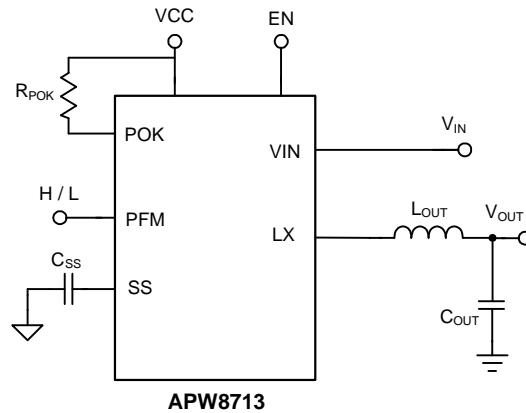
The APW8713 is available in TQFN4x4-23 (Power PAK).

Applications

- **Notebook**
- **Mother Board**
- **Table PC**
- **Hand-Held Portable**
- **AIO PC**
- **Set-top boxes**
- **LCD TV**

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Simplified Application Circuit

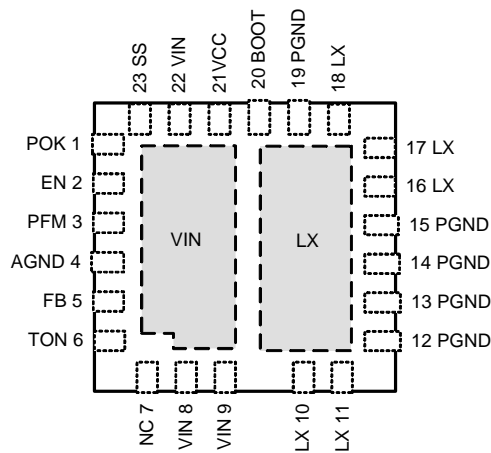


Ordering and Marking Information

| | |
|---|---|
| <p>APW8713 □□□-□□□</p> <p>Assembly Material Handling Code Temperature Range Package Code</p> | <p>Package Code QB: TQFN4x4-23 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Lead Free Code L : Lead Free Device G : Halogen and Lead Free Device</p> |
| <p>APW8713 QB : XXXXX</p> | <p>XXXXX - Date Code</p> |

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TQFN 4x4 -23 (TOP VIEW)
 = Exposed and Thermal Pad

Absolute Maximum Ratings (Note 1)

| Symbol | Parameter | Rating | Unit |
|----------------|--|----------------------|------|
| V_{VCC} | VCC Supply Voltage (VCC to AGND) | -0.3 ~ 7 | V |
| V_{IN} | VIN Supply Voltage (VIN to AGND) | -0.3 ~ 30 | V |
| V_{TON} | TON Supply Voltage (TON to AGND) | -0.3 ~ 30 | V |
| $V_{BOOT-GND}$ | BOOT Supply Voltage (BOOT to AGND) | -0.3 ~ 37 | V |
| V_{BOOT} | BOOT Supply Voltage (BOOT to PHASE) | -0.3 ~ 7 | V |
| V_{GND} | AGND to PGND | -0.3 ~ +0.3 | V |
| | All Other Pins (POK, EN, FB, SS and PFM to AGND) | -0.3 ~ 7 | V |
| V_{LX} | LX Voltage (LX to GND) <20ns pulse width >20ns pulse width | -5 ~ 32 -0.3 ~ 30 | V |
| T_J | Junction Temperature | 150 | °C |
| T_{STG} | Storage Temperature | -65 ~ 150 | °C |
| T_{SDR} | Maximum Lead Soldering Temperature(10 Seconds) | 260 | °C |

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

| Symbol | Parameter | Typical Value | Unit |
|---------------|---|---------------|------|
| θ_{JA} | Junction-to-Ambient Resistance in free air (Note 2) | 50 | °C/W |

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

| Symbol | Parameter | Range | Unit |
|-----------|---|------------|------|
| V_{VCC} | VCC Supply Voltage | 4.5 ~ 5.5 | V |
| V_{IN} | Converter Input Voltage | 2.7 ~ 28 | V |
| V_{OUT} | Converter Output Voltage | 0.8 ~ 13.2 | V |
| I_{OUT} | Converter Output Current | 0 ~ 8 | A |
| C_{IN} | PWM1/2 Converter Input Capacitor (MLCC) | 10 ~ | μF |
| C_{VCC} | VCC Output Capacitor (MLCC) | 1.0 ~ | μF |
| T_A | Ambient Temperature | -40 ~ 85 | °C |
| T_J | Junction Temperature | -40 ~ 125 | °C |

Note 3: Refer to the application circuit for further information.

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN}=12V, V_{EN}=5V$ and $T_A = -40$ to $85^\circ C$. Typical values are at $T_A=25^\circ C$.

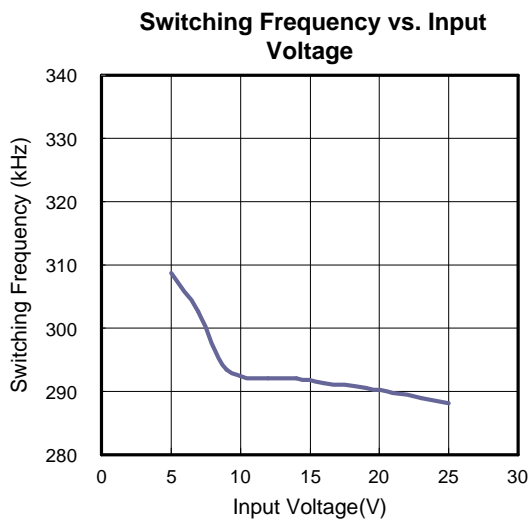
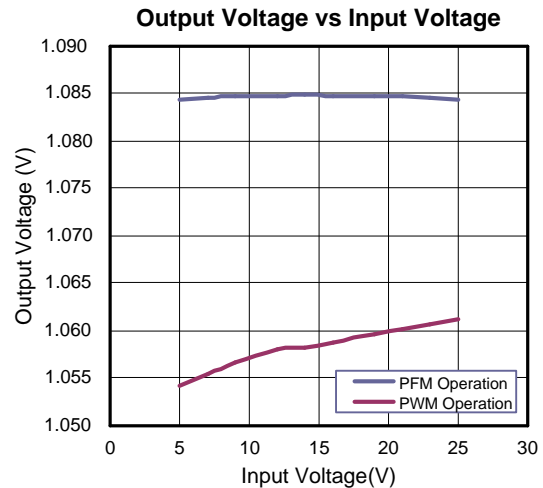
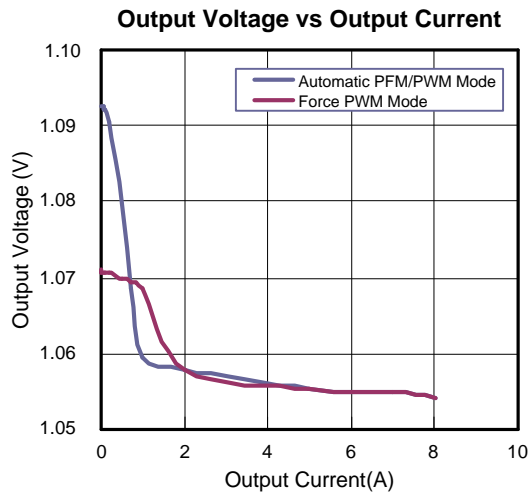
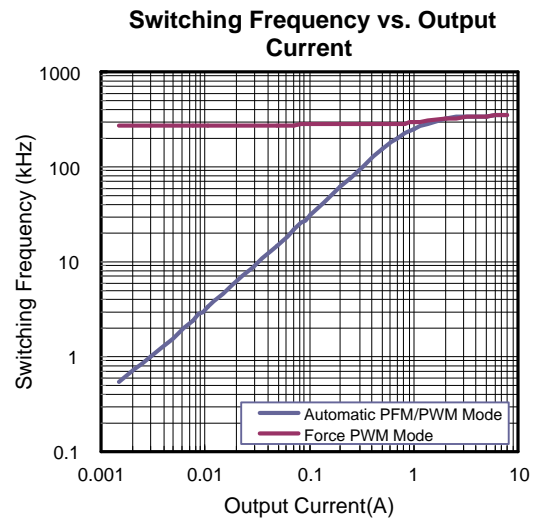
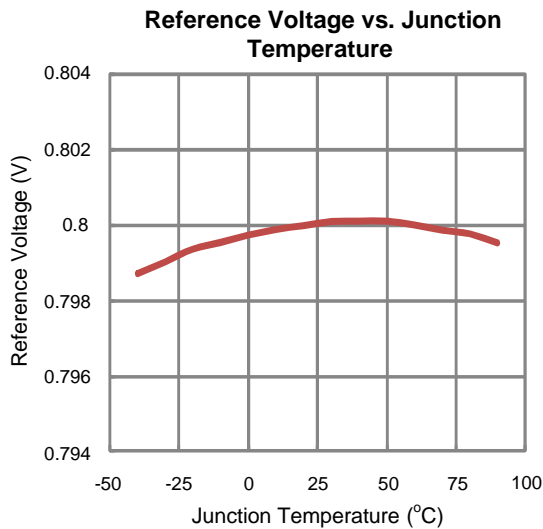
| Symbol | Parameter | Test Condition | APW8713 | | | |
|--|-----------------------------------|--|---------|---------------------|------|------------|
| | | | Min. | Typ. | Max. | Unit |
| VOUT AND VFB VOLTAGE | | | | | | |
| V_{OUT} | Output Voltage | Adjustable output range | 0.8 | | 13.2 | V |
| V_{REF} | Reference Voltage | | | 0.8 | | V |
| | Regulation Accuracy | $T_A = -40^\circ C \sim 85^\circ C$ | -1.0 | - | +1.0 | % |
| I_{FB} | FB Input Bias Current | FB=0.75V | | 0.02 | - | μA |
| T_{STOP} | Output Discharge Time | EN go low to output remain below 0.1V | - | 5*Tss | - | - |
| SUPPLY CURRENT | | | | | | |
| $I_{VCC_NOR_MAL}$ | VCC Quiescent Supply Current | EN=5V, FB=0.835V, VCC=5V | - | 0.7 | 1 | mA |
| I_{VCC_SHDN} | VCC Shutdown Current | EN=GND, VCC=5V | - | - | 25 | μA |
| ON-TIME TIMER AND INTERNAL SOFT START | | | | | | |
| T_{ON} | Nominal on time | $V_{IN}=12V, V_{OUT}=1V, R_{TON}=100k\Omega$ | 200 | 250 | 300 | ns |
| F_{SW} | Frequency adjustable range | | 100 | | 1000 | kHz |
| $T_{OFF(MIN)}$ | Minimum off time | $V_{FB}=0.75V, V_{PHASE}=-0.1V$ | - | 250 | - | ns |
| I_{SS} | Internal Soft Start Current | $V_{SS}=0V, C_{SS}=0.001\mu F$ to $0.1\mu F$ | 8 | 10 | 12 | μA |
| T_{SS} | Internal Soft Start Time | EN High to POK High | - | 330*C _{SS} | - | ms |
| GATE DRIVER | | | | | | |
| | High Side MOSFET On Resistance | $V_{IN}=12V, V_{CC}=5V$ | - | 30 | 45 | m Ω |
| | Low Side MOSFET On Resistance | $V_{IN}=12V, V_{CC}=5V$ | - | 9 | 13.5 | m Ω |
| BOOTSTRAP SWITCH | | | | | | |
| V_F | Ron | $V_{PVCC} - V_{BOOT-GND}, I_F = 10mA$ | - | 0.5 | 0.7 | V |
| I_R | Reverse Leakage | $V_{BOOT-GND} = 30V, V_{PHASE} = 25V, V_{PVCC} = 5V$ | - | - | 0.5 | μA |
| VCC POR THRESHOLD | | | | | | |
| V_{LCC_THF} | Falling VCC POR Threshold Voltage | | 4.25 | 4.35 | 4.45 | V |
| | LDO POR Hysteresis | | - | 100 | - | mV |
| CONTROL INPUTS | | | | | | |
| | EN High-Level Input Voltage | | 2.5 | - | - | V |
| | EN Low-Level Input Voltage | | - | - | 0.5 | V |
| | EN Leakage | EN=0V | - | 0.1 | - | μA |
| | PFM High-Level Input Voltage | | 2.5 | - | - | V |
| | PFM Low-Level Input Voltage | | - | - | 0.5 | V |
| | PFM Leakage | PFM=0V | - | 0.1 | - | μA |

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN}=12V, V_{EN}=5V$ and $T_A = -40$ to $85^\circ C$. Typical values are at $T_A=25^\circ C$.

| Symbol | Parameter | Test Condition | APW8713 | | | |
|---------------------------|---------------------------------|------------------------------------|---------|------|------|------------|
| | | | Min. | Typ. | Max. | Unit |
| POWER-OK INDICATOR | | | | | | |
| V_{POK} | POK Threshold | POK in from Lower (POK Goes High) | 87 | 90 | 93 | % |
| | | POK out from Normal (POK Goes Low) | 120 | 125 | 130 | % |
| I_{POK} | POK Leakage Current | $V_{POK}=5V$ | - | 0.1 | - | μA |
| | POK Sink Current | $V_{POK}=0.5V$, | 1.25 | 7.5 | - | mA |
| | POK Out Debounce Time2 | When run away 90% | - | 20 | - | μs |
| | POK Enable Delay Time | From EN High to POK High | - | Tss | - | ms |
| CURRENT SENSE | | | | | | |
| I_{OCP} | OCP Threshold | Valley Current of IL | 11 | - | - | A |
| | Zero Crossing Comparator Offset | V_{GND-LX} Voltage, PFM=0V | -5 | 0 | 5 | mV |
| PROTECTION | | | | | | |
| V_{UV} | UVP Threshold | | 65 | 70 | 75 | % |
| | UVP Debounce Interval | | | 16 | | μs |
| | UVP Enable Delay | EN high to UVP workable | | Tss | | ms |
| V_{OVR} | OVP Rising Threshold1 | OVP Occur | 120 | 125 | 130 | % |
| | OVP Propagation Delay | V_{FB} Rising, Over Voltage=10mV | - | 3 | - | μs |
| T_{OTR} | OTP Rising Threshold (Note 5) | | - | 145 | - | $^\circ C$ |
| | OTP Hysteresis (Note 5) | | - | 45 | - | $^\circ C$ |

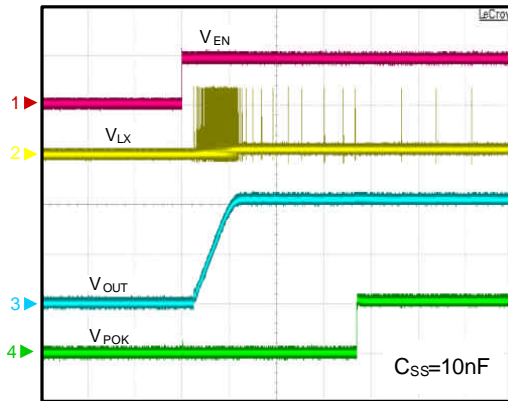
Typical Operating Characteristics



Operating Waveforms

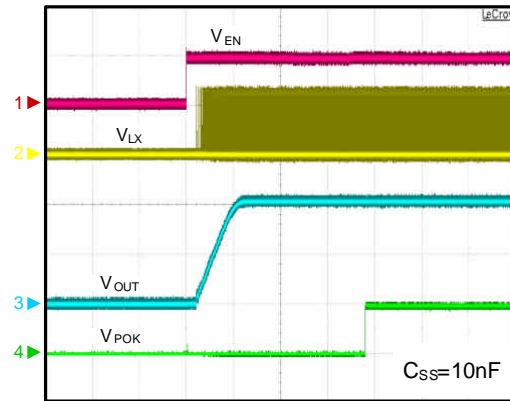
Refer to the typical application circuit. $T_A = 25^\circ\text{C}$ unless otherwise specified.

Enable Without Loading



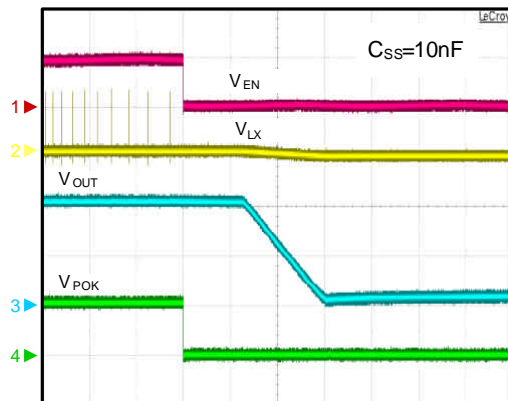
CH1: V_{EN} , 5V/Div, DC
 CH2: V_{LX} , 10V/Div, DC
 CH3: V_{OUT} , 500mV/Div, DC
 CH4: V_{POK} , 5V/Div, DC
 TIME: 1ms/Div

Enable With Loading



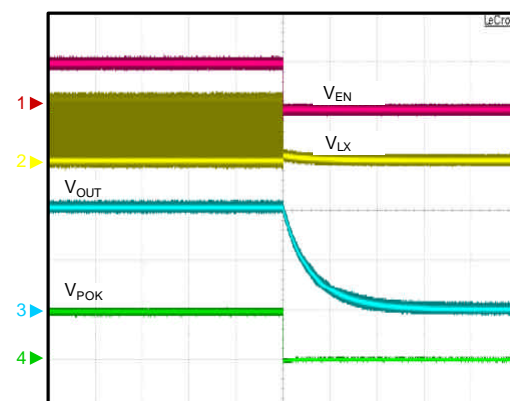
CH1: V_{EN} , 5V/Div, DC
 CH2: V_{LX} , 10V/Div, DC
 CH3: V_{OUT} , 500mV/Div, DC
 CH4: V_{POK} , 5V/Div, DC
 TIME: 1ms/Div

Soft- Stop Function



CH1: V_{EN} , 5V/Div, DC
 CH2: V_{LX} , 10V/Div, DC
 CH3: V_{OUT} , 500mV/Div, DC
 CH4: V_{POK} , 5V/Div, DC
 TIME: 5ms/Div

Shutdown With Loading

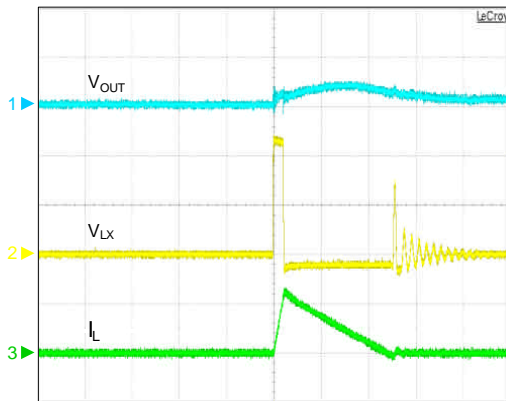


CH1: V_{EN} , 5V/Div, DC
 CH2: V_{LX} , 10V/Div, DC
 CH3: V_{OUT} , 500mV/Div, DC
 CH4: V_{POK} , 5V/Div, DC
 TIME: 500 μ s/Div

Operating Waveforms

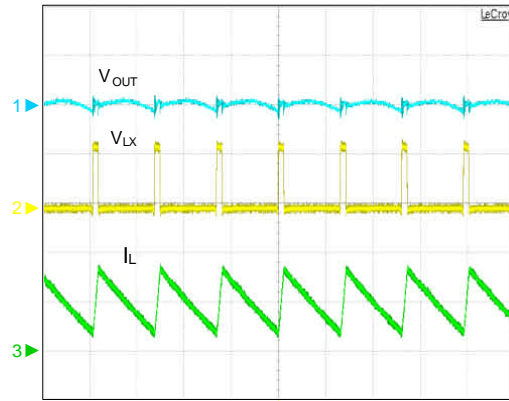
Refer to the typical application circuit. $T_A = 25^\circ\text{C}$ unless otherwise specified.

PFM Switching Waveform



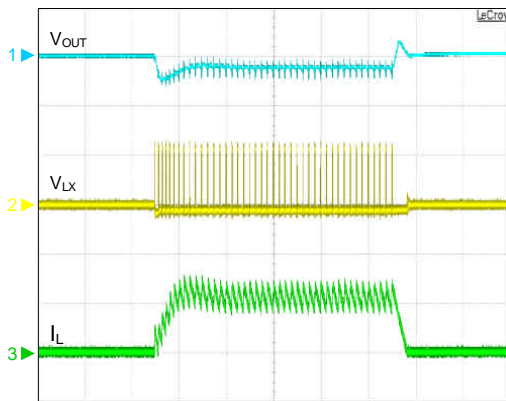
CH1: V_{OUT} , 50mV/Div, AC
 CH2: V_{LX} , 5V/Div, DC
 CH3: I_L , 2A/Div, DC
 TIME: 1 μ s/Div

PWM Switching Waveform



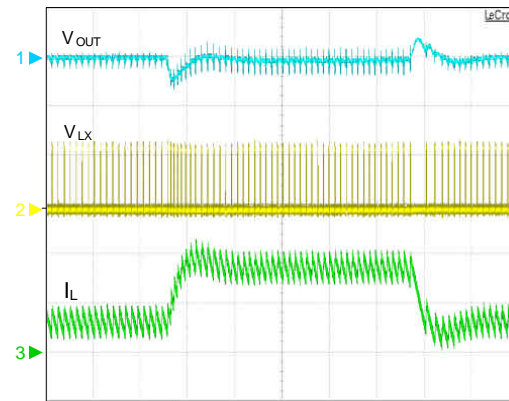
CH1: V_{OUT} , 50mV/Div, AC
 CH2: V_{LX} , 10V/Div, DC
 CH3: I_L , 2A/Div, DC
 TIME: 2 μ s/Div

Load Transient 1



CH1: V_{OUT} , 100mV/Div, AC
 CH2: V_{LX} , 10V/Div, DC
 CH3: I_L , 5A/Div, DC
 TIME: 20 μ s/Div

Load Transient 2

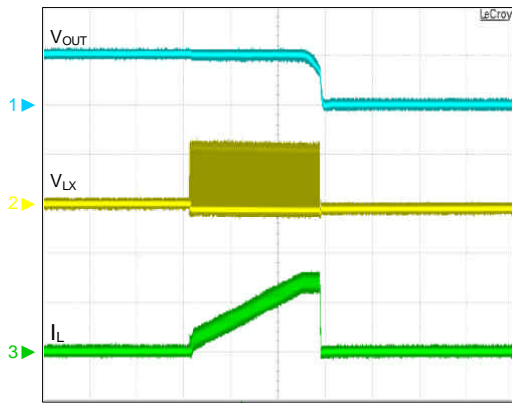


CH1: V_{OUT} , 100mV/Div, AC
 CH2: V_{LX} , 10V/Div, DC
 CH3: I_L , 5A/Div, DC
 TIME: 20 μ s/Div

Operating Waveforms

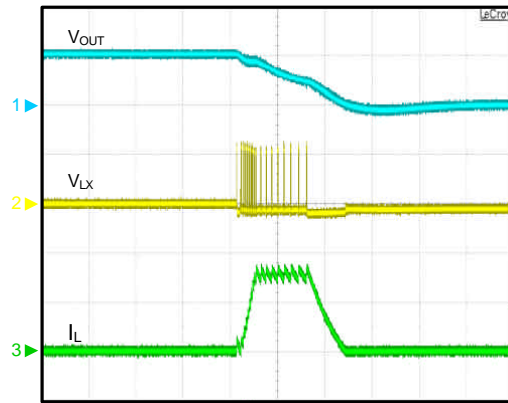
Refer to the typical application circuit. $T_A = 25^\circ\text{C}$ unless otherwise specified.

Current Limit and UVP Function



CH1: V_{OUT} , 1V/Div, DC
 CH2: V_{LX} , 10V/Div, DC
 CH3: I_L , 10A/Div, DC
 TIME: 500 μ s/Div

Short Circuit Protection

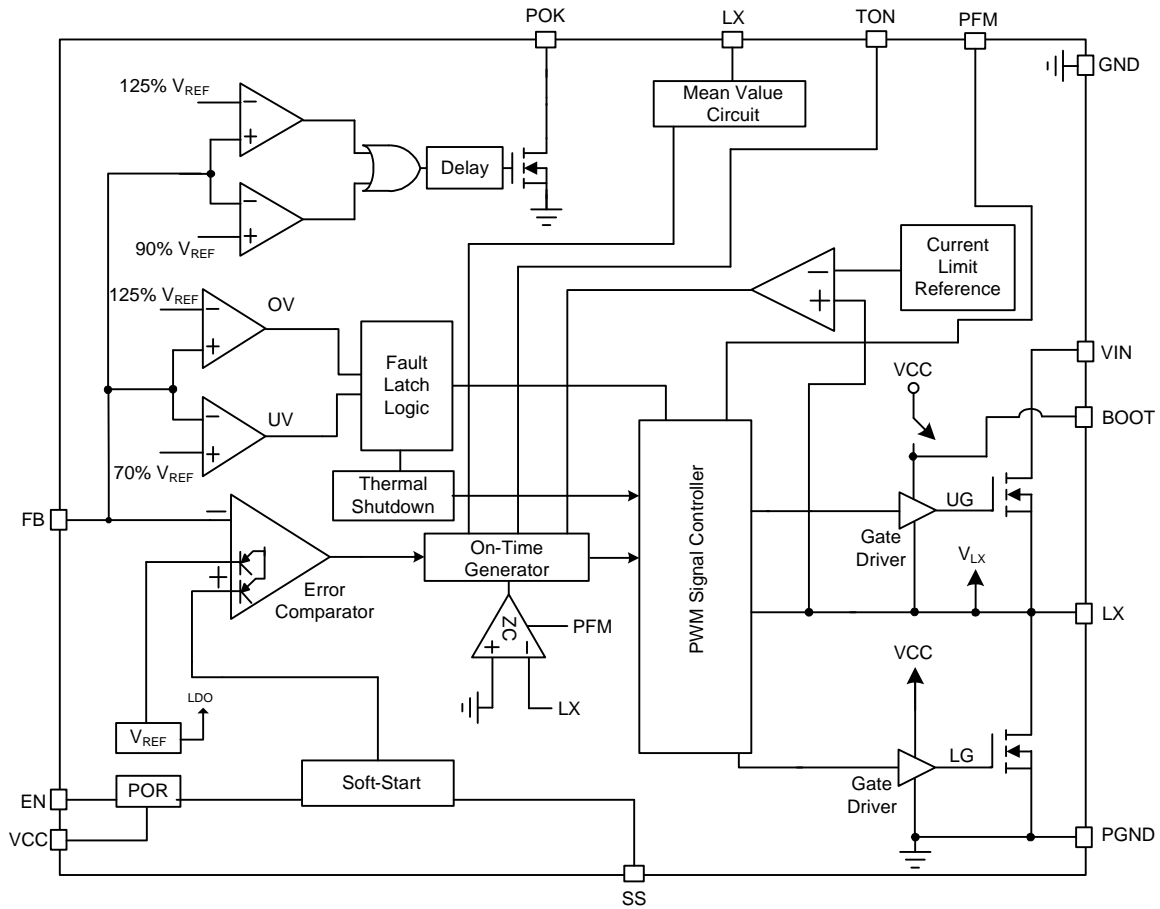


CH1: V_{OUT} , 1V/Div, DC
 CH2: V_{LX} , 10V/Div, DC
 CH3: I_L , 10A/Div, DC
 TIME: 20 μ s/Div

Pin Description

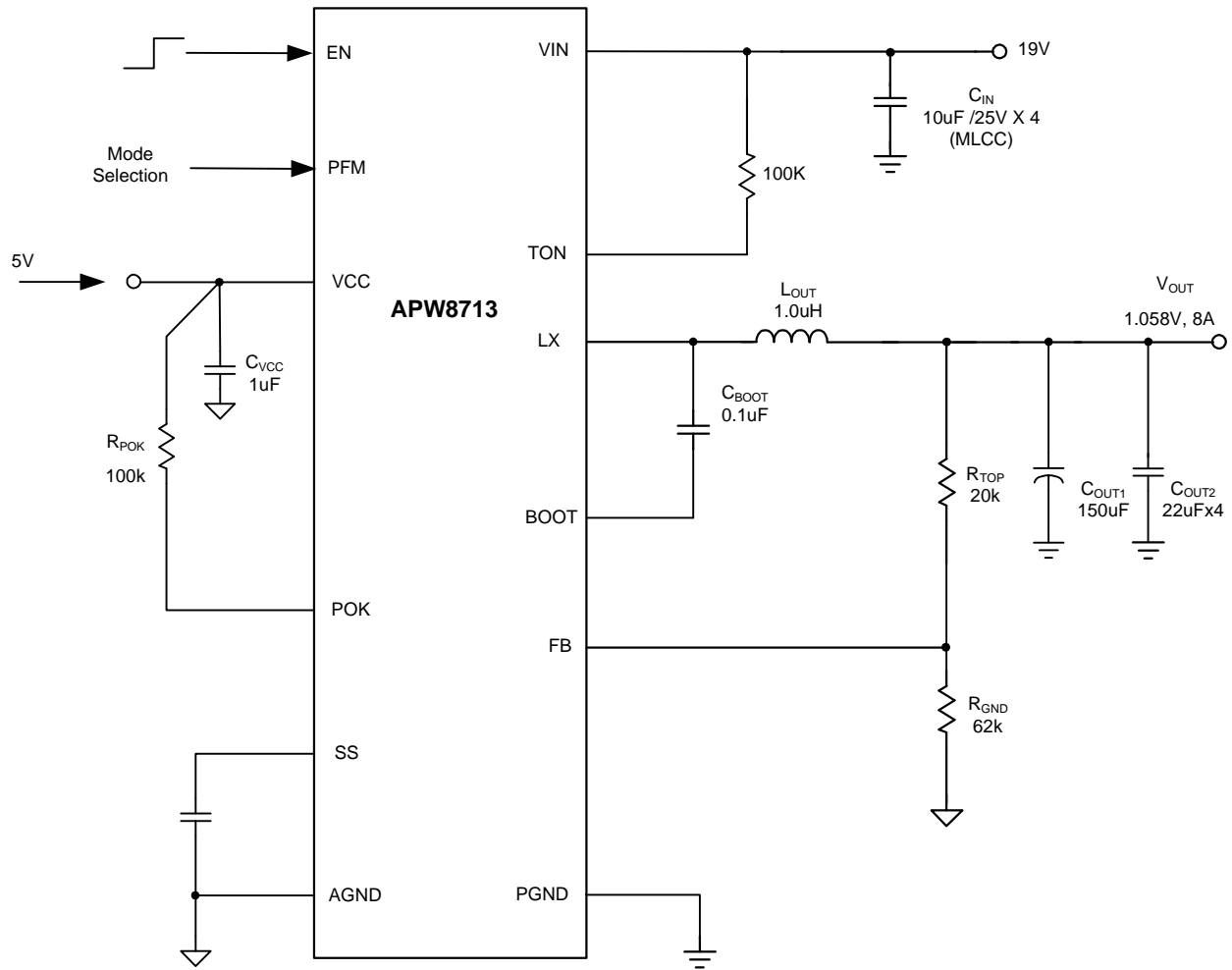
| PIN | | FUNCTION |
|---------------|------|---|
| NO. | NAME | |
| 1 | POK | Power-Good Output Pin of PWM. POK is an open-drain output used to indicate the status of the PWM output voltage. Connect the POK in to +5V through a pull-high resistor. |
| 2 | EN | PWM Enable. PWM is enabled when EN=1. When EN=0, PWM is in shutdown. |
| 3 | PFM | PFM Selection Input. When the PFM is above high logic level, the Device is in force PWM mode. When the PFM is below low logic level, the device is in automatic PFM/PWM Mode. |
| 4 | AGND | Signal Ground for The IC. |
| 5 | FB | Output Voltage Feedback Pin. This pin is connected to the resistive divider that set the desired output voltage. The POK, UVP, and OVP circuits detect this signal to report output voltage status. |
| 6 | TON | This Pin is Allowed to Adjust The Switching Frequency. Connect a resistor R_{TON} from TON pin to VIN pin. |
| 7 | NC | No connect. |
| 8, 9, 22 | VIN | Battery Voltage Input Pin. VIN powers linear regulators and is also used for the constant on-time PWM on-time one-shot circuits. Connect VIN to the battery input and bypass with a $1\mu\text{F}$ capacitor for noise interference. |
| 10, 11, 16~18 | LX | Junction Point of The High-Side MOSFET Source, Output Filter Inductor and The Low-Side MOSFET Drain for PWM. Connect this pin to the Source of the high-side MOSFET. LX serves as the lower supply rail for the UGATE high-side gate driver. LX is the current-sense input for the PWM. |
| 12~15, 19 | PGND | Power Ground of The LGATE Low-Side MOSFET Drivers. |
| 20 | BOOT | Supply Input for The UGATE Gate Driver and an internal level-shift circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET. |
| 21 | VCC | Supply Voltage Input Pin for Control Circuitry, Connect +5V from the VCC pin to the GND pin. Decoupling at least $1\mu\text{F}$ of a MLCC capacitor from the VCC pin to the AGND pin. |
| 23 | SS | Soft Start Output. Connect a capacitor to GND to set the soft start interval. |

Block Diagram



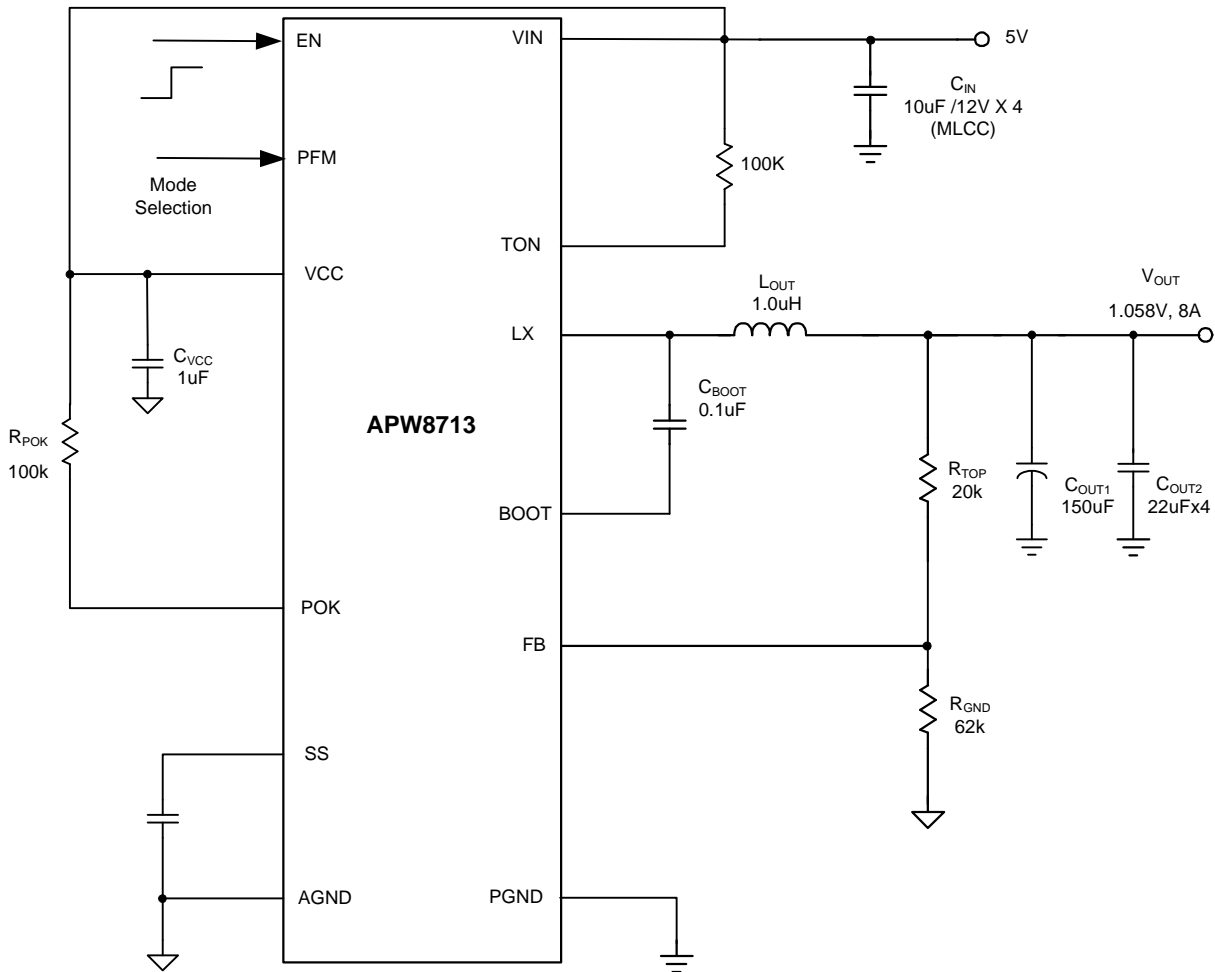
Typical Application Circuit

When $V_{in}=19V$, Dual Power Input :



Typical Application Circuit

When $V_{in}=5V$, Single Power Input :



Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block.

The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant on-time controller, which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on VIN pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typical: 250ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Over-Current Protection of the PWM Converter

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$T_{\text{ON-PFM}} = \frac{1}{F_{\text{SW}}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Where FSW is the nominal switching frequency of the converter in PWM mode.

The load current at handoff from PFM to PWM mode is given by:

$$\begin{aligned} I_{\text{LOAD (PFM to PWM)}} &= \frac{1}{2} \times \frac{V_{\text{IN}} - V_{\text{OUT}}}{L} \times T_{\text{ON-PFM}} \\ &= \frac{V_{\text{IN}} - V_{\text{OUT}}}{2L} \times \frac{1}{F_{\text{SW}}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} \end{aligned}$$

Forced-PWM Mode

The Forced-PWM mode disables the zero-crossing comparator, which truncates the low-side switch on-time at the inductor current zero crossing. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads while UG maintains a duty factor of $V_{\text{OUT}}/V_{\text{IN}}$. The benefit of Forced-PWM mode is to keep the switching frequency fairly constant. The Forced-PWM mode is most useful for reducing audio frequency noise, improving load-transient response, and providing sink-current capability for dynamic output voltage adjustment.

When V_{PFM} is above the PFM high threshold (2.5V, minimum), the converter is in forced-PWM mode. When V_{PFM} is below the PFM low threshold (0.5V, maximum), the chip is in automatic PFM/PWM Mode.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising POR voltage threshold (4.35V, typical), the POR signal goes high and the chip initiates soft-start operations. Should this voltage drop lower than 4.25V (typical), the POR disables the chip.

En Pin Control

When V_{EN} is above the EN high threshold (2.5V, minimum), the converter is enabled. When V_{EN} is below the EN low threshold (0.5V, maximum), the chip is in the shutdown and only low leakage current is taken from VCC.

Function Description (Cont.)

Soft-Start

The APW8713 provides the programmed soft-start function to limit the inrush current. The soft-start time can be programmed by the external capacitor between SS and GND. Typical charge current is 10uA, and the soft-start time can be calculated by the following formula:

$$T_{SS}(\mu s) = 330 \times C_{SS}(nF)$$

The APW8713 integrates soft-start circuits to ramp up the output voltage of the converter to the programmed regulation set point at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during soft-start process. When the EN pin is pulled above the rising EN threshold voltage, the device initiates a soft-start process to ramp up the output voltage.

During soft-start stage before the PGOOD pin is ready, the under voltage protection is prohibited. The over voltage and current limit protection functions are enabled. If the output capacitor has residue voltage before startup, both low-side and high-side MOSFETs are in off-state until the soft start voltage equal the V_{FB} voltage. This will ensure the output voltage starts from its existing voltage level.

In the event of under-voltage, over-voltage, over-temperature or shutdown, the chip enables the soft-stop function. The soft-stop function discharges the output voltages by low side turns MOSFET on linearly.

Power Good Indicator

POK is actively held low in shutdown and soft-start status. In the soft-start process, the POK is an open-drain. When the soft-start is finished, the POK is released. In normal operation, the POK window is from 90% to 125% of the converter reference voltage. When the output voltage has to stay within this window, POK signal will become high. When the output voltage outruns 90% or 125% of the target voltage, POK signal will be pulled low immediately. In order to prevent false POK drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

Under-Voltage Protection (UVP)

In the process of operation, if a short circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage protection circuit continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under voltage threshold, the under voltage threshold is 70% of the nominal output voltage, the internal UVP delay counter starts to count. After 16ms de-bounce time, the device turns off both high side and low-side MOSFET with latched. Toggling enable pin to low, or recycling VIN, will clear the latch and bring the chip back to operation.

Over-Voltage Protection (OVP)

The over voltage function monitors the output voltage by FB pin. Should the FB voltage increase over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over voltage protection comparator designed with a 3μs noise filter will force the low-side MOSFET gate driver fully turn on and latch high. This action actively pulls down the output voltage.

This OVP scheme only clamps the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It's a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, it can only be reset by toggling EN or VIN power-on-reset signal.

Current Limit

The current limit circuit employs a "valley" current-sensing algorithm (See Figure 1). The APW8713 uses the low-side MOSFET's $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at LX pin is above the current-limit threshold 11A(minimum), the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and input voltage.

Function Description (Cont.)

Current Limit(Cont.)

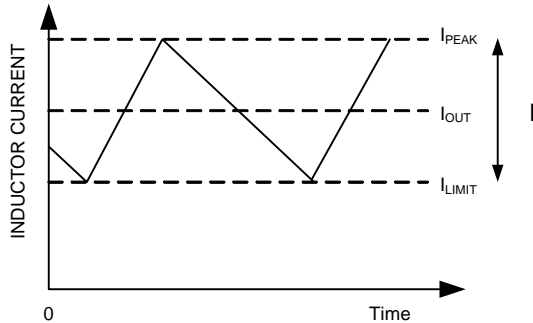


Figure 1. Current Limit algorithm

The PWM controller uses the low-side MOSFETs on-resistance $R_{DS(ON)}$ to monitor the current for protection against shorted outputs. The MOSFET's $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacture's datasheet.

The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at LX. Place the hottest power MOSFETs as close to the IC as possible for best thermal coupling. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance.

Over-Temperature Protection (OTP)

When the junction temperature increases above the rising threshold temperature T_{OTR} , the IC will enter the over temperature protection state that suspends the PWM, which forces the UG and LG gate drivers output low. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 45°C. The OTP designed with a 45°C hysteresis lowers the average T_j during continuous thermal overload conditions, which increases lifetime of the APW8713.

Programming the On-Time Control and PWM Switching Frequency

The APW8713 does not use a clock signal to produce PWM. The device uses the constant on-time control architecture to produce pseudo-fixed frequency with input voltage feed-forward. The on-time pulse width is proportional to output voltage V_{OUT} and inverse proportional to input voltage V_{IN} . In PWM, the on-time calculation is written as below equation.

$$T_{ON} = \frac{26.3 \times 10^{-12} \times R_{TON}(\Omega)}{V_{IN}(V)}$$

Where:

R_{TON} is the resistor connected from TON pin to VIN pin. Furthermore, The approximate PWM switching frequency is written as:

$$T_{ON} = \frac{D}{F_{SW}}, F_{SW} = \frac{V_{OUT}/V_{IN}}{T_{ON}}$$

Where:

F_{SW} is the PWM switching frequency.

Application Information

Output Inductor Selection

The output voltage is adjustable from 0.8V to 12V with a resistor-divider connected with FB, GND, and converter's output. Using 1% or better resistors for the resistor-divider is recommended. The output voltage is determined by:

$$V_{OUT} = 0.8 \times \left(1 + \frac{R_{TOP}}{R_{GND}}\right)$$

Where 0.8 is the reference voltage, R_{TOP} is the resistor connected from converter's output to FB, and R_{GND} is the resistor connected from FB to GND. Suggested R_{GND} is in the range from 1k to 20k Ω . To prevent stray pickup, locate resistors R_{TOP} and R_{GND} close to APW8713.

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value (L) determines the inductor ripple current, I_{RIPPLE} , and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage.

A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage. Besides, the inductor needs to have low DCR to reduce the loss of efficiency.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turnoff, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak inductor's current. These two voltages can be represented by:

$$\Delta C_{OUT} = \frac{I_{RIPPLE}}{8 \times C_{OUT} \times F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor (1 μ F) in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered.

To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from over-heating.

Application Information (Cont.)

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power-up, the input capacitors have to handle great amount of surge current. For low-duty notebook applications, ceramic capacitor is recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impedance PCB layout.

Thermal Consideration

Because the APW8802 build-in high-side and low-side MOSFET, the heat dissipated may exceed the maximum junction temperature of the part in applications. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the LX node will become high impedance. To avoid the APW8713 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The main power dissipated by the part is approximated:

$$P_{UPPER} = I_{OUT}^2(1+TC)(R_{DS(ON)})D + 0.5(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$

$$P_{LOWER} = I_{OUT}^2(1+TC)(R_{DS(ON)})(1-D)$$

I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_{SW} is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Note that both internal MOSFETs have conduction losses while the upper MOSFET include an additional transition loss. The switching interval, t_{SW} , is the function of the reverse transfer capacitance C_{RSS} . The $(1+TC)$ term factors in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "RDS(ON) vs. Temperature" curve of the power MOSFET. In APW8713 case, the $R_{DS(ON)}$ is about 30mW from specification table.

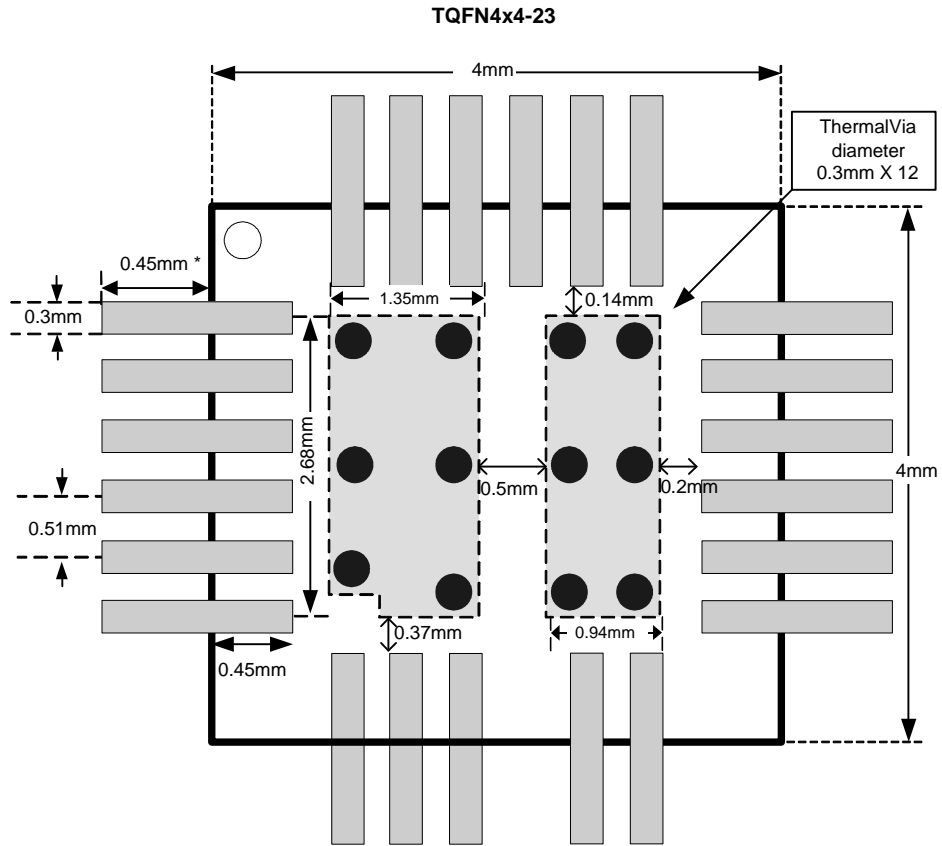
Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Besides, signal and power grounds are to be kept separate and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

- Keep the switching nodes (BOOT and LX) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with these traces on any layer.
- The large layout plane between the drain of the MOSFETs (VIN and LX nodes) can get better heat sinking.
- The current sense resistor should be close to OCSET pin to avoid parasitic capacitor effect and noise coupling.
- Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins.
- The output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors.
- Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces (BOOT and LX).

Application Information (Cont.)

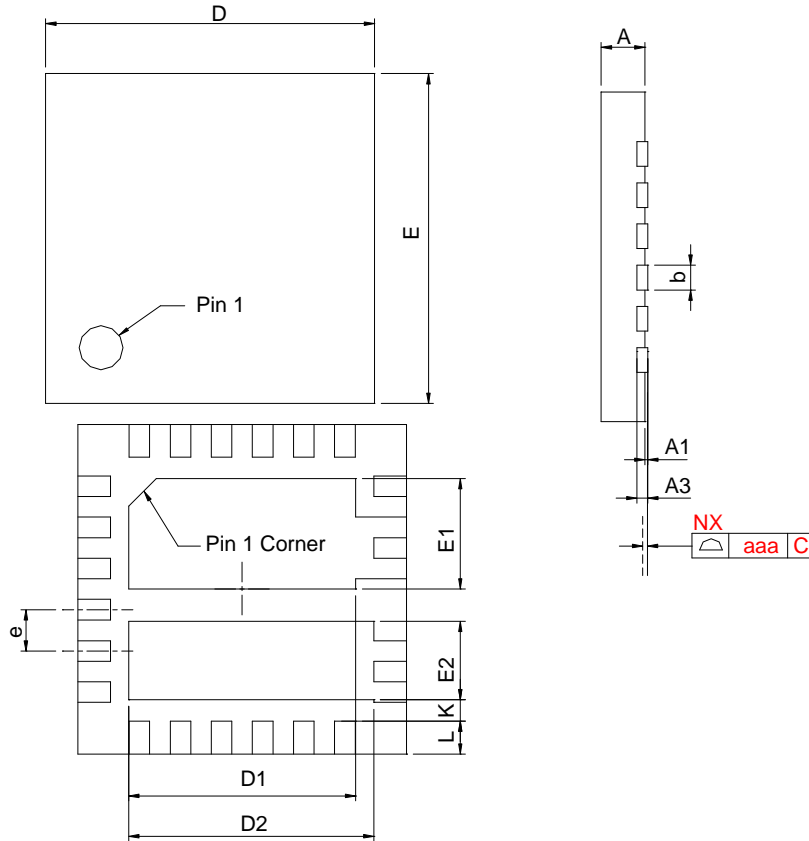
Recommended Minimum Footprint



* Just Recommend

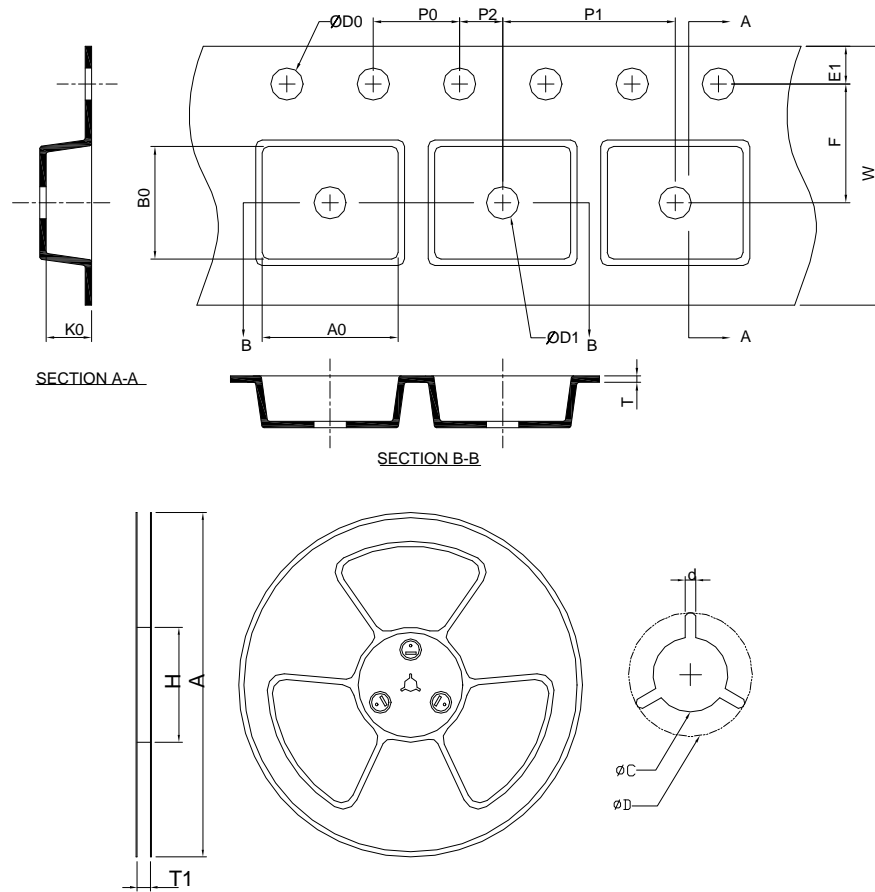
Package Information

TQFN4x4-23



| DIMENSIONS | TQFN4x4-23 | | | |
|------------|-------------|------|-----------|-------|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.70 | 0.80 | 0.028 | 0.032 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 |
| A3 | 0.20 REF | | 0.008 REF | |
| b | 0.20 | 0.30 | 0.008 | 0.012 |
| D | 3.90 | 4.10 | 0.154 | 0.161 |
| D1 | 2.58 | 2.78 | 0.102 | 0.109 |
| D2 | 2.95 | 3.15 | 0.116 | 0.124 |
| E | 3.90 | 4.10 | 0.154 | 0.161 |
| E1 | 1.24 | 1.44 | 0.049 | 0.057 |
| E2 | 0.85 | 1.05 | 0.033 | 0.041 |
| e | 0.50 BSC | | 0.020 BSC | |
| L | 0.35 | 0.45 | 0.014 | 0.018 |
| K | 0.20 | | 0.008 | |
| aaa | 0.08 | | 0.003 | |

Carrier Tape & Reel Dimensions



| Application | A | H | T1 | C | d | D | W | E1 | F |
|-------------|-------------|------------|--------------------|--------------------|----------|-------------------|------------|------------|------------|
| TQFN4x4 | 330.0 ±2.00 | 50 MIN. | 12.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 12.0 ±0.30 | 1.75 ±0.10 | 5.50 ±0.10 |
| | P0 | P1 | P2 | D0 | D1 | T | A0 | B0 | K0 |
| | 4.00 ±0.10 | 8.00 ±0.10 | 2.00 ±0.05 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.40 | 4.30 ±0.20 | 4.30 ±0.20 | 1.00 ±0.20 |

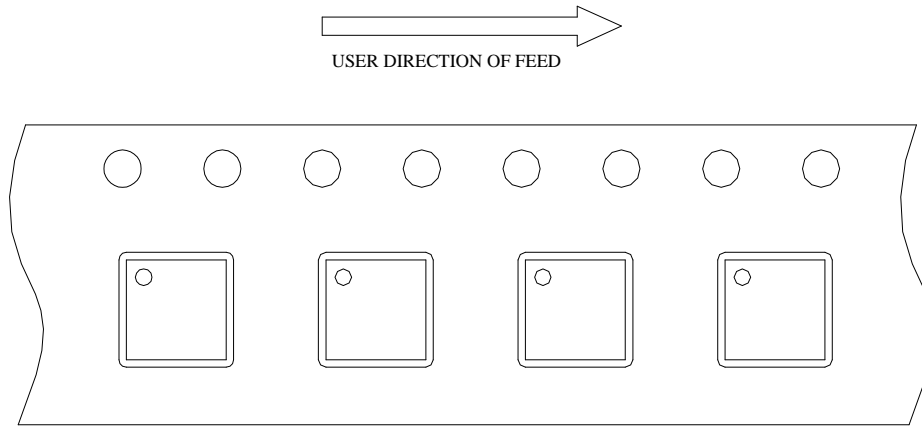
(mm)

Devices Per Unit

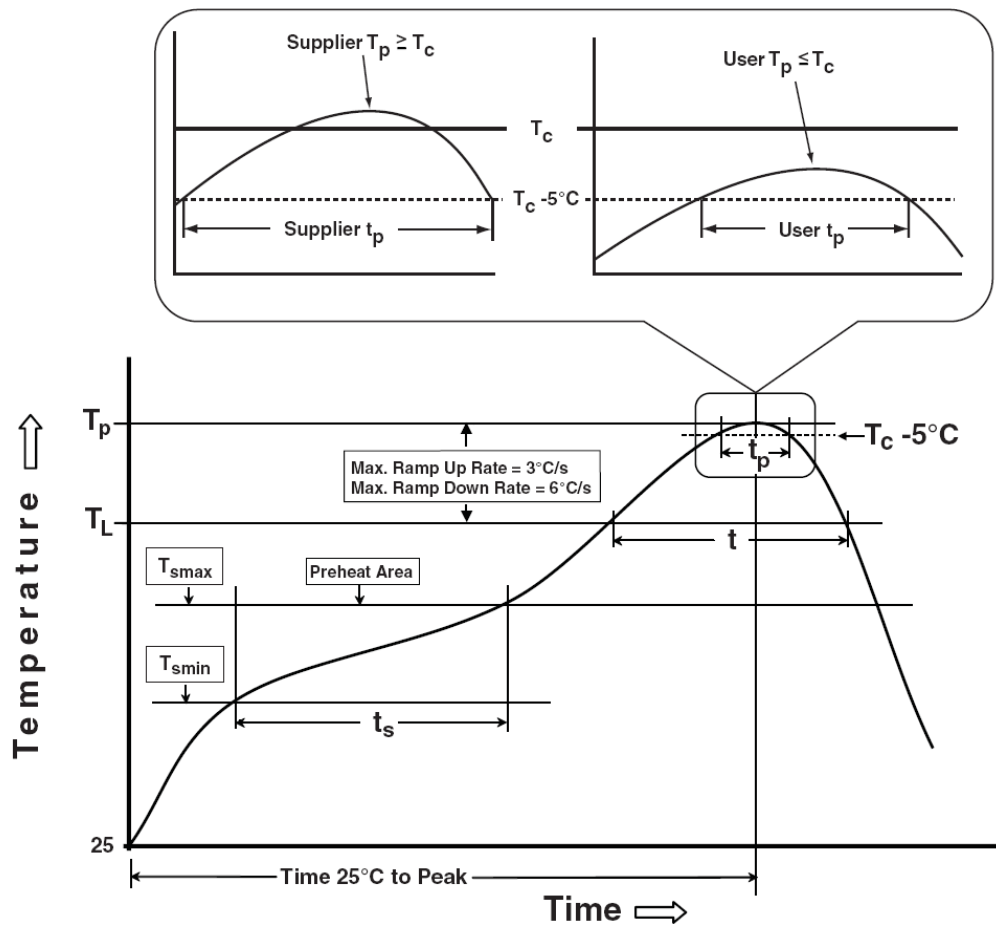
| Package Type | Unit | Quantity |
|--------------|-------------|----------|
| TQFN4x4 | Tape & Reel | 3000 |

Taping Direction Information

TQFN4x4



Classification Profile



Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|--|------------------------------------|------------------------------------|
| Preheat & Soak | | |
| Temperature min (T_{smin}) | 100 °C | 150 °C |
| Temperature max (T_{smax}) | 150 °C | 200 °C |
| Time (T_{smin} to T_{smax}) (t_s) | 60-120 seconds | 60-120 seconds |
| Average ramp-up rate (T_{smax} to T_p) | 3 °C/second max. | 3°C/second max. |
| Liquidous temperature (T_L) | 183 °C | 217 °C |
| Time at liquidous (t_L) | 60-150 seconds | 60-150 seconds |
| Peak package body Temperature (T_p)* | See Classification Temp in table 1 | See Classification Temp in table 2 |
| Time (t_p)** within 5°C of the specified classification temperature (T_c) | 20** seconds | 30** seconds |
| Average ramp-down rate (T_p to T_{smax}) | 6 °C/second max. | 6 °C/second max. |
| Time 25°C to peak temperature | 6 minutes max. | 8 minutes max. |
| * Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. | | |
| ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum. | | |

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

| Package Thickness | Volume mm ³ <350 | Volume mm ³ ≥350 |
|-------------------|--------------------------------|--------------------------------|
| <2.5 mm | 235 °C | 220 °C |
| ≥2.5 mm | 220 °C | 220 °C |

Table 2. Pb-free Process – Classification Temperatures (T_c)

| Package Thickness | Volume mm ³ <350 | Volume mm ³ 350-2000 | Volume mm ³ >2000 |
|-------------------|--------------------------------|------------------------------------|---------------------------------|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm – 2.5 mm | 260 °C | 250 °C | 245 °C |
| ≥2.5 mm | 250 °C | 245 °C | 245 °C |

Reliability Test Program

| Test item | Method | Description |
|---------------|--------------------|--|
| SOLDERABILITY | JESD-22, B102 | 5 Sec, 245°C |
| HOLT | JESD-22, A108 | 1000 Hrs, Bias @ $T_j=125^\circ\text{C}$ |
| PCT | JESD-22, A102 | 168 Hrs, 100%RH, 2atm, 121°C |
| TCT | JESD-22, A104 | 500 Cycles, -65°C~150°C |
| HBM | MIL-STD-883-3015.7 | VHBM 2KV |
| MM | JESD-22, A115 | VMM 200V |
| Latch-Up | JESD 78 | 10ms, 1 _{tr} 100mA |

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