

3N246

MINIATURE INTEGRAL DIODE ASSEMBLIES

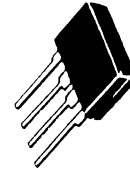
... with silicon rectifier chips interconnected and encapsulated into voidless rectifier bridge circuits.

- High Resistance to Shock and Vibration
- High Dielectric Strength
- Built-In Printed Circuit Board Stand-Offs
- UL Recognized
- RO_{JA} = 60°C/W



SINGLE-PHASE
 FULL-WAVE BRIDGE

1.0 AMPERE
 50-1000 VOLTS



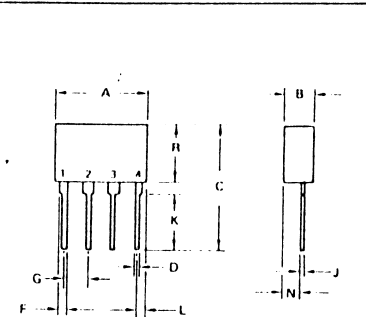
MAXIMUM RATINGS		3N246		Unit
Rating (Per Diode)	Symbol			
Peak Repetitive Reverse Voltage	VRRM	50		Volts
Working Peak Reverse Voltage	VRWM			
DC Blocking Voltage	VR			
DC Output Voltage	Vdc	32		Volts
Resistive Load	Vdc	50		Volts
Capacitive Load	Vdc			
Sine Wave RMS Input Voltage	VR(RMS)	35		Volts
Average Rectified Forward Current (single phase bridge operation, resistive load, 60 Hz, T _A = 75°C)	I _O	1.0		Amp
Non-Repetitive Peak Surge Current (Preceded and followed by rated current and voltage, T _A = 75°C)	I _{FSM}	30 (for 1 cycle)		Amp
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to +150		°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Instantaneous Forward Voltage (Per Diode) (I _F = 1.57 Amp, T _J = 25°C)	v _F	1.15	1.3	Volts
Reverse Current (Per Diode) (Rated V _R , T _A = 25°C)	I _R		10	µA

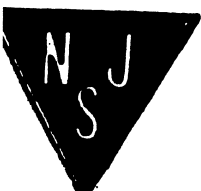
MECHANICAL CHARACTERISTICS

CASE: Transfer Moulded Plastic	MOUNTING POSITION: Any
POLARITY: Terminal-designation on case	WEIGHT: 1.8 grams (approx)
Pin 1 (+) for DC output	TERMINALS: Readily solderable
Pin 4 (-) for DC output	connections, corrosion resistant.
Pins 2 and 3 (AC) for AC input	



STYLE 1
 TERM 1 POS
 2 AC
 3 AC
 4 NEG

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.99	15.49	0.590	0.610
B	4.57	5.08	0.180	0.200
C		20.57		0.810
D	0.76	1.02	0.030	0.040
F	1.02	1.27	0.040	0.050
G	3.68	3.94	0.145	0.155
J	0.56	0.71	0.022	0.028
K		9.02		0.355
L	1.78	2.03	0.070	0.080
N	2.54	2.79	0.100	0.110
R	9.40	10.03	0.370	0.395



ELECTRICAL CHARACTERISTICS

 (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
Common Source Power Gain (VDD = 18 Vdc, VGG = 7.0 Vdc, f = 200 MHz) (VDD = 24 Vdc, VGG = 6.0 Vdc, f = 45 MHz) (VDD = 24 Vdc, VGG = 6.0 Vdc, f = 45 MHz) (VDD = 18 Vdc, f _{LO} = 245 MHz, f _{RF} = 200 MHz)	3N211	G _{ps}	24	35	dB
	3N211		29	37	
	3N213	27	35		
	3N212	G _c (6)	21	28	
Bandwidth (VDD = 18 Vdc, VGG = 7.0 Vdc, f = 200 MHz) (VDD = 18 Vdc, f _{LO} = 245 MHz, f _{RF} = 200 MHz) (VDD = 24 Vdc, VGG = 6.0 Vdc, f = 45 MHz)	3N211	BW	5.0	12	MHz
	3N212		4.0	7.0	
	3N211,213		3.5	6.0	
Gain Control Gate-Supply Voltage(5) (VDD = 18 Vdc, ΔG _{ps} = -30 dB, f = 200 MHz) (VDD = 24 Vdc, ΔG _{ps} = -30 dB, f = 45 MHz)	3N211	V _{GG} (GC)	—	-2.0	Vdc
	2N211,213		—	±1.0	

(1) Measured after five seconds of applied voltage.

(2) All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage limiting network is functioning properly.

(3) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

(4) This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating. The signal is applied to gate 1 with gate 2 at ac ground.

 (5) ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7.0 Volts (3N211) and V_{GG} = 6.0 Volts (3N213).

 (6) Power Gain Conversion. Amplitude at input from local oscillator is adjusted for maximum G_c.