Programmable Peripheral
ZPSD6XX(V) Family
Field-Programmable Microcontroller Peripherals with Embedded Micro⇔Cells™

Preliminary

Introduction

The ZPSD6XX(V) series is a complete family of Field Programmable Microcontroller Peripherals with Embedded Micro⇔Cell™ Programmable Logic. The devices are used to rapidly implement highly integrated embedded control systems. The device family offers a variety of functions including Zero Power PLDs (ZPLDs) with embedded Micro⇔Cells, dynamically reconfigurable I/O Ports, programmable power management, EPROM, SRAM and other functions.

Drawing from WSI's years of experience with microcontroller (MCU) applications, the new ZPSD6XX(V) product family radically simplifies the addition of programmable logic to embedded system designs. New innovative "microcontroller-macrocells", called Micro⇔Cells, bring inexpensive programmable logic to MCU-based embedded system designs. Because the Micro⇔Cells are directly connected to the system address/data bus, their NVM-based programmable logic is tightly coupled to the software programs running in the system MCU. The MCU's ability to communicate directly with the Micro⇔Cells at the Flip-Flop level makes ZPSD6XX(V) devices ideal for implementing the functions most frequently needed in embedded systems.

Communicating with Microcontrollers – Regardless of the function they perform, all microcontroller peripherals must communicate to the MCU. All MCUs require clock, data bus, chip select, and read or write signals. To implement these signals using current industry standard PLDs required the use of valuable product terms and macrocells in each PLD chip. In the case of most embedded system designs, this left so few remaining usable PLD resources to implement the peripheral function that designers dismissed the use of a PLD as too expensive.

The Micro⇔Cell directly connects its PLD logic to the MCU. The MCU then sees the PLD in the ZPSD6XX(V) as a decoded location in the address map. Direct read and write operations can be easily and simply performed. Functions like counters and serial ports can be constructed with programmable logic without any design time or resources lost interfacing to the MCU.

Key Features

- ❑ A simple, programmable interface to 8 or 16 bit microcontrollers using either multiplexed or non-multiplexed busses. The bus interface logic directly decodes microcontroller control signals. Microcontroller families supported include the Intel 8031, 80196, 80186, 80C251 and 80386EX; Motorola 68HC11, 68HC16, 68HC12 and 683XX; Philips 8031 and 8051XA; National 16000; Zilog Z80 and Z8; and Neuron 3150.
- ❑ Three ZPLDs (Zero Power PLDs) with 12 Output Micro⇔Cells and 23 Input Micro⇔Cells, 63 inputs and 129 product terms. The ZPSD6XX(V) ZPLDs may be used to efficiently implement a variety of logic functions including state machines and address decoders for internal and external control. The ZPLD also provides seven external chip select outputs.
- ❑ Embedded Input and Output Micro⇔Cells that enable efficient implementation of user defined system logic functions that require both microcontroller software and hardware interaction.
- ❑ Zero Power CMOS technology reduces the device standby current to 10 µA typical. Active power is as low as 0.8 mA per bus MHz.

Key Features (cont.)

- ❑ Twenty six individually configurable I/O Port pins. The Ports may be used as MCU I/Os, PLD I/Os, latched MCU address outputs or special function I/Os. Fifteen I/O port pins can be configured as open drain outputs.
- ❑ Internal EPROM in densities of 256 Kbit, 512 Kbit and 1 Mbit, configurable in eight or sixteen-bit widths. The EPROM is divided into eight equal-size blocks, accessible by user-specified addresses. The access time includes address latching and PLD decoding. The EPROM includes a low power option.
- ❑ Internal 4 Kbit SRAM can be configured in eight or sixteen-bit data widths. The SRAM retains data if power is lost by automatically switching to standby power.
- ❑ A page register expands the microcontroller address space by a factor of sixteen.
- ❑ A security bit prevents copying the ZPSD6XX(V) configuration and ZPLD logic as well as the EPROM contents.
- ❑ ZPSD6XXV(V) devices (2.7V to 5.5V operation) are specifically designed for low voltage and low power applications.
- ❑ The programmable Power Management Unit (PMU) supports two separate, low-power modes allowing operations with as little as 10 µA (at 5V V_{CC}). The device can automatically detect a lack of microcontroller activity and put the PSD into power down mode.
- ❑ The devices are available in EPROM versions. The ceramic package is ideal for prototyping and low-volume production, and in OTP versions for high-volume, low-cost applications.
- ❑ Package choices include 52 pin plastic chip carrier (J), ceramic chip carrier (L), and plastic quad flat pack (U).
- ❑ ZPSD6XX(V) family development is supported by the WSI's PC based PSDsoft™ design system. The software is MS-Windows® and Windows 95 compatible. The suite includes PSDabel™ (ABEL®), to specify the ZPLD logic, and an efficient fitter. The tool also includes the PSDsilosIII simulator from SIMUCAD™. The MagicPro® III programmer is an engineering development tool and can program any PSD device.

General Information

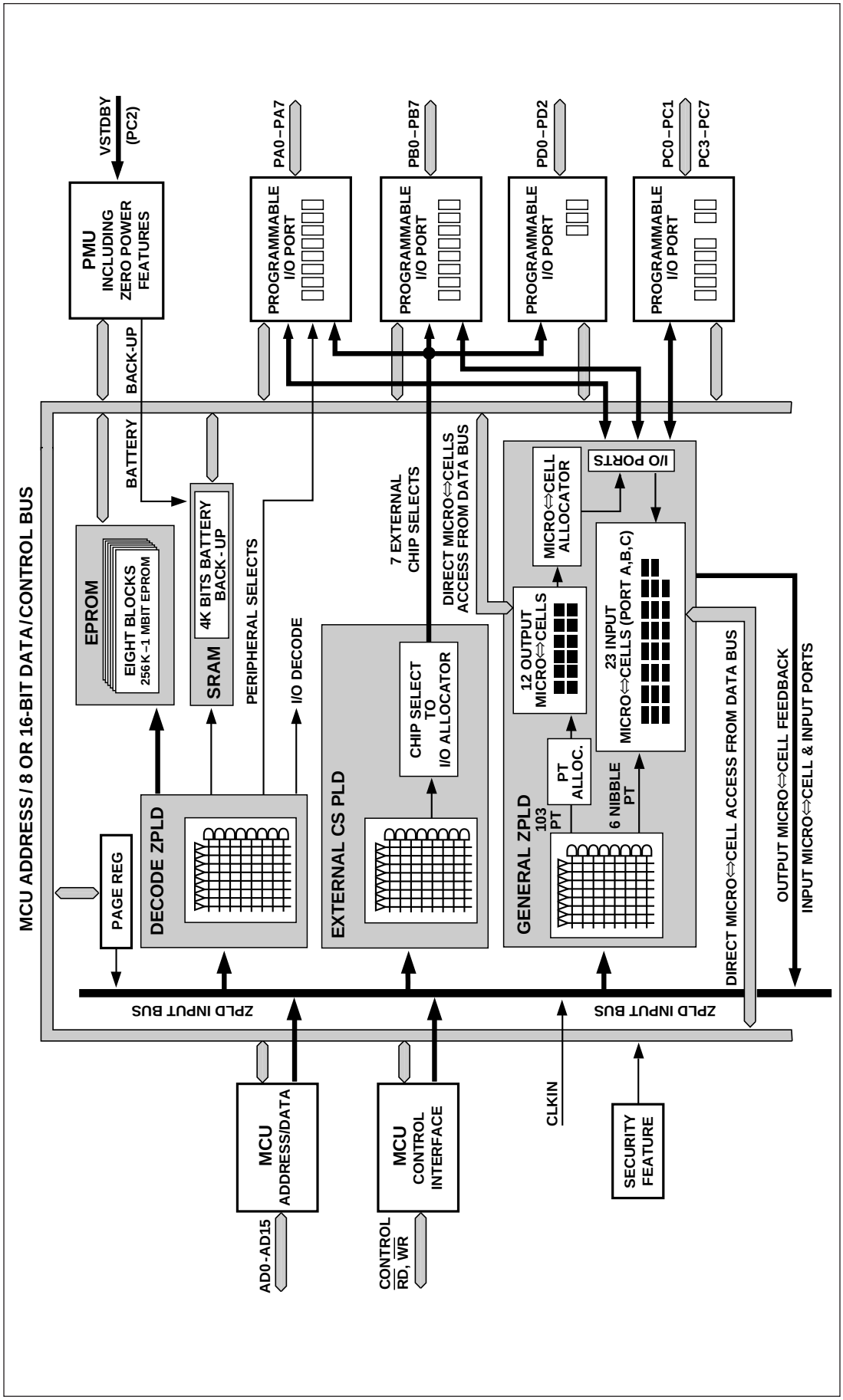
The ZPSD6XX(V) series of Field Programmable Microcontroller Peripherals combine an innovative architecture with advanced technology to provide a user-programmable, high-performance, low-power solution to microcontroller system design. The embedded input and output Micro⇔Cells enable efficient implementation of user defined logic functions that require both software and hardware interaction. The devices eliminate the need for discrete 'glue' logic and allow the development of entire systems using only a few highly integrated devices.

ZPSD Background

Portable and battery powered systems have recently become major embedded control application segments. As a result, the demand for electronic components having extremely low power consumption has increased dramatically. Recognizing this need, WSI, Inc. has developed a new ZPSD (Zero Power PSD) technology. ZPSD products virtually eliminate the DC component of power consumption reducing it to standby levels. Eliminating the DC component is the basis for the words "Zero Power" in the ZPSD name. ZPSD products also minimize the AC power component when the chip is changing states. The result is a programmable microcontroller peripheral family that replaces at least six discrete circuit functions while drawing much less power than a single EPROM.

Please refer to the revision block at the end of this document for updated information.

Figure 1. ZPSD6XX(V) Architecture



Integrated Power Management™ Operation

Upon each address or logic input change to the ZPSD, the device powers up from low power standby for a short time. The ZPSD consumes only the necessary power to deliver new logic or memory data to its outputs as a response to the input change. After the new outputs are stable, the ZPSD latches them and automatically reverts back to standby mode. The I_{CC} current flowing during standby mode and during DC operation is identical and is only a few microamperes.

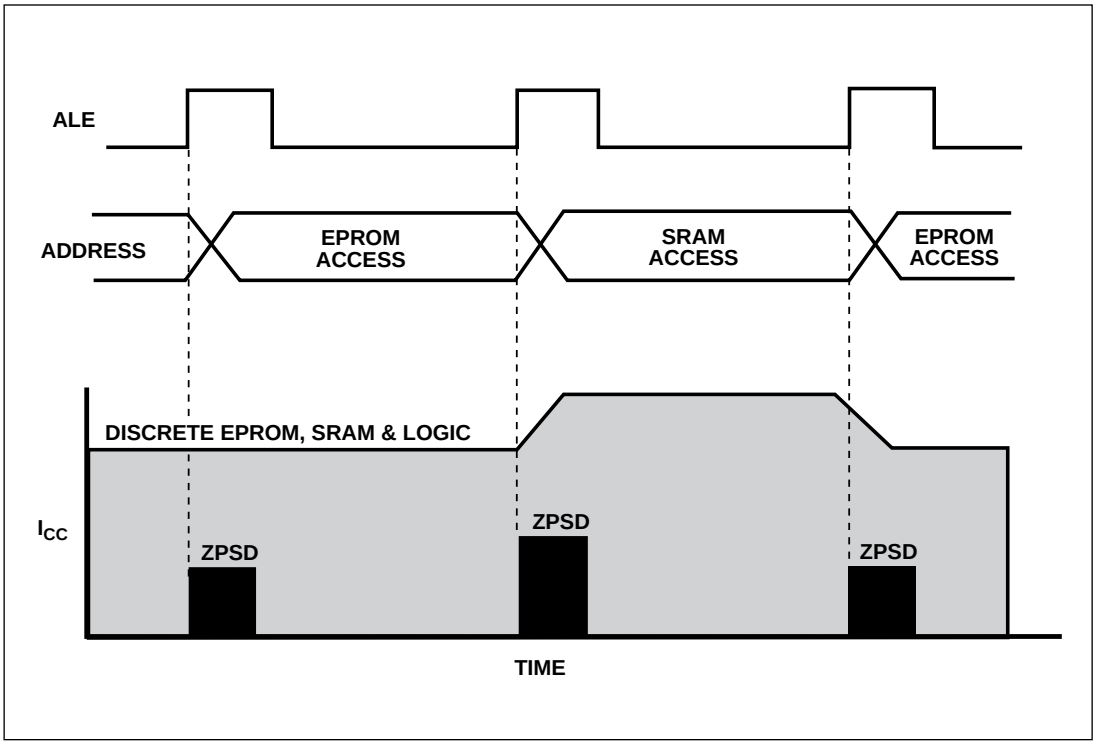
The ZPSD automatically reduces its DC current drain to these low levels and does not require controlling by the CSI (Chip Select) input. Disabling the CSI pin unconditionally forces the ZPSD to standby mode independent of other input transitions.

The only significant power consumption in the ZPSD occurs during AC operation. The ZPSD contains the first architecture to apply zero power techniques to memory circuit blocks as well as logic.

Figure 2 compares ZPSD zero power operation to the operation of a discrete solution. A standard microcontroller (MCU) bus cycle usually starts with an ALE (or AS) pulse and the generation of an address. The ZPSD detects the address transition and powers up for a very short time. The ZPSD then latches the outputs of the PAD, EPROM and SRAM to the new values. After finishing these operations, the ZPSD shuts off its internal power and enters standby mode. The time taken for the entire cycle is less than the ZPSD's "access time."

The ZPSD will stay in standby mode if the address does not change between bus cycles (for example, looping on a single address or a Halt operation). In an alternate system implementation using an EPROM, SRAM and other discrete components, the system will consume operating power during the entire bus cycle. This is because the chip select inputs on the memory devices are usually active throughout the entire cycle. The AC power consumption of the ZPSD may be calculated using the ALE frequency.

Figure 2. ZPSD Power Operation vs. Discrete Implementation

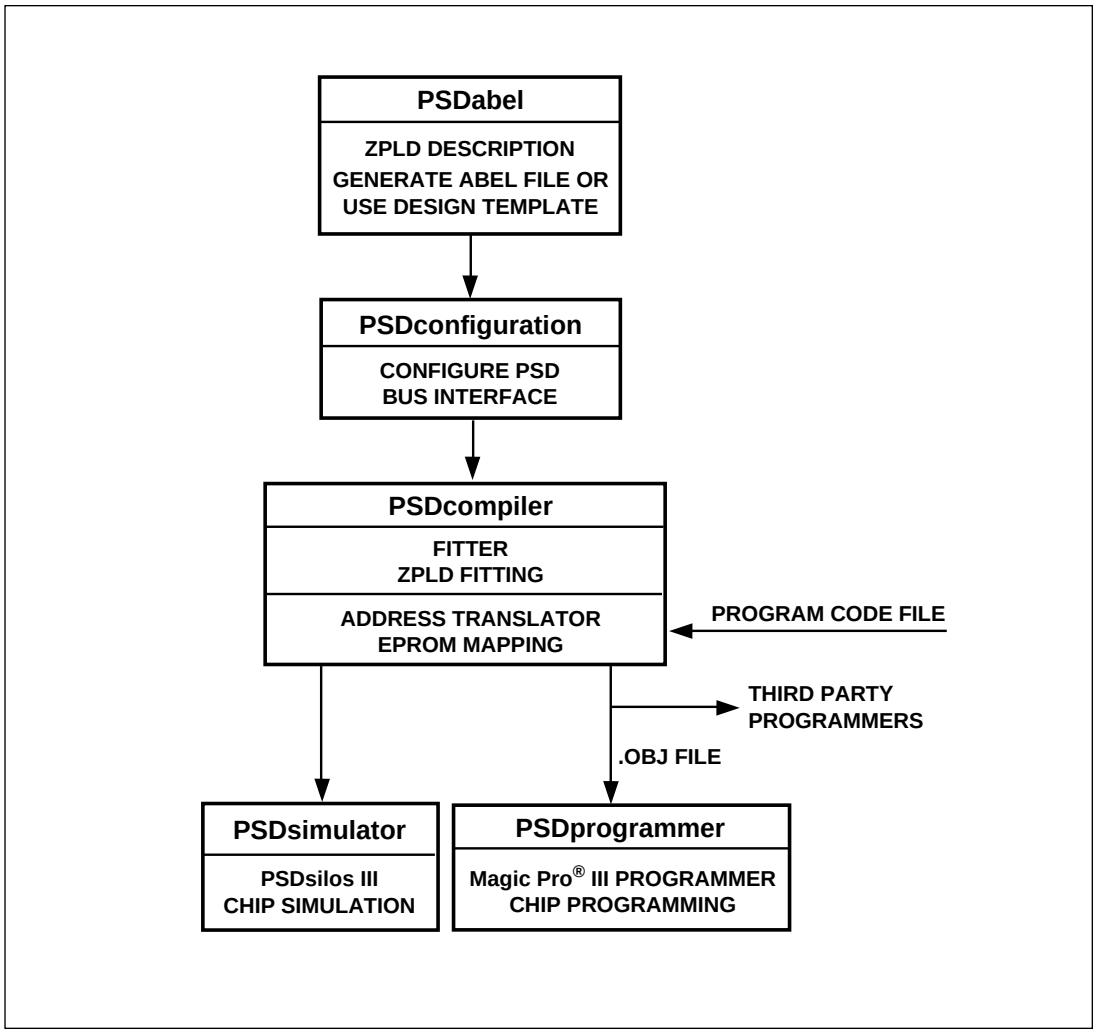


Development System

The ZPSD6XX(V) family is supported by the Windows-based PSDsoft Development System. The PSDsoft design flow is shown in Figure 3. The ZPLD design entry is done using PSDabel, which creates a minimized logic implementation, and provides logic simulation of the ZPLDs. The ZPSD6XX(V) Bus Interface and I/O Port configuration are entered in PSDconfiguration.

The PSDcompiler, comprised of a fitter and an address translator, generates an object file from the PSDabel, PSDconfiguration and MCU code files. The object file is then downloaded to a programmer (MagicPro III, Data I/O, or other third party programmer for device programming) or to a PSDsimulator (PSDsilos III Logic simulator) for device-level simulation.

Figure 3. PSDsoft Development Tools



Device Versions

The ZPSD6XX(V) window package versions are ideal for general purpose embedded systems development. The ZPSD6XX(V) plastic packaged OTP versions deliver the lowest cost ZPSD6XX(V) solution.

ZPSD6XX(V) Family

There are 6 devices in the ZPSD6XX(V) family. The part classifications are based on EPROM size and data bus width. The features of each part are listed in Table 1.

Table 1. ZPSD6XX(V) Product Matrix

Part #	Bus Width	I/O Pins	EPROM K Bit	SRAM K Bit
ZPSD601(V)E1	x8/x16	26	256	4
ZPSD611(V)E1	x8	26	256	4
ZPSD602(V)E1	x8/x16	26	512	4
ZPSD612(V)E1	x8	26	512	4
ZPSD603(V)E1	x8/x16	26	1024	4
ZPSD613(V)E1	x8	26	1024	4

Table 2. ZPSD6XX(V) Pin Descriptions

The following table describes the pin names and pin functions of the ZPSD6XX(V). Pins that have multiple names and/or functions are defined by configuration.

Pin Name	Pin	Type	Function Description
ADIO0–7	30–37	I/O	Address/Data Port, interface to Microcontroller Bus 1. Input pins for multiplexed low order address/data byte. ALE or AS latches address A0-7. The PSD drives data out only if read is active and one of the internal PSD functional blocks is selected. 2. Address A0-7 inputs for non-multiplexed bus or 80C251 mode 3. A4/D0-A11/D7 inputs in 80C51XA mode 4. Address (or latched address) inputs to ZPLD
ADIO8–15	39–46	I/O	Address/Data Port, interface to Microcontroller Bus 1. Address A8-15 inputs in 8-bit data bus mode, or as multiplexed high order address/data byte inputs in 16-bit data bus mode. ALE or AS latches address A8-15. The PSD drives data out only if read is active and one of the internal PSD functional blocks is selected. 2. Address A8-15 inputs in non-multiplexed bus mode 3. AD8-AD15 inputs in 80C251 mode 4. A12-A19 or A12/D8 - A19/D15 inputs in 80C51XA mode 5. Address (or latched address) inputs to ZPLD
CNTL0) ($\overline{WR}$, R_$\overline{W}$, $\overline{WRL}$)	47	I	Write Input pin with multiple configurations. Depending on the MCU interface selected, this pin can be: 1. $\overline{WR}$ – active low write input 2. R_$\overline{W}$ – read/write pin, low for write bus cycle 3. $\overline{WRL}$ – for 16 bit data bus only, write to low byte, active low 4. Control signal (CNTL0) input to ZPLD
CNTL1 ($\overline{RD}$, E, $\overline{DS}$, $\overline{LDS}$, $\overline{PSEN}$)	50	I	Read or Data Strobe Input pin with multiple configurations. Depending on the MCU interface selected, this pin can be: 1. $\overline{RD}$ – active low read input 2. E – E clock input. During a write bus cycle, E is high and R/W is low During a read bus cycle, E is high and R/W is high 3. $\overline{DS}$ – Data Strobe, active low 4. $\overline{LDS}$ – Strobe for low data byte, 16-bit data bus mode, active low 5. $\overline{PSEN}$ – Program Select Enable, active low in read bus cycle (80C251 configuration) 6. Control signal (CNTL1) input to ZPLD
CNTL2 ($\overline{PSEN}$, $\overline{BHE}$, $\overline{UDS}$, SIZ0)	49	I	Read or other Control input pin with multiple configurations. Depending on the MCU interface selected, this pin can be: 1. $\overline{PSEN}$ – Program Select enable, active low in code fetch bus cycle 2. $\overline{BHE}$ – High byte enable, 16-bit data bus 3. $\overline{UDS}$ – Strobe for high data byte, 16-bit data bus mode, active low 4. SIZ0 – Byte enable input 5. Control signal (CNTL2) input or general input to ZPLD

Table 2. ZPSD6XX(V) Pin Descriptions (cont.)

Pin Name	Pin	Type	Function Description
$\overline{\text{RESET}}$	48	I	Active low input. Resets I/O Ports, ZPLD Micro⇔Cells and some of the Configuration Registers. Must be active at power up.
PA0 PA1 PA2 PA3	29 28 27 25	I/O	Port A, PA0 – 3. This port is pin configurable and has multiple functions: 1. MCU I/O – standard output or input port 2. External chip select (ECSPLD) output, or input to GPLD 3. Latched address outputs (see Table 3) 4. As Address A0-3 inputs in 80C51XA mode 5. As Data Bus Port (D0–3) in non-multiplexed bus configuration 6. Peripheral I/O mode
PA4 PA5 PA6 PA7	24 23 22 21	I/O CMOS or Open Drain	Port A, PA4–7. This port is pin configurable and has multiple functions: 1. MCU I/O – standard output or input port 2. GPLD Micro⇔Cell (McellAB) output or input 3. Latched address outputs (see Table 3) 4. As Data Bus Port (D4–7) in non-multiplexed bus configuration 5. Peripheral I/O mode
PB0 PB1 PB2 PB3	7 6 5 4	I/O	Port B, PB0–3. This port is pin configurable and has multiple functions: 1. MCU I/O – standard output or input port 2. External chip select (ECSPLD) output, or input to GPLD 3. Latched address outputs (see Table 3) 4. As Data Bus Port (D8-11) in non-multiplexed bus configuration with 16-bit data bus
PB4 PB5 PB6 PB7	3 2 52 51	I/O CMOS or Open Drain	Port B, PB4–7. This port is pin configurable and has multiple functions: 1. MCU I/O – standard output or input port 2. GPLD Micro⇔Cell (McellAB) output or input 3. Latched address outputs (see Table 3) 4. As Data Bus Port (D12–15) in non-multiplexed bus configuration with 16-bit data bus
PC0 PC1 PC3 PC4 PC5 PC6 PC7 ($\overline{\text{WRH}}$)	20 19 17 14 13 12 11	I/O CMOS or Open Drain	Port C, PC0, PC1, PC3–7. This port is pin configurable and has multiple functions: 1. MCU I/O – standard output or input port 2. GPLD Micro⇔Cell (McellC) output or input 3. PC7 pin only ($\overline{\text{WRH}}$), Write strobe input for high byte. Active low, for 16-bit MCU with $\overline{\text{WRH}}$
PC2 (Vstby)	18	I	Port C pin PC2. Dedicated SRAM Standby Voltage Input. Pin should be grounded if Vstby is not required.

Table 2. ZPSD6XX(V) Pin Descriptions (cont.)

Pin Name	Pin	Type	Function Description
PD0 (ALE)	10	I/O	Port D Pin PD0 can be configured as: 1. ALE input - latches addresses on ADIO0–15 pins 2. MCU I/O 3. GPLD input 4. ECSPLD output
PD1 (CLKIN)	9	I/O	Port D Pin PD1 can be configured as: 1. MCU I/O 2. GPLD input 3. External chip select (ECSPLD) output 4. CLKIN clock input – clock input to the GPLD Micro⇔Cells, the APD power down counter and GPLD AND Array
PD2 ($\overline{CSI}$)	8	I/O	Port D Pin PD2 can be configured as: 1. MCU I/O 2. GPLD input 3. External (ECSPLD) output 4. $\overline{CSI}$ input – When low, the $\overline{CSI}$ enables the PSD EPROM/SRAM. When high, the EPROM/SRAM are disabled to conserve power
V_{CC}	15 38		Power pins
GND	1 16 26		Ground pins

Table 3. I/O Port Latched Address Output Assignments*

Microcontroller	Port A (3:0)	Port A (7:4)	Port B (3:0)	Port B (7:4)
8051XA (8-Bit)	N/A	Address [7:4]	Address [11:8]	N/A
80C251 (Page Mode)	N/A	N/A	Address [11:8]	Address [15:12]
All Other 8-Bit Multiplexed	Address [3:0]	Address [7:4]	Address [3:0]	Address [7:4]
8051XA (16-Bit)	N/A	Address [7:4]	Address [11:8]	Address [15:12]
All Other 16-Bit Multiplexed	Address [3:0]	Address [7:4]	Address [11:8]	Address [15:12]
8-bit Non-Multiplexed Bus	N/A	N/A	Address [3:0]	Address [7:4]

N/A = Not Applicable

*Refer to the I/O Port Section on how to enable the Latched Address Output function.

ZPSD6XX(V) Register Description and Address Offset

Tables 4 and 4A show the offset address to the ZPSD6XX(V)registers relative to the CSIOP base address. The CSIOP space is the 256 bytes of address that is allocated by the user to the internal ZPSD6XX(V) registers. Some Motorola 16-bit microcontrollers, including the M68HC16, M68302 and M683XX, have a different data byte orientation requiring separate address offset maps.

Table 4 shows the CSIOP address offsets for all MCUs except those from Motorola in 16-bit mode. Table 4A shows the address offsets for Motorola MCUs in 16-bit mode.

Table 4. Register Address Offset

Register Name	Port A	Port B	Port C	Port D	Other *	Description
Data In	00	01	10	11		Reads Port pin as input, MCU I/O input mode
Control	02	03				Selects mode between MCU I/O or Address Out
Data Out	04	05	12	13		Stores data for output to Port pins, MCU I/O output mode
Direction	06	07	14	15		Configures Port pin as input or output
Drive	08	09	16	17		Configures Port pin between CMOS, Open Drain and Slew rate
Input Micro⇔Cell	0A	0B	18			Reads Input Micro⇔Cell
Enable Out	0C	0D	1A			Reads the status of the output enable to the I/O Port driver
Output Micro⇔Cell	20	20	21			Read – reads output of Micro⇔Cells (McellC, McellAB) Write – loads Micro⇔cell Flip-Flops
PMMR0					B0	Power Management Register 0
PMMR1					B2	Power Management Register 1
Page					E0	Page Register
VM					E2	8031/PIO Configuration Register

*Other registers that are not part of the I/O ports.

ZPSD6XX(V) Register Description and Address Offset (cont.)

Table 4A. Register Address Offset for 16-Bit Motorola Microcontrollers in 16-Bit Mode

Register Name	Port A	Port B	Port C	Port D	Other *	Description
Data In	01	00	11	10		Reads Port pin as input, MCU I/O input mode
Control	03	02				Selects mode between MCU I/O or Address Out
Data Out	05	04	13	12		Stores data for output to Port pins, MCU I/O output mode
Direction	07	06	15	14		Configures Port pin as input or output
Drive	09	08	17	16		Configures Port pin between CMOS, Open Drain and Slew rate
Input Micro⇔Cell	0B	0A	19			Reads Input Micro⇔Cell
Enable Out	0D	0C	1B			Reads the status of the output enable to the I/O Port driver
Output Micro⇔Cell	21	21	20			Read – reads output of Micro⇔Cells (McellC, McellAB) Write – loads Micro⇔cell Flip-Flops
PMMR0					B1	Power Management Register 0
PMMR1					B3	Power Management Register 1
Page					E1	Page Register
VM					E3	8031/PIO Configuration Register

*Other registers that are not part of the I/O ports.

ZPSD6XX(V) Architectural Overview

ZPSD6XX(V) devices consist of several major functional blocks. Figure 1 shows the architecture of the ZPSD6XX(V) device family. The functions of each block are described briefly in the following sections. Many of the blocks perform multiple functions, and are user configurable.

Zero Power PLDs

The device contains three ZPLD blocks each optimized for a different function as shown in Table 5. The functional partitioning of the ZPLDs reduces power consumption, optimizes cost/performance and ease of design entry.

The Decode PLD (DPLD) is used to decode and generate chip selects for the ZPSD6XX(V) internal memory, registers and peripheral mode. The External Chip Select PLD (ECSPLD) is optimized to generate chip selects for devices external to the ZPSD6XX(V). The General Purpose PLD (GPLD) can implement user defined logic functions. The DPLD and ECSPLD have combinatorial outputs while the GPLD has 12 Output Micro⇔Cells. The ZPSD6XX(V) also has 23 Input Micro⇔Cells that can be configured as inputs to the ZPLD. The ZPLDs receive their inputs from the ZPLD Input bus and are differentiated by their output destinations, number of product terms, and Micro⇔Cells.

The ZPLDs are designed to consume minimum power by using Zero Power design techniques. The speed and power consumption of the ZPLD is controlled by the Turbo Bit in the PMMR0 Register that is set by the microcontroller.

I/O Ports

The ZPSD6XX(V) has 26 I/O pins divided among four ports. Each I/O pin can be individually configured to provide many functions. Ports A, B, C and D can be configured as standard MCU I/O ports, ZPLD I/O, or latched address outputs for microcontrollers using multiplexed address/data busses.

Ports A and B can also be configured as a data port for microcontrollers with a non-multiplexed bus. In these modes, Port A is connected to D0–7 and Port B to D8–15.

Table 5.

Name	Abbreviation	Inputs	Outputs	Product Terms
Decode PLD	DPLD	63	12	13
External Chip Select PLD	ECSPLD	24	7	7
General PLD	GPLD	63	12	109

ZPSD6XX(V) Architectural Overview (cont.)

Microcontroller Bus Interface

The ZPSD6XX(V) easily interfaces with most popular eight and sixteen-bit microcontrollers with either multiplexed or non-multiplexed address/data busses. The device is configured to respond to the microcontroller control signals which are also used as inputs to the ZPLDs.

Memory

The ZPSD6XX(V) contains EPROM and SRAM. The EPROM densities available are 256 Kbit, 512 Kbit and 1 Mbit. The memory space is divided into eight equally-sized blocks. Each block can be located in a different address space defined by the user. The access time of the EPROM includes the address latching and DPLD decoding.

The 4 Kbit SRAM may be used as a scratch pad memory and an extension of the microcontroller SRAM. The SRAM data is retained in the event of a system power down, provided a backup battery is connected to the Vstby pin (PC2). Switching from the V_{CC} supply to standby power occurs automatically when V_{CC} drops below Vstby voltage.

Page Register

The four-bit Page Register expands the address range of the microcontroller by sixteen times. The paged address can be used as part of the address space to access external memory and peripherals or internal EPROM, SRAM and I/O.

Power Management Unit

The Power Management Unit (PMU) in the ZPSD6XX(V) enables the user to control the power consumption on selected functional blocks based on system requirements. The PMU includes an Automatic Power Down unit (APD) that will turn off device functions due to microcontroller inactivity in one of two modes: the Power Down mode and Sleep mode.

Other power saving features, such as the CMiser and Turbo bits in the PMU, allow the EPROM/SRAM/ZPLD to operate at a slower rate to conserve power.

The ZPSD6XX(V) Functional Blocks

The ZPSD6XX(V) consists of five major functional blocks:

- ***ZPLD Block***
- ***Bus Interface***
- ***I/O Ports***
- ***Memory Block***
- ***Power Management Unit***

The functions of each block are described in the following sections. Many of the blocks perform multiple functions, and are user configurable.

ZPLDs

The Zero Power PLDs (ZPLDs) bring programmable logic functionality to the ZPSD6XX(V). After specifying the logic for the ZPLDs by using the PSDabel tool in PSDsoft, the logic configuration is programmed into the device and available when power is applied.

The ZPLDs (DPLD, ECSPLD and GPLD) consist of an AND array. The GPLD architecture includes 12 Output Micro⇔Cells in addition to the AND array. There are 23 Input Micro⇔Cells that can be configured as inputs to the ZPLD. Figure 4 shows the organization of the ZPLD.

The AND array is used to form product terms specified using the PSDabel tool in the PSDsoft development system. When the inputs used in a term are true, the output is active. The GPLD Input Bus consists of 63 signals as shown in Table 6. Both the true and complement value of inputs are available to the AND array. The DPLD and ECSPLD Input Busses consist of fewer inputs and are a subset of the 63 inputs.

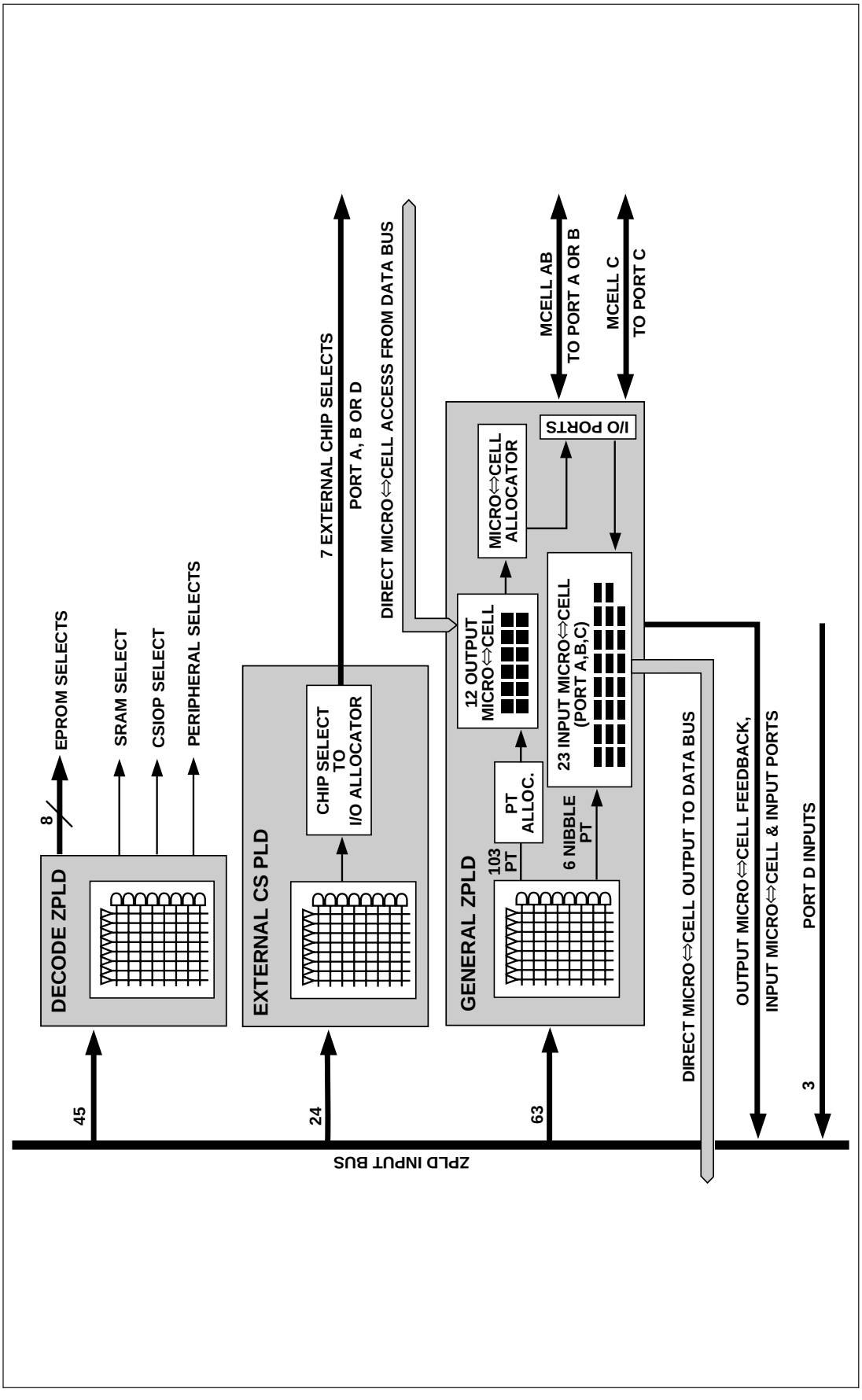
Table 6. GPLD Inputs

Input Source	Input Name	Number of Signals
MCU Address Bus	A[15:0]*	16
MCU Control Signals	CNTL[2:0]	3
Reset	RST	1
Power Down	PDN	1
I/O Ports Inputs (Input Micro⇔Cells)	PA[7:0], PB[7:0] PC[7:3], PC[1:0]	23
Port D Inputs	PD[2:0]	3
Page Register	PGR[3:0]	4
Port A or B Micro⇔Cell Feedback	MCELLAB.FB[7:4]	4
Port C Micro⇔Cell Feedback	MCELLC.FB[7:0]	8

***NOTE:** The address inputs are A[19:4] in 80C51XA mode.

ZPLDs
(cont.)

Figure 4. ZPLD Block Diagram



ZPLDs (cont.)

The ZPLDs can minimize power consumption by switching off when inputs remain unchanged for an extended time of about 70ns. Setting the Turbo mode bit to off (Bit 3 of the PMMR0 register) automatically places the ZPLDs into standby if no inputs are changing. Turbo off mode increases propagation delays while reducing power consumption. Refer to the Power Management Unit on how to set up the Turbo Bit. Power is further reduced by the PSDsoft development tools which disables unused product terms.

Each of the three ZPLDs has unique characteristics suited for its applications. They are described in the following sections.

Decode PLD

The Decode PLD (DPLD), shown in Figure 5, is used to select the internal ZPSD6XX(V) functions: EPROM blocks, SRAM, Registers (CSIOP) and the Port A Peripheral Mode. All the select signals are active high and have one product term, except ES7 which has two. The CSIOP is the select line for the ZPSD6XX(V) internal registers that occupies 256 bytes of memory space. A second level decoder selects a register based on the address inputs A[7-0].

Each EPROM block has its own chip select. The chip select of the eighth EPROM block has two product terms, ES7A and ES7B. This allows the eighth block to reside in two memory spaces, where ES7B can typically select reset vectors or configuration bytes that are stored in the MCU address space.

PSEL 0 & 1 are used as inputs to Port A to control the port's Peripheral I/O mode operation. Usually PSEL 0&1 are defined in term of the MCU address inputs. This mode is explained in the I/O Port section.

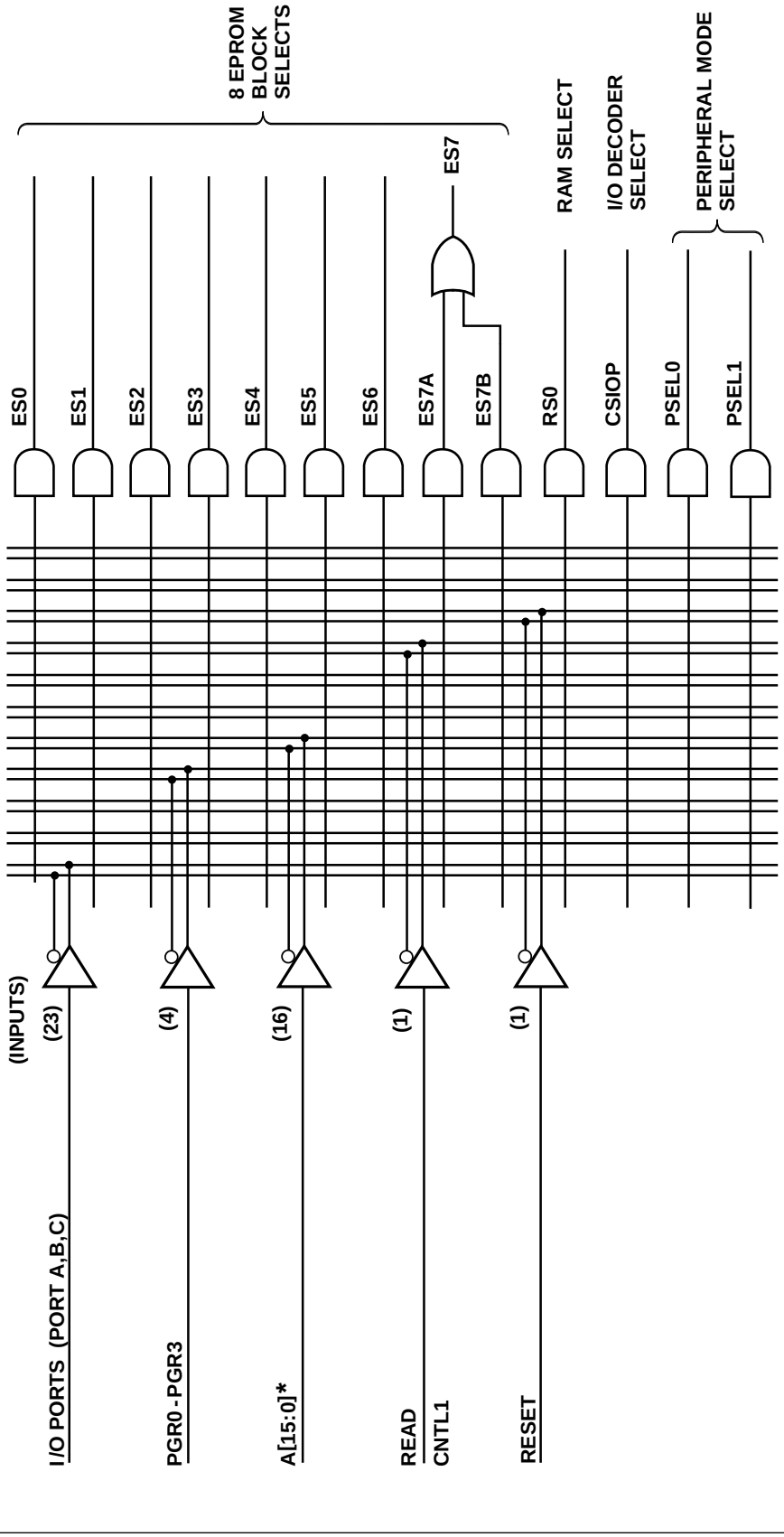
Table 7. DPLD Inputs

Input Source	Input Name	Number of Bits
MCU Address Bus	A[15:0]*	16
I/O Ports A, B, and C	PA[7:0], PB[7:0] PC[7:3], PC[1:0]	23
Page Register	PGR[3:0]	4
Control Signal	CNTL1 (Read)	1
Reset Pin	$\overline{\text{RESET}}$	1

***NOTE:** The address inputs are A[19:4] in 80C51XA mode, A[3:0] are assigned to Port A.

ZPLDs
(cont.)

Figure 5. DPLD Logic Array



ZPLDs (cont.)

External Chip Select PLD

The External Chip Select PLD (ECSPLD) provides the means to select external devices. The output buffer of the ECSPLD can be configured to operate in high slew rate by writing a “1” to the corresponding bit in the Drive Register. The slew rate is a measurement of the rise and fall times of the output. A higher slew rate means a faster output response while a lower slew rate is a slower response. Refer to Table 25 in the I/O Section for setting up the Drive Register.

Faster transitions are more likely to cause line reflections and system noise than slower rates. Adjusting the slew rate allows a trade-off between greater speed and noise sensitivity. The selection should be based on the performance requirements of the system and its noise characteristics. Set the corresponding bits in the Drive Register to “0” (for normal speed) or “1” (for fast drive). The default value is zero.

The ECSPLD has 24 inputs as shown in Table 8. Its outputs are combinatorial, of either polarity, and have one product term each as shown in Figure 6.

Table 8. ECSPLD Inputs

Input Source	Input Name	Number of Bits
MCU Address Bus	A[15:0]*	16
MCU Control Signals	CNTL[2:0]	3
Power Down Signal	PDN**	1
Page Register	PGR[3:0]	4

*In 80C51XA mode, the address inputs are A[19:4]
**APD output. When PDN is high, the PSD6XX(V) is in power down mode

The seven ECSPLD outputs may be driven off the device through Ports A, B, or D, as shown in Table 9, via the Micro⇔Cell Allocator. Port selection is specified in the PSDabel file or assigned by the PSDcompiler.

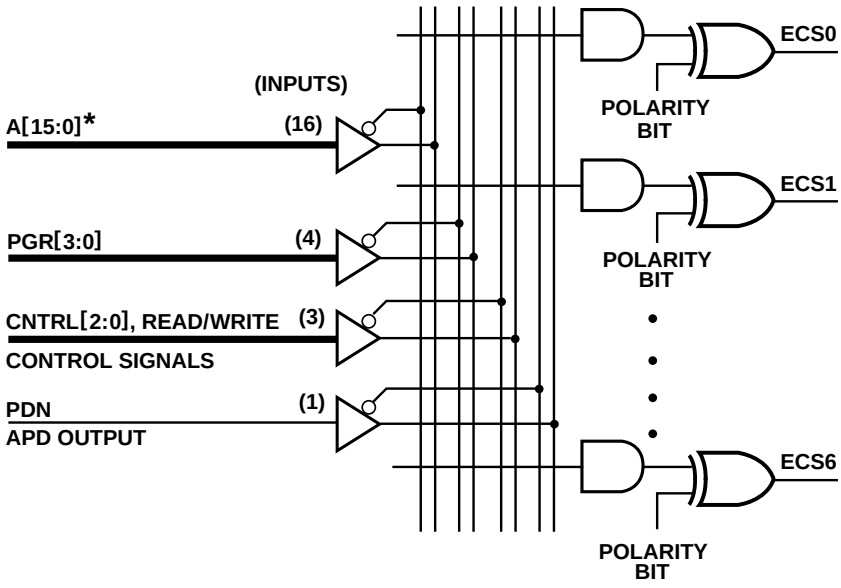
Table 9. ECSPLD Output Port Assignments

ECSPLD Output	Port A, B, or D Assignments
ECS0	PA0, PB0
ECS1	PA1, PB1
ECS2	PA2, PB2
ECS3	PA3, PB3
ECS4	PD0*
ECS5	PD1*
ECS6	PD2*

*Port D has no output enable (.oe) product terms for ECS4-6 outputs.

ZPLDs (cont.)

Figure 6. ECSPLD Logic Array



*In 80C51XA mode, the address inputs are A[19:4].

General PLD

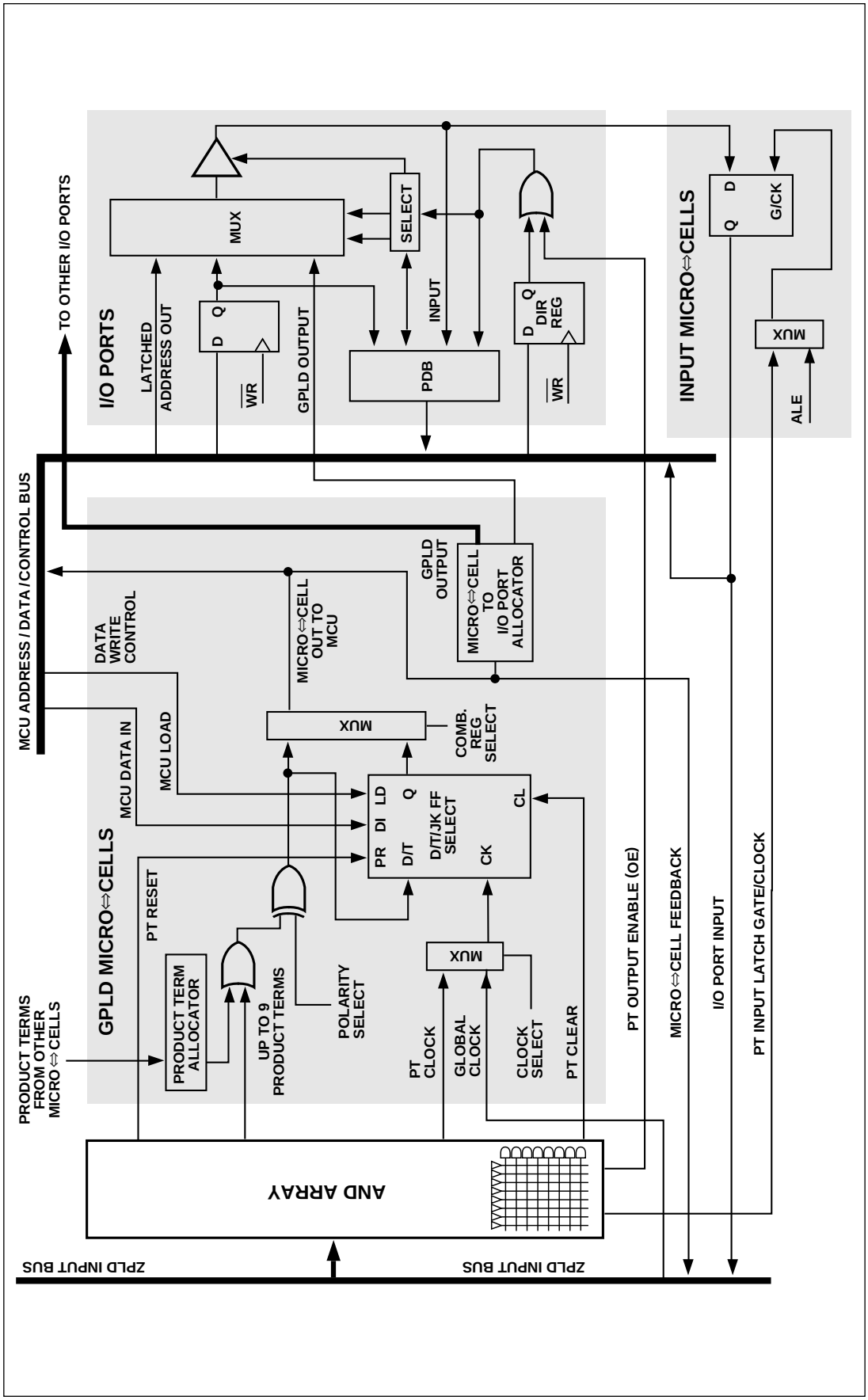
The General PLD (GPLD) is used to implement system logic such as MCU loadable counters, system mailboxes or handshaking protocols. In addition the GPLD can implement random logic and state machine functions.

The GPLD has Output and Input Micro⇔Cells. The GPLD, Output and Input Micro⇔Cells architectures appear in Figure 7 along with the Port. The Micro⇔Cells are configured using the PSDsoft development system. Like the other ZPLDs, the GPLD has an AND array which can generate up to 109 product terms, a maximum of nine product terms for each of the twelve Micro⇔Cells.

The Input and Output Micro⇔Cells are connected to the ZPSD6XX(V) internal data bus and can be directly accessed by the microcontroller. This enables the MCU software to load data into the Output Micro⇔Cells or read data from both the Input and Output Micro⇔Cells. This feature allows efficient implementation of system logic and eliminates the need to connect the data bus to the AND logic array as required in most standard PLD macrocell architectures.

ZPLDs
(cont.)

Figure 7. The GPLD and I/O Port



ZPLDs (cont.)

Output Micro⇔Cell

Eight of the Output Micro⇔Cells are connected to Port C pins (except PC2) and are named as McellC0-7. The remaining four Micro⇔Cells can be connected to Port A or Port B and are named as McellAB4-7. If an McellAB output is not assigned to a specific pin in PSDabel, the Micro⇔Cell Allocator will assign it to either Port A or B. Table 10 shows the Micro⇔Cells and Port assignment.

Table 10. Output Micro⇔Cell Port and Data Bit Assignments

Output Micro⇔Cell	Port Assignment	Native Product Terms	Max Borrowed Product Terms	Data Bit for Loading or Reading in 8-Bit Mode	Data Bit for Loading or Reading in 16-Bit Mode
McellC0	Port C0	4	5	D0	D8
McellC1	Port C1	4	5	D1	D9
McellC2	*	4	5	D2	D10
McellC3	Port C3	4	5	D3	D11
McellC4	Port C4	4	5	D4	D12
McellC5	Port C5	4	5	D5	D13
McellC6	Port C6	4	5	D6	D14
McellC7	Port C7	4	5	D7	D15
McellAB4	Port A4, B4	3	6	D4	D4
McellAB5	Port A5, B5	3	6	D5	D5
McellAB6	Port A6, B6	3	6	D6	D6
McellAB7	Port A7, B7	3	6	D7	D7

*Internal node only.

The Product Term Allocator

All Micro⇔Cells have the same basic cell architecture except McellC has four native product terms and McellAB has three product terms. The GPLD also has a Product Term Allocator with which the PSDcompiler can automatically borrow product terms from one Micro⇔Cell to another. The McellC may borrow up to five product terms from other Micro⇔Cells for a total of nine product terms. The McellAB has three native product terms and can borrow up to six product terms. Borrowing allows Micro⇔Cell outputs needing more product terms to use the unused product terms of others.

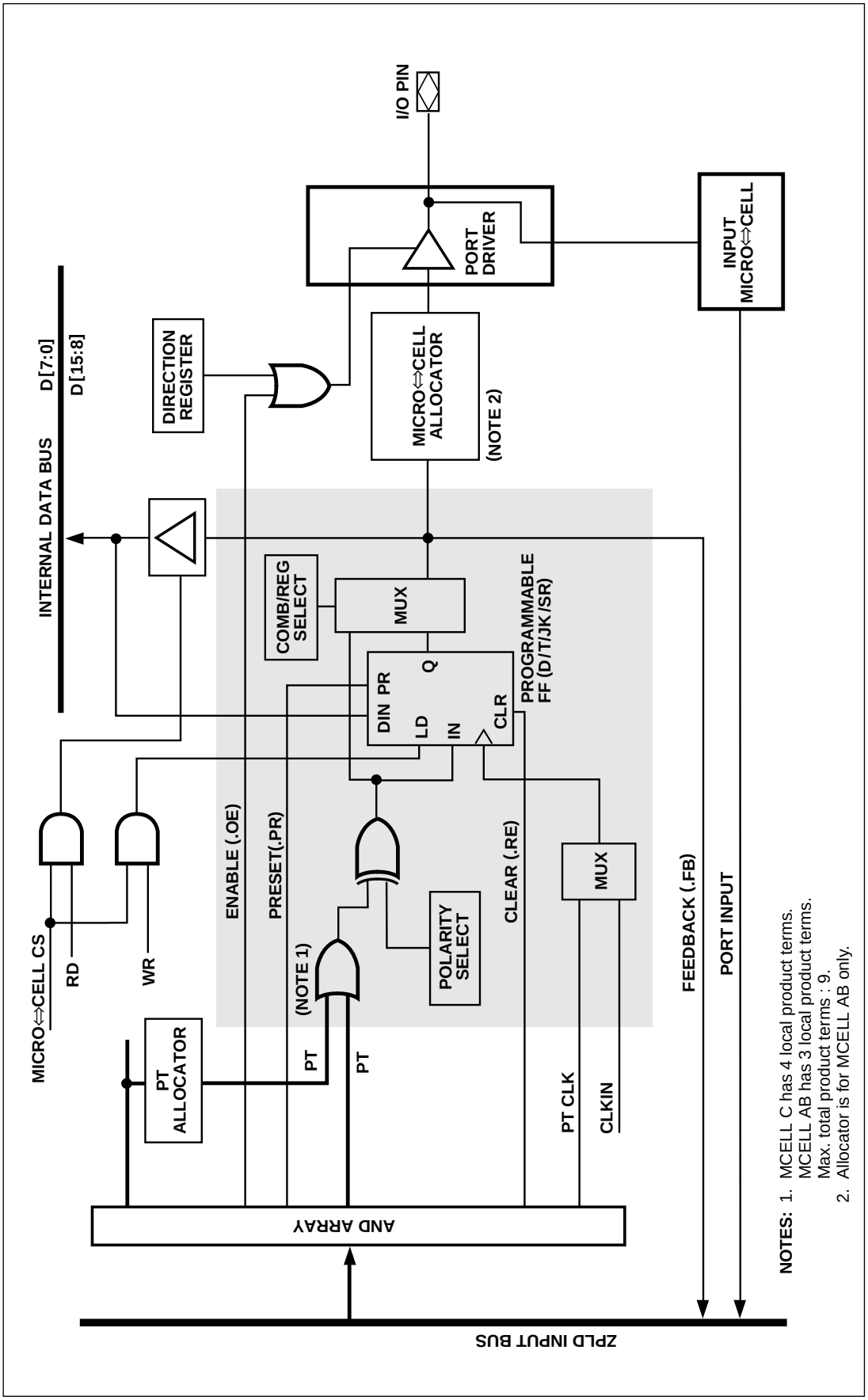
The architecture of the 12 Output Micro⇔Cells, as shown in Figure 8, consists of native product terms and borrowed product terms from other Micro⇔Cells. The polarity of the product term input is controlled by the XOR gate. The Micro⇔Cell can implement either sequential logic, using the Flip-Flop element, or combinatorial functions. The multiplexer selects the combinatorial or the sequential logic as the Micro⇔Cell output. The multiplexer output can drive a Port pin and has also a feedback path to the AND array inputs.

Micro⇔Cell Flip-Flop Type

The Flip-Flop in the Micro⇔Cell can be configured as a D, Toggle, JK or SR type by using PSDabel in PSDsoft. The Flip-Flop Clock, Preset and Clear inputs are driven from a product term of the AND array. Alternatively, the device clock input (CLKIN) can be used for the Flip-Flop. The Preset and Clear are active high inputs; the Flip-Flop is clocked by the rising edge of the clock input.

ZPLDs
(cont.)

Figure 8. GPLD Output Micro⇔Cell



ZPLDs (cont.)

Loading and Reading the Micro⇔Cells

The GPLD Micro⇔Cells occupy a memory location in the MCU address space as defined by the CSIOP (refer to the I/O section). The Flip-Flops in each of the 12 Micro⇔Cells can be loaded from the data bus by a microcontroller write bus cycle to the Micro⇔Cell (see I/O Port section for Micro⇔Cell Addresses). A “1” in the data bit that associates with the Micro⇔Cell will load a “1” to the Flip-Flop, a “0” in the data bit will load a “0” to the Flip-Flop. The loading bus cycle takes priority over other Flip-Flop inputs that include the Preset, Clear and clock. See Table 11 for the data bits that are connected to the Micro⇔Cells. The ability to load the Flip-Flops and read them back is useful in such applications as loadable counters, shift registers, mailboxes or handshaking protocols.

Table 11. Micro⇔Cell Flip-Flop Loading

LD	Din	Clk	In	PR	CLR	Q
1	1	X	X	X	X	1
1	0	X	X	X	X	0
0	X	Normal Flip-Flop Function				

NOTE: LD is “1” when the MCU writes to the Micro⇔Cell address

The Output Enable

The Micro⇔Cell can be connected to a ZPSD6XX(V) I/O pin as PLD output. The output enable of each of the Port pin output driver is controlled by a single product term (.oe) from the AND array ORed with the Direction Register output. Upon power up, if no output enable (.oe) equation is defined and the pin is declared as a ZPLD output in PSDsoft, the pin is enabled.

If the Micro⇔Cell output is declared as internal node and not as Port pin output in the PSDabel file, then the Port pin can be used for other I/O functions. The internal node feedback can be routed as an input to the AND array.

Input Micro⇔Cell

The Input Micro⇔Cells as shown in Figure 9 are used to latch, register or pass incoming Port signals prior to driving them onto the ZPLD Input bus. The outputs of these Micro⇔Cells can also be read by the microcontroller through the internal Data Bus. The GPLD has 23 Input Micro⇔Cells, one for each pin of Ports A, B and C (except PC2). The Input Micro⇔Cells are individually configurable.

The enable/clock for the latch and Flip-Flop is driven by a multiplexer whose inputs are a product term from the GPLD AND array and the MCU address strobe (ALE). Each product term output is used to latch/clock four Input Micro⇔Cells. Port inputs [3:0] can be controlled by one product term and [7:4] can be controlled by another one.

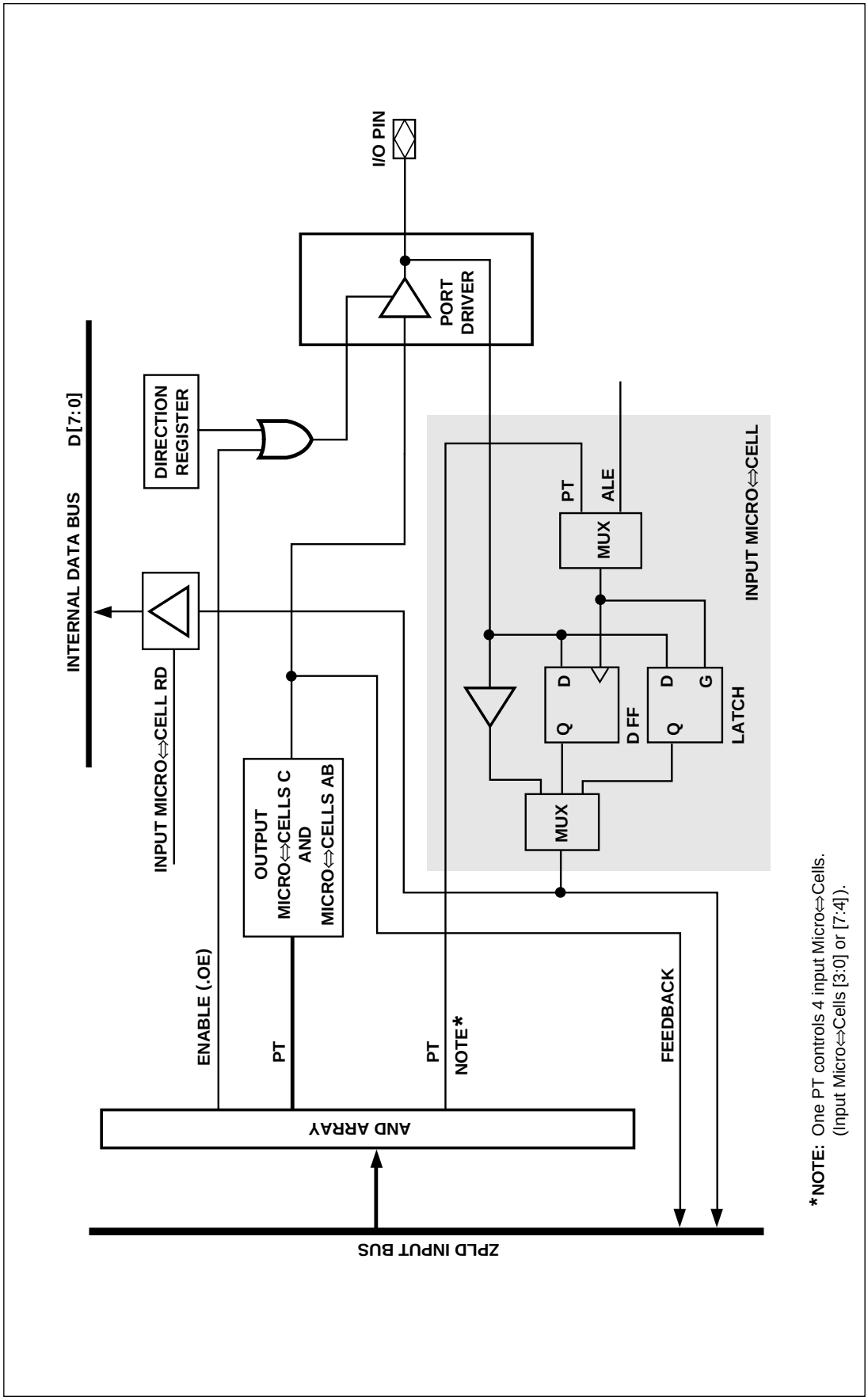
The Input Micro⇔Cell configurations are specified by equations written in PSDabel. Outputs of the Micro⇔Cells can be read by the microcontroller via the “Input Micro⇔Cell” buffer. See the I/O Port section on how to read the Micro⇔Cells.

Input Micro⇔Cells can use the ALE to latch the higher address bits (A31 – A16). The latched addresses are routed to the ZPLD as inputs.

The Input Micro⇔Cell is particularly useful in handshaking communication applications where two processors wish to pass data between each other through a commonly accessible storage. Figure 10 shows a typical configuration where the Master MCU writes to the Port A Data Out Register that is read by the Slave MCU via the activation of the Slave-Read output enable product term. The Slave MCU can write to Port A Input Micro⇔Cells by activating the Slave-WR product term. The Master MCU can then read the Input Micro⇔Cells. The Slave-Read and Slave-WR signals are product terms that are derived from the Slave MCU signals $\overline{RD}$, $\overline{WR}$, and Slave_CS.

ZPLDs
(cont.)

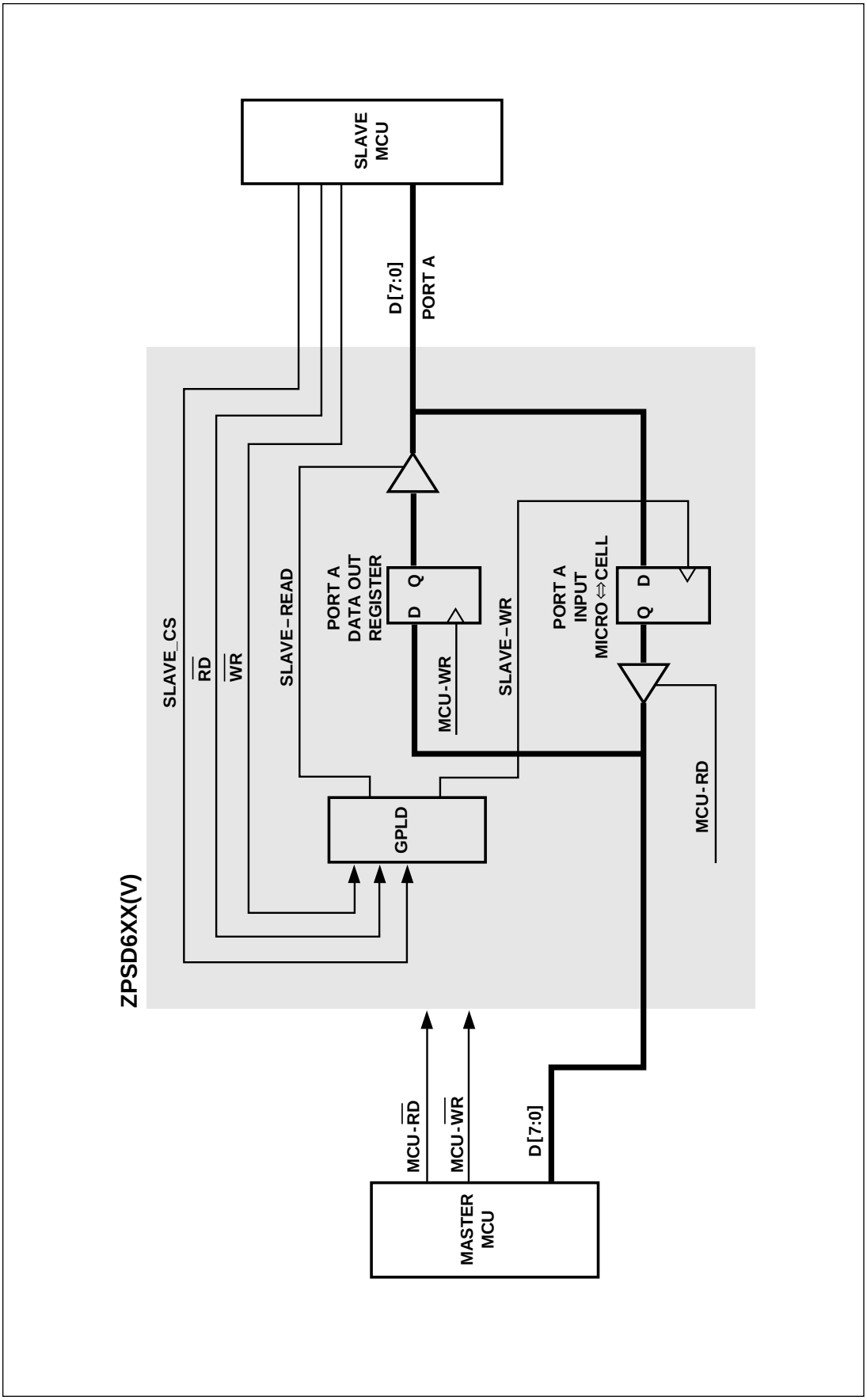
Figure 9. Input Micro⇔Cell



***NOTE:** One PT controls 4 input Micro⇔Cells. (Input Micro⇔Cells [3:0] or [7:4]).

ZPLDs
(cont.)

Figure 10. Handshaking Communication Using Input Micro⇔Cells



Bus Interface

The “no-glue logic” ZPSD6XX(V) Microcontroller Bus Interface can be directly connected to the most popular microcontrollers. Some of these microcontrollers with their bus types and control signals are shown in Table 12. The interface type is specified using the PSDsoft tools.

Table 12. Microcontroller Busses and Control Signals

MCU	Data Bus	CNTL0	CNTL1	CNTL2	PC7	PD0**	ADIO0	PA3–PA0
8031	8	$\overline{WR}$	$\overline{RD}$	$\overline{PSEN}$	*	ALE	A0	*
68330	8	R/W	$\overline{DS}$	*	*	ALE	A0	*
80198	8	$\overline{WR}$	$\overline{RD}$	*	*	ALE	A0	*
68HC11	8	R/W	E	*	*	AS	A0	*
80C51XA	8	$\overline{WR}$	$\overline{RD}$	$\overline{PSEN}$	*	ALE	A4	A3 – A0
80C251	8	$\overline{WR}$	$\overline{PSEN}$	*	*	ALE	A0	*
80C251	8	$\overline{WR}$	$\overline{RD}$	$\overline{PSEN}$	*	ALE	A0	*
Z8	8	R/$\overline{W}$	$\overline{DS}$	*	*	AS	A0	*
Neuron 3150	8	R/$\overline{W}$	$\overline{DS}$	*	*	*	A0	*
80196	16	$\overline{WRL}$	$\overline{RD}$	$\overline{BHE}$	*	ALE	A0	*
80196	16	$\overline{WRL}$	$\overline{RD}$	*	$\overline{WRH}$	ALE	A0	*
68HC12***	16	R/$\overline{W}$	E	A0	*	–	$\overline{LSTRB}$	*
68302	16	R/$\overline{W}$	$\overline{LDS}$	$\overline{UDS}$	*	AS	–	*
68330	16	R/$\overline{W}$	$\overline{DS}$	$\overline{BHE}$	*	AS	A0/BLE	*
68332	16	R/$\overline{W}$	$\overline{DS}$	SIZ0	*	AS	A0	*
80C51XA	16	$\overline{WRL}$	$\overline{RD}$	$\overline{PSEN}$	$\overline{WRH}$	ALE	A4/D0	A3 – A1
68LC302	16	$\overline{WEL}$	$\overline{OE}$		$\overline{WEH}$	AS	–	*
80186	16	$\overline{WR}$	$\overline{RD}$	$\overline{BHE}$	*	ALE	A0	*
80C166	16	$\overline{WR}$	$\overline{RD}$	$\overline{BHE}$	*	ALE	A0	*

*Not used CNTL2 pin can be configured as GPLD input. Other not used pins (PC7, PD0, PA3-0) can be configured for other I/O functions.

**ALE/AS input is optional for microcontrollers with a non-multiplexed bus.

***This configuration is for the 68HC12 with non-mux bus.

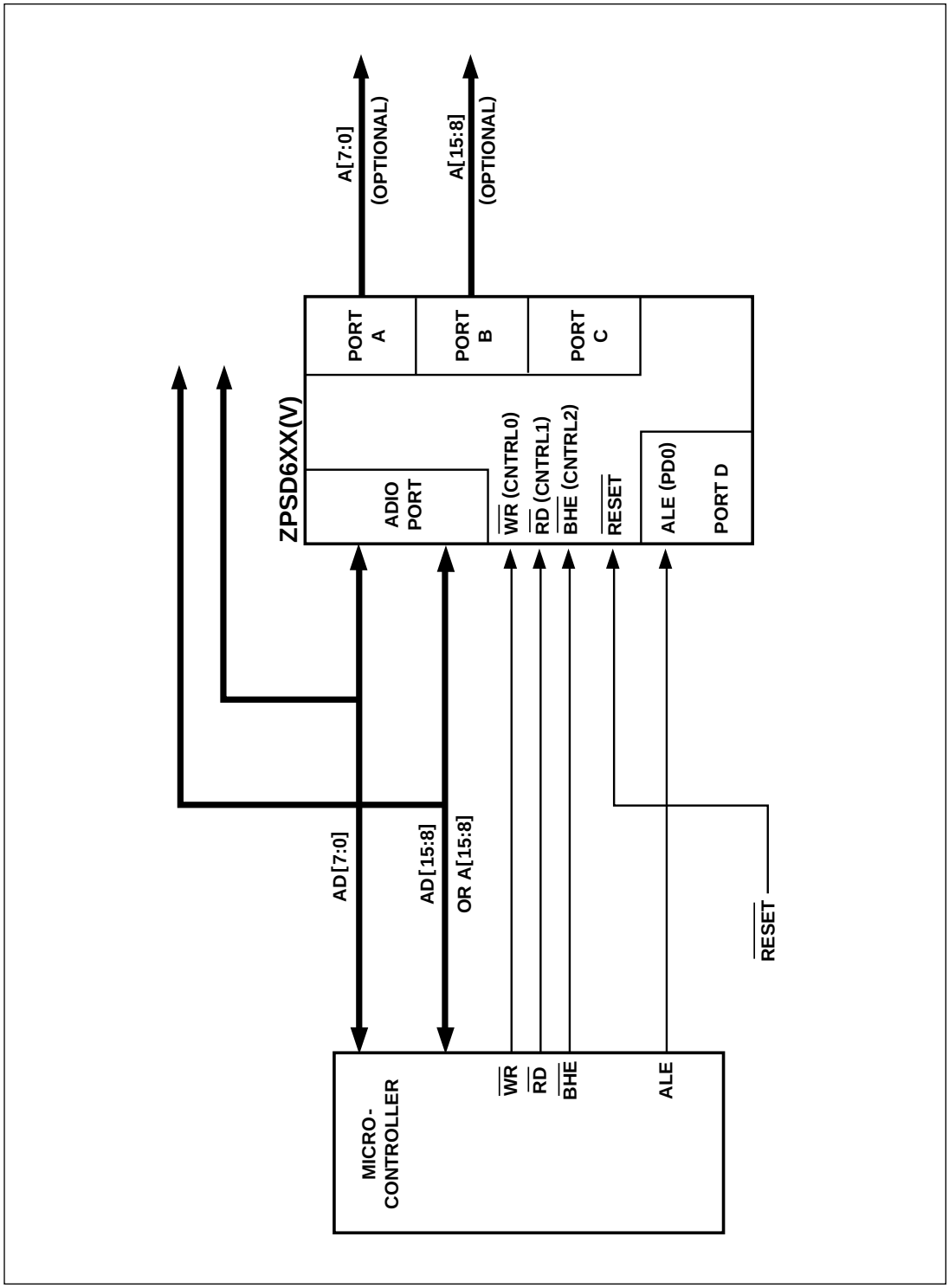
Table 12 shows the names of the ZPSD6XX(V) bus interface control pins and their functions. The control pins have multiple functions and can be configured to interface to many microcontrollers. Depending on the microcontroller, some of the control input pins are not required and may be used as GPLD input or other I/O functions. Specific examples of interfaces to different microcontrollers are provided in the following sections. For microcontrollers that have more than 16 address lines, Port A, B, or C pins may be used as additional address inputs.

Bus Interface (cont.)

ZPSD6XX(V) Interface To a Multiplexed Bus

Figure 11 shows an example of a system using a microcontroller with a multiplexed bus and a ZPSD6XX(V). The ADIO port on the ZPSD6XX(V) is connected directly to the microcontroller address/data bus. The bus may be multiplexed only on one byte (eight-bit data) or on both bytes (sixteen-bit data). The ALE latches the address lines internally; latched addresses can be brought out to Port A or B. The ZPSD6XX(V) drives the ADIO data bus only when one of its internal resources is accessed and the RD input is active.

Figure 11. An Example of a Typical Multiplexed Bus Interface, 8 or 16-Bit Data Bus

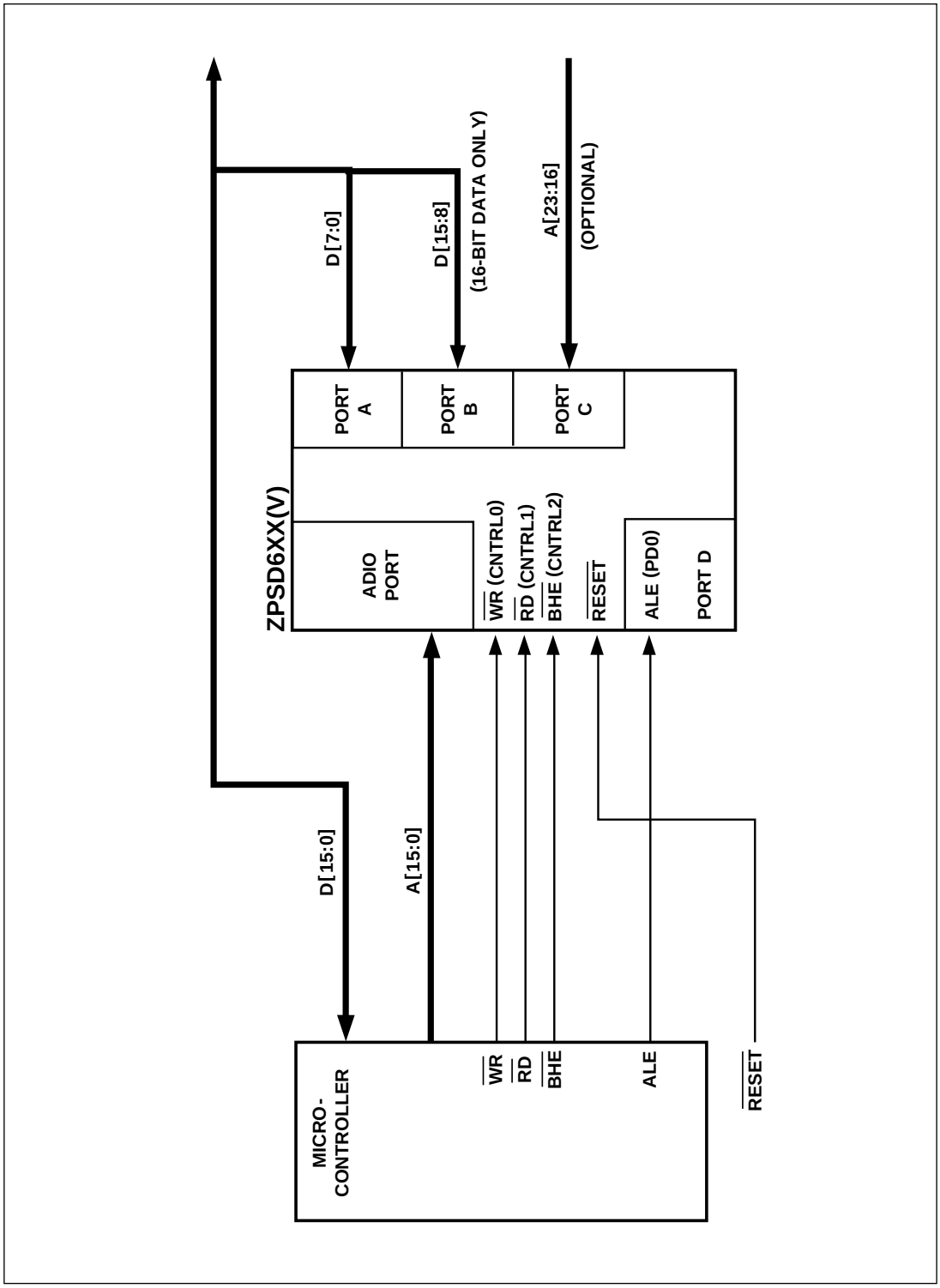


Bus Interface (cont.)

ZPSD6XX(V) Interface To a Non-Multiplexed Bus

Figure 11 shows an example of a system using a microcontroller with a non-multiplexed bus and a ZPSD6XX(V). The address bus is connected to the ADIO Port, and the data bus is connected to Port A (D[7:0]) and to Ports B (D[15:8], 16-bit data bus only). The data Ports are in a tri-state mode when the ZPSD6XX(V) is not accessed by the microcontroller. Should the system address bus exceed sixteen bits, Port A, B, or C may be used as additional address inputs.

Figure 12. An Example of a Typical Non-Multiplexed Bus Interface, 8 or 16-Bit Data Bus



Bus Interface (cont.)

Data Byte Enable Reference

Microcontrollers have different data byte orientations. The following tables show how the ZPSD6XX(V) interprets byte/word operation in different write bus configurations. Even-byte refers to locations with address A0 equal to zero and odd byte as locations with A0 equal to one.

Table 13. 8-Bit Data Bus

BHE	A0	D7 – D0
X	0	Even Byte
X	1	Odd Byte

Table 14. 16-Bit Data Bus With $\overline{BHE}$

BHE	A0	D15 – D8	D7 – D0
0	0	Odd Byte	Even Byte
0	1	Odd Byte	–
1	0	–	Even Byte

Table 15. 16-Bit Data Bus With $\overline{WRH}$ and $\overline{WRL}$

WRH	WRL	D15 – D8	D7 – D0
0	0	Odd Byte	Even Byte
0	1	Odd Byte	–
1	0	–	Even Byte

Table 16. 16-Bit Data Bus With SIZ0, A0 (Motorola MCU)

SIZ0	A0	D15 – D8	D7 – D0
0	0	Even Byte	Odd Byte
1	0	Even Byte	–
1	1	–	Odd Byte

Table 17. 16-Bit Data Bus With $\overline{UDS}$, $\overline{LDS}$ (Motorola MCU)

LDS	UDS	D15 – D8	D7 – D0
0	0	Even Byte	Odd Byte
1	0	Even Byte	–
0	1	–	Odd Byte

Bus Interface (cont.)

Microcontroller Interface Examples

Figures 13 through 20 show examples of the basic connections between the ZPSD6XX(V) and some popular microcontrollers. The ZPSD6XX(V) control input pins are labeled as the microcontroller function for which they are configured. The MCU interface is specified using the PSDsoft tools. The PC2 pin should be grounded if Vstby is not used.

80C31

Figure 13 shows the interface to the 80C31 which has an 8-bit multiplexed address/data bus. The lower address byte is multiplexed with the data bus. The microcontroller $\overline{RD}$ and WR signals may be used for accessing internal SRAM and I/O Ports while the $\overline{PSEN}$ signal is used to read the EPROM. The ALE input (Port D PD0) latches the address. Refer to the Memory Section for additional 80C31 operating modes.

68HC11

Figure 14 shows an interface to an 68HC11 where the ZPSD6XX(V) is configured in 8-bit multiplexed mode with E and R/W settings. The ECSPLD can generate the READ and WR signals for external on board devices. The CNTL2 pin is not used and can be used as a ZPLD input.

80C196

In Figure 15, the Intel 80C196 microcontroller, which has a multiplexed sixteen-bit bus, is shown connected to a ZPSD6XX(V). The $\overline{BHE}$ signal is used for high data byte selection. Port pins can be configured in the PSDabel as ZPLD outputs to control the READY and BUSWIDTH pins of the 80C196.

MC68331

Figure 16 shows a Motorola MC68331 with non-multiplexed sixteen-bit data bus and 24-bit address bus. The data bus from the MC68331 is connected to Port A (D0–7) and Port B (D8–15). The SIZ0 and A0 inputs determine the high/low byte selection.

80C51XA

The Philips 80C51XA microcontroller family has an 8 or 16 bit multiplexed bus that supports burst cycles. Address bits A[3:0] are not multiplexed while A[19:4] are multiplexed with data bits D[15:0] in 16-bit mode. In 8-bit mode, A[11:4] are multiplexed with data bits D[7:0].

The 80C51XA can be configured to operate with a ZPSD6XX(V) in an 8-bit (shown in Figure 17) or 16-bit (shown in Figure 18) data mode. With a 16-bit data bus, the 80C51XA's $\overline{WRH}$ pin is connected to the PC7 pin on the ZPSD6XX(V). Pin PA0 is grounded and not used.

The 80C51XA improves bus throughput and performance by executing Burst cycles to fetch codes from memory. In Burst cycles, address A19–4 are latched internally by the ZPSD6XX(V), while the 80C51XA changes the A3–0 lines to sequentially fetch up to 16 bytes of code. The PSD access time is then measured from address A3–A0 valid to data in valid. The ZPSD6XX(V) bus timing requirement in Burst cycle is identical to the normal bus cycle except the address set up or hold time with respect to ALE is not required.

Bus Interface (cont.)

80C251

The Intel 80C251 microcontroller features a user-configurable bus interface with four possible bus configurations as shown in Table 18.

Table 18. 80C251 Configurations

Configuration	80C251 Read/Write Pins	Connecting to PSD6XX(V) Pins	Page Mode
1	$\overline{WR}$ $\overline{RD}$ $\overline{PSEN}$	CNTL0 CNTL1 CNTL2	Non-Page Mode, 80C31 compatible A[7:0] multiplex with D[7:0}
2	$\overline{WR}$ $\overline{PSEN}$ only	CNTL0 CNTL1	Non-Page Mode A[7:0] multiplex with D[7:0}
3	$\overline{WR}$ $\overline{PSEN}$ only	CNTL0 CNTL1	Page Mode A[15:8] multiplex with D[7:0}
4	$\overline{WR}$ $\overline{RD}$ $\overline{PSEN}$	CNTL0 CNTL1 CNTL2	Page Mode A[15:8] multiplex with D[7:0}

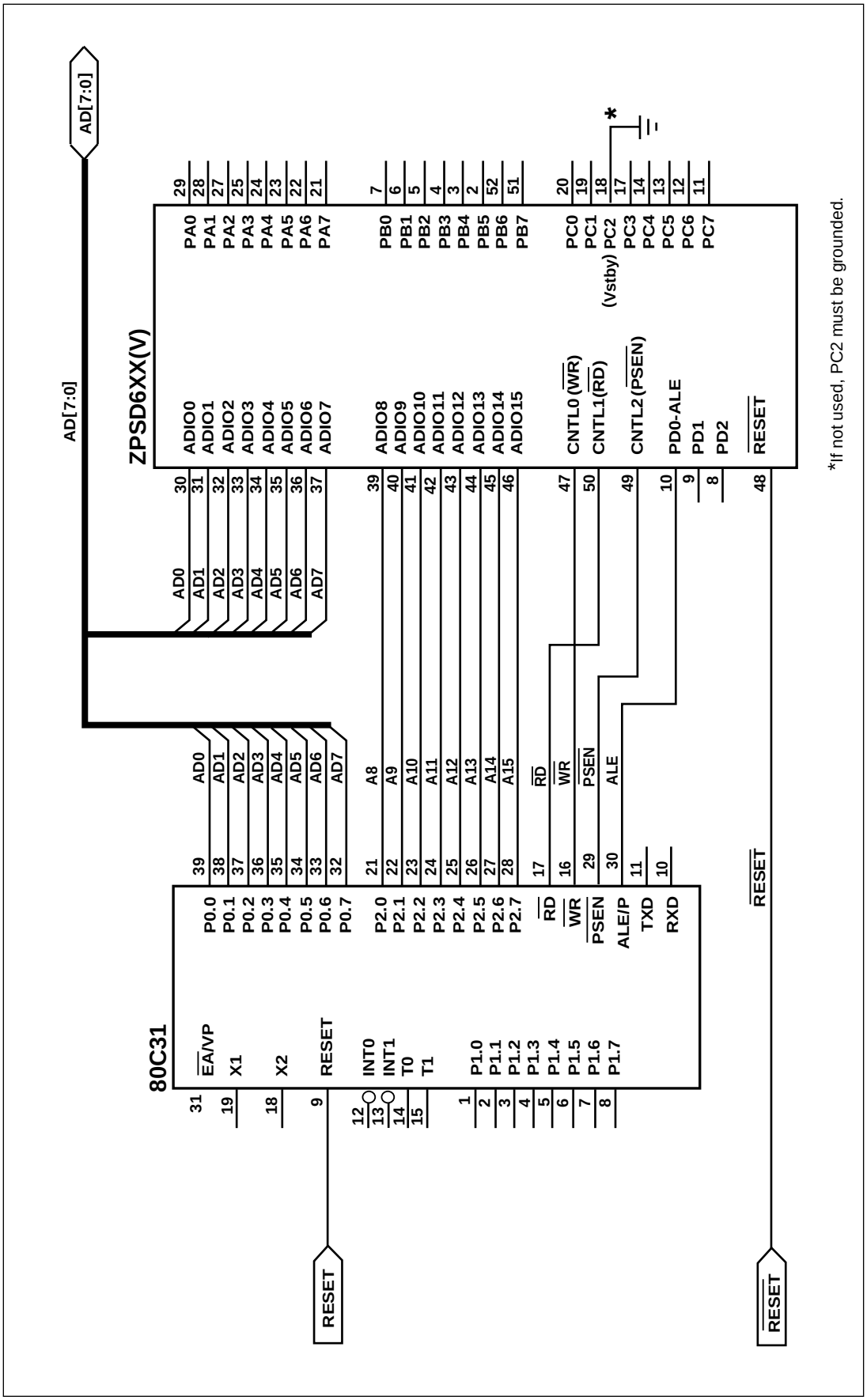
Configuration 1 is 80C31 compatible. The bus interface to the ZPSD6XX(V) is identical to that shown in Figure 13. Configurations 2 and 3 have the same bus connection as shown in Figure 19. There is only one read input ($\overline{PSEN}$) connected to the CNTL1 pin on the ZPSD6XX(V). The A16 connection to the PA0 pin allows for a larger address input to the ZPSD6XX(V). Configuration 4 is shown in Figure 20. The $\overline{RD}$ signal is connected to CNTL1 and the $\overline{PSEN}$ signal is connected to the CNTL2.

The 80C251 has two major operating modes: Page Mode and Non-Page Mode. In Non-Page Mode, the data is multiplexed with the lower address byte. The ALE is active in every bus cycle. In Page Mode, data D[7:0] is multiplexed with address A[15:8]. In a bus cycle where there is a Page hit, the ALE signal is not active and only addresses A[7:0] are changing. The ZPSD6XX(V) supports both modes. In Page Mode, the PSD bus timing is identical to Non-Page Mode except the address hold time and setup time with respect to ALE is not required. The ZPSD6XX(V) access time is measured from address A[7:0] valid to data in valid.

Upon power up the 80C251 accesses data at addresses FFF8h and FFF9h where the bus configuration bytes reside. After the configuration register is set, the 80C251 starts executing codes from location 0000h. The 7th EPROM block in the ZPSD6XX(V) has two chip selects, ES7A and ES7B. The second chip select, (ES7B) can be defined to occupy the configuration byte locations while ES7A is assigned to a different memory space.

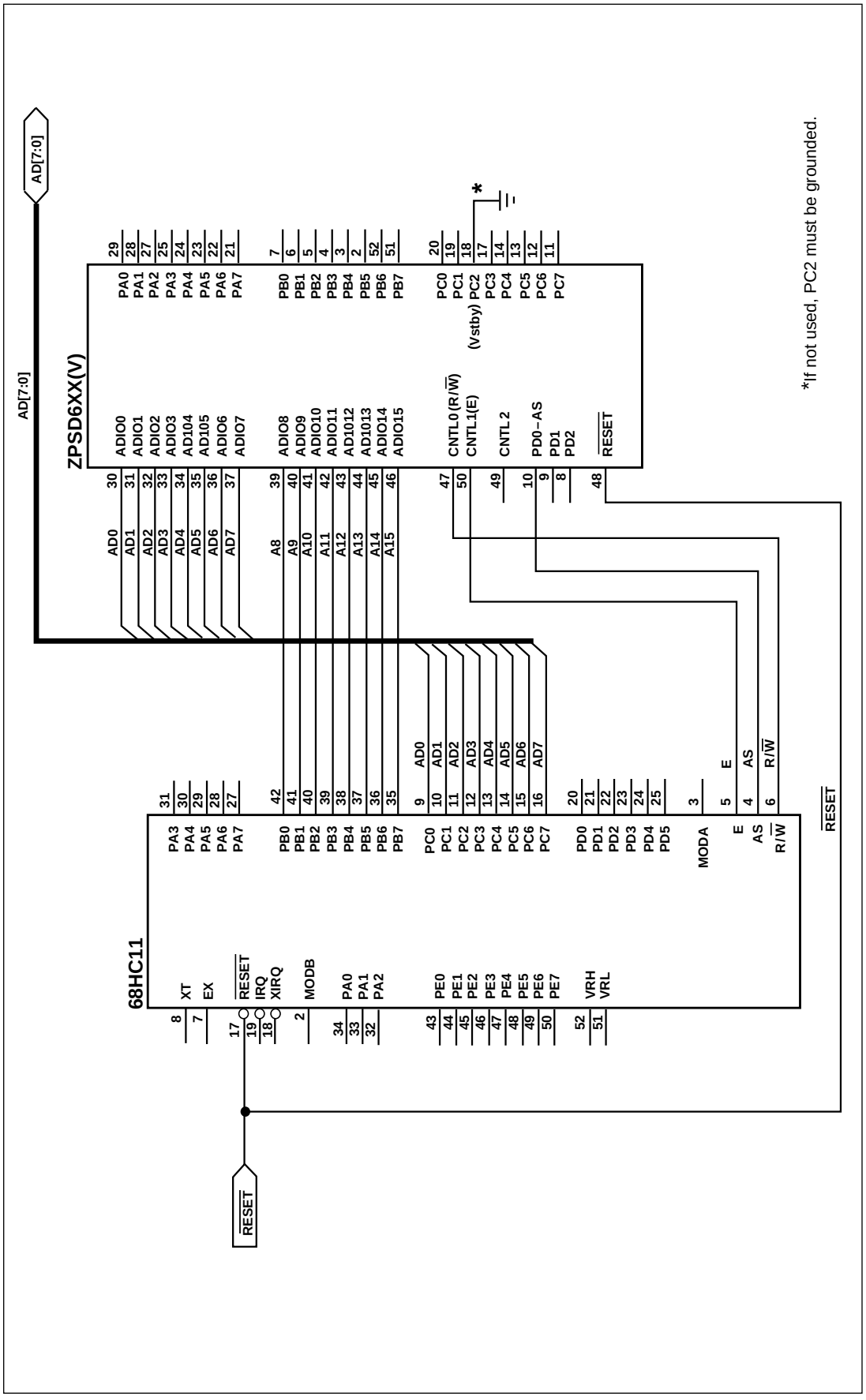
Bus Interface (cont.)

Figure 13. Interfacing the ZPSD6XX(V) with an 80C31 MCU



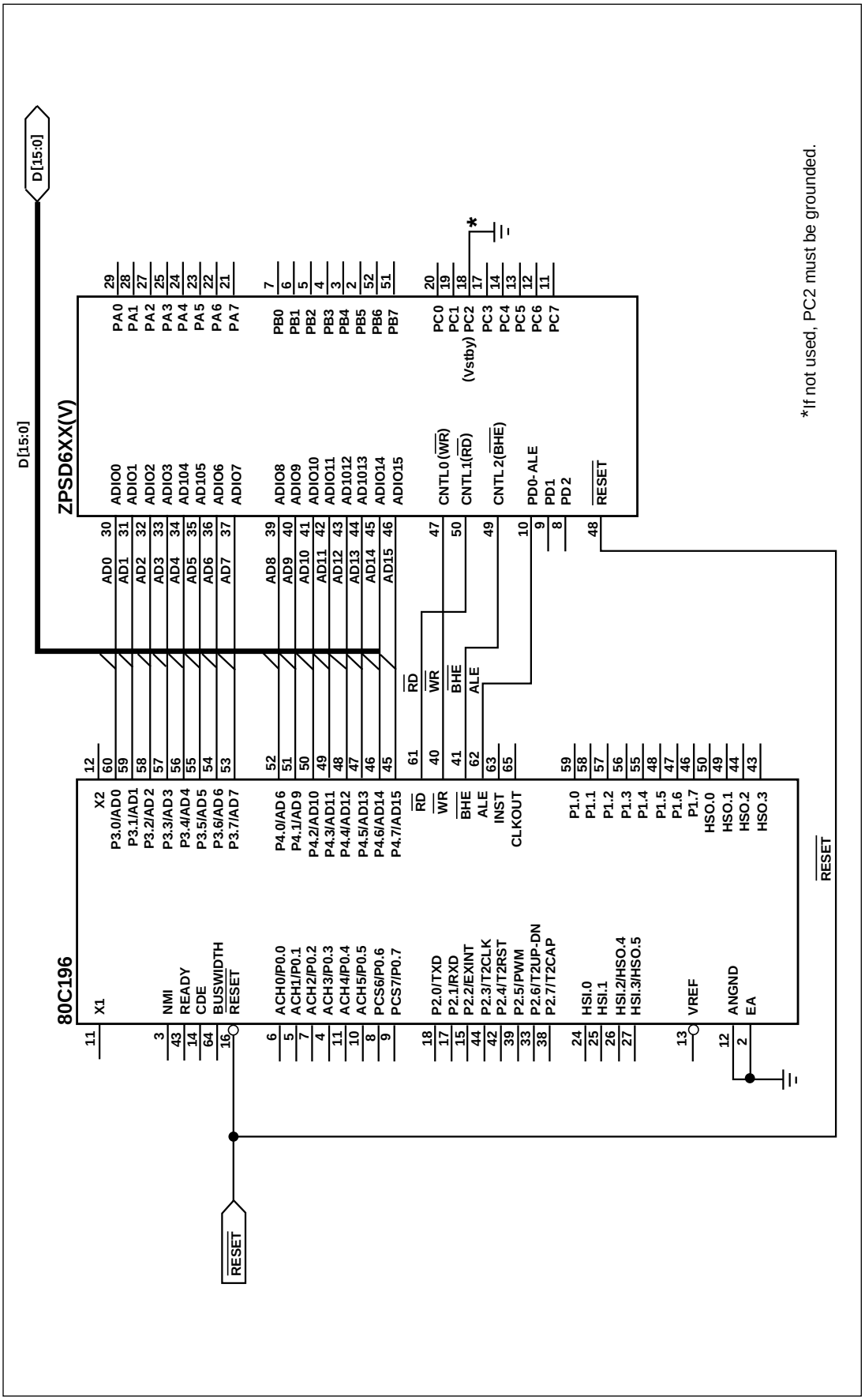
Bus Interface (cont.)

Figure 14. Interfacing the ZPSD6XX(V) with a 68HC11



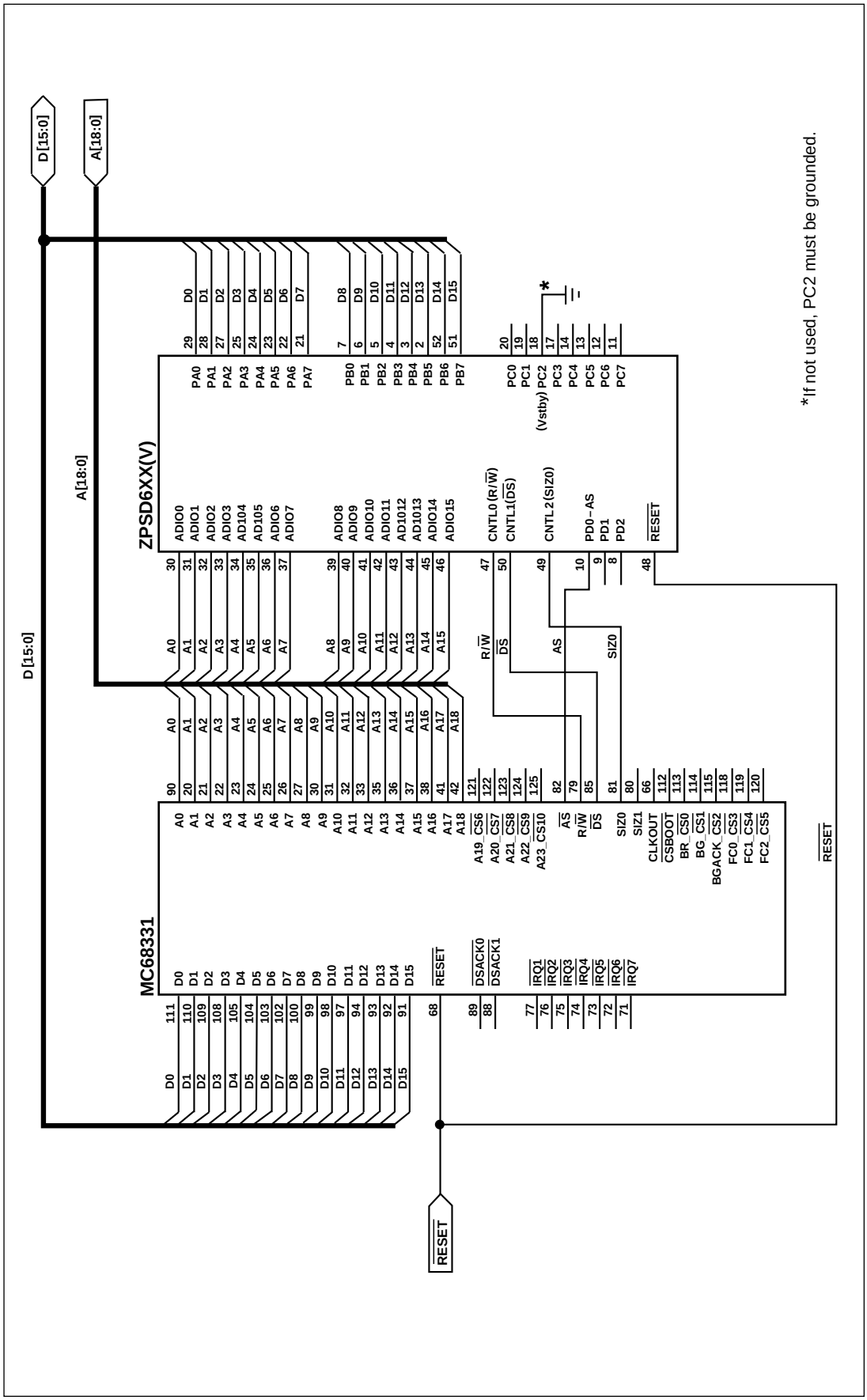
Bus Interface (cont.)

Figure 15. Interfacing the ZPSD6XX(V) to an 80C196



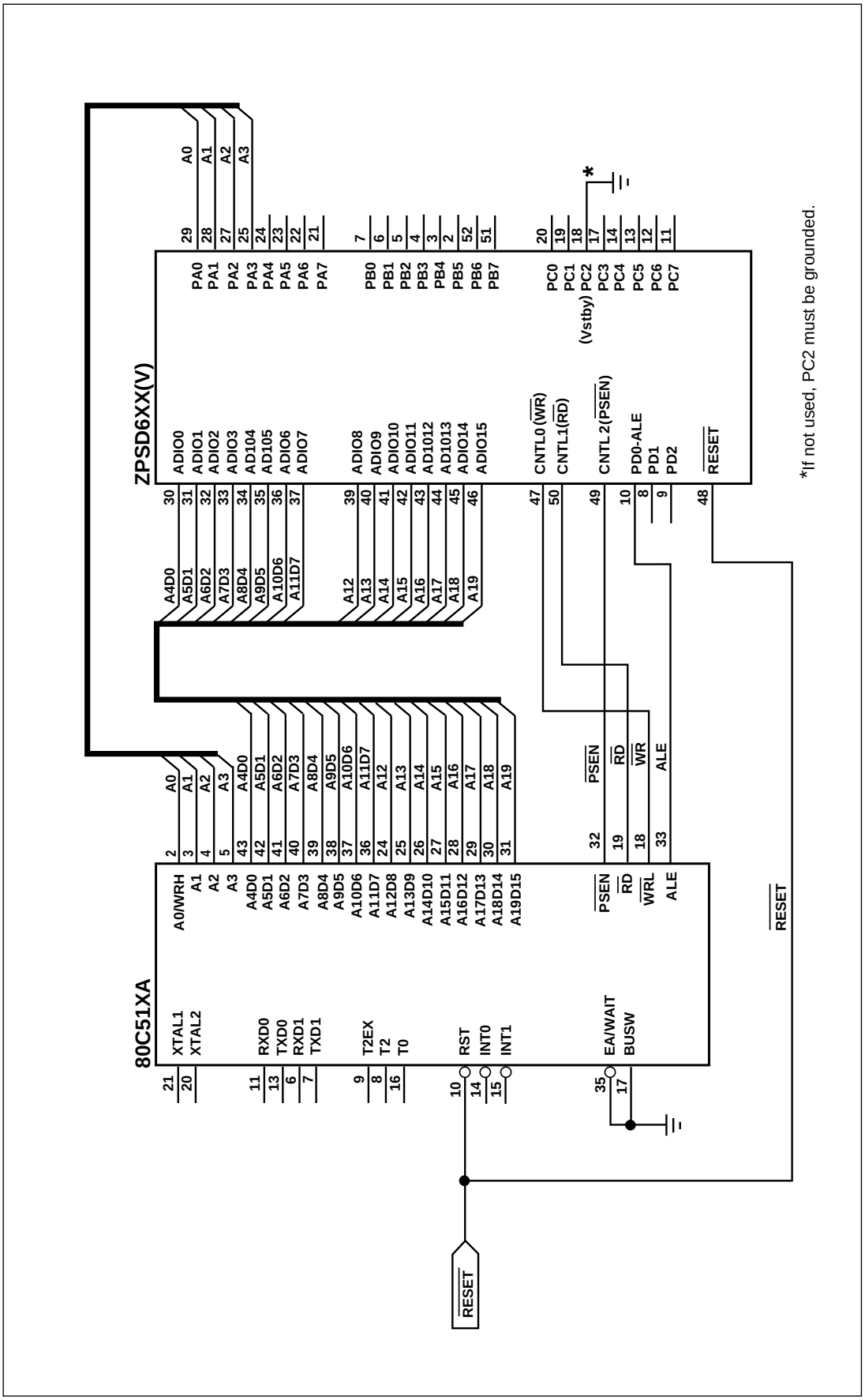
Bus Interface (cont.)

Figure 16. Interfacing the ZPSD6XX(V) to the MC68331



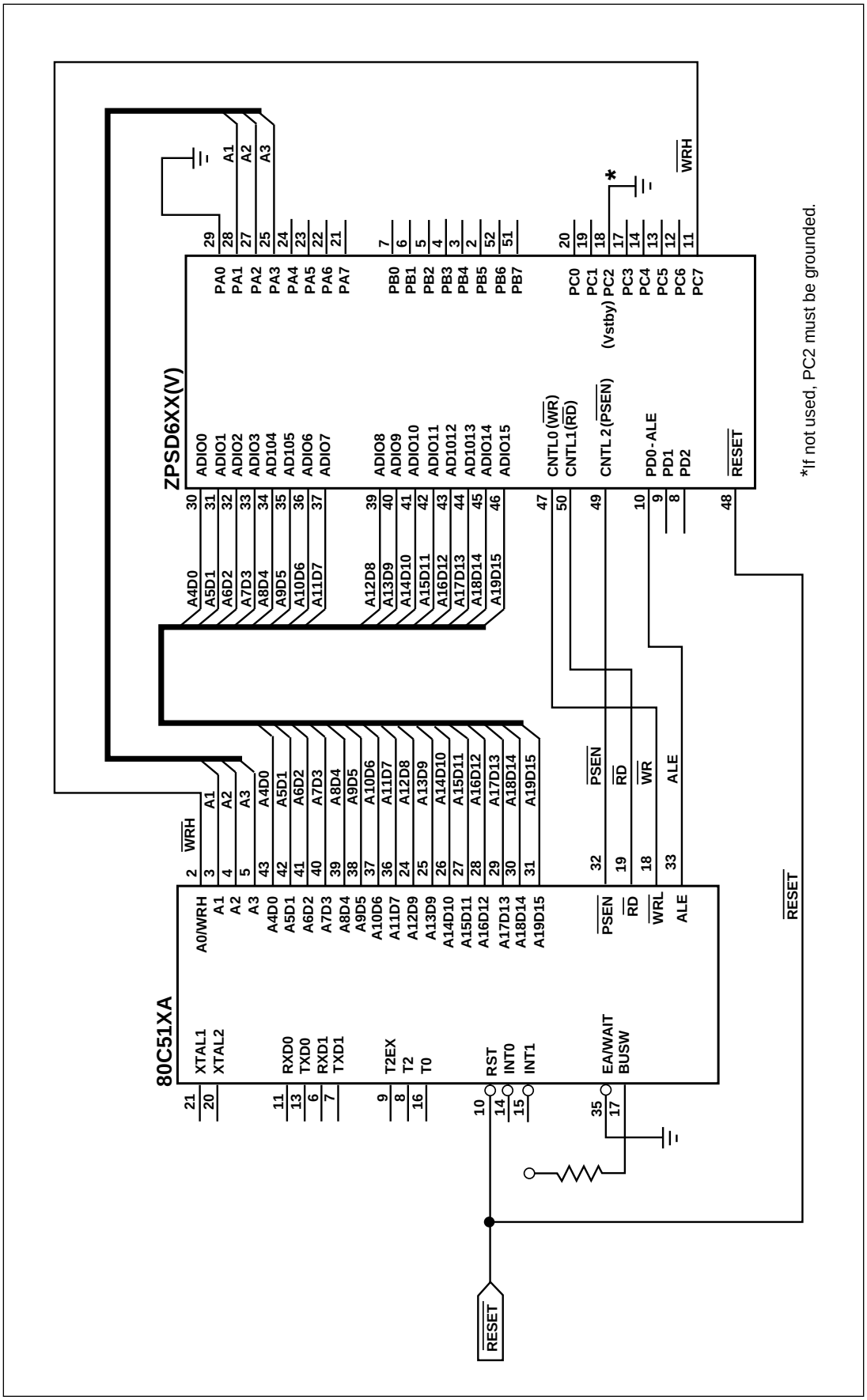
Bus Interface (cont.)

Figure 17. Interfacing the ZPSD6XX(V) to the 80C51XA, 8-Bit Data Bus



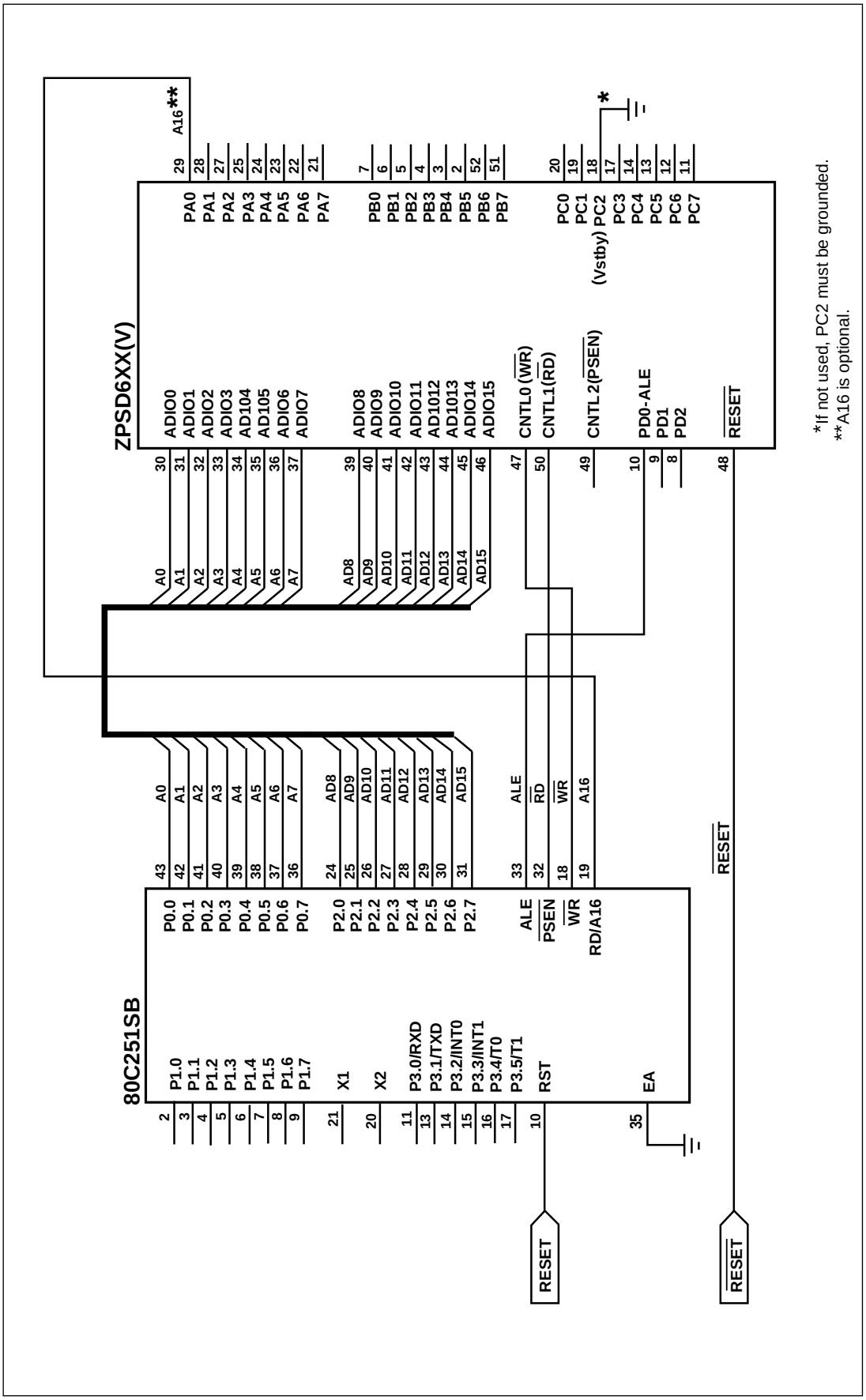
Bus Interface (cont.)

Figure 18. Interfacing the ZPSD6XX(V) to the 80C51XA, 16-Bit Data Bus



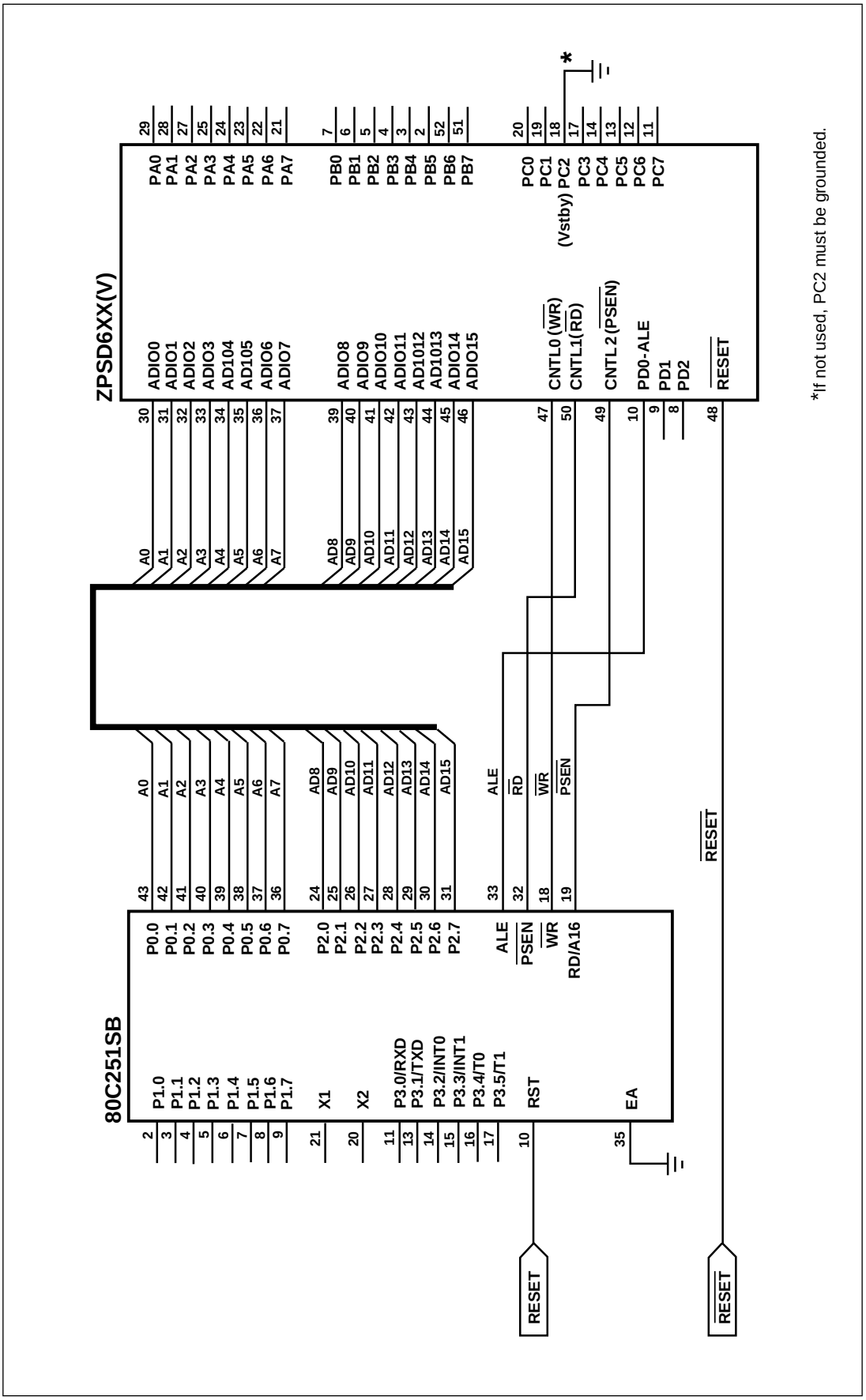
Bus Interface (cont.)

Figure 19. Interfacing the ZPSD6XX(V) to the 80C251, with One READ Input



Bus Interface (cont.)

Figure 20. Interfacing the ZPSD6XX(V) to the 80C251, with READ and $\overline{PSEN}$ Input



I/O Ports

There are four programmable I/O ports: Ports A, B are 8 bits, Port C is seven bits and Port D is three bits. The ports can be configured to function in different modes of operation.

Each port pin is individually configurable allowing a single port to perform multiple functions. The configuration is defined either using the PSDsoft tools or by the microcontroller writing to the on-chip registers.

I/O Port Architecture

The general architecture of the I/O Port is shown in Figure 21. Individual Port diagrams are shown in Figures 23, 24 and 25, and will be discussed in the section below. If the ZPSD6XX(V) is configured to a non-multiplexed bus mode, Port A and/or Port B are connected to the MCU data bus and are not available as general purpose I/O ports.

As shown in Figure 21, the port pins contain an output multiplexer whose selects are driven by the configuration defined in PSDabel and the Control Registers. Inputs to the multiplexer include the following:

- ❏ Output data from the Data Out Register in the MCU I/O output mode
- ❏ Latched address outputs
- ❏ GPLD Micro⇔Cell output or ECSPLD external chip select output

The above inputs are also connected to the Port Data Buffer (PDB) for feedback to the Internal Data Bus that can be read by the microcontroller. The PDB is a three-state buffer operating like a multiplexer that allows only one source to be read at a time. The PDB also has inputs from the Direction Register, Control Register and direct port pin input (Data In).

The Port pin's tri-state output driver enable is controlled by a two input OR gate whose inputs come from the GPLD AND array Enable product term (.oe) and the Direction Register. If the enable product term of the array output is not defined, then the Direction Register has sole control of the buffer. Refer to Tables 19 and 20 on how the direction of a port pin is configured.

Table 19. Port Pin Direction Control, Output Enable P.T. Not Defined

Direction Register Bit	Port Pin Mode
0	Input
1	Output

Table 20. Port Pin Direction Control, Output Enable P.T. Defined

Direction Register Bit	Output Enable P.T.*	Port Pin Mode
0	0	Input
0	1	Output
1	0	Output
1	1	Output

*Port D does not have an output enable P.T.

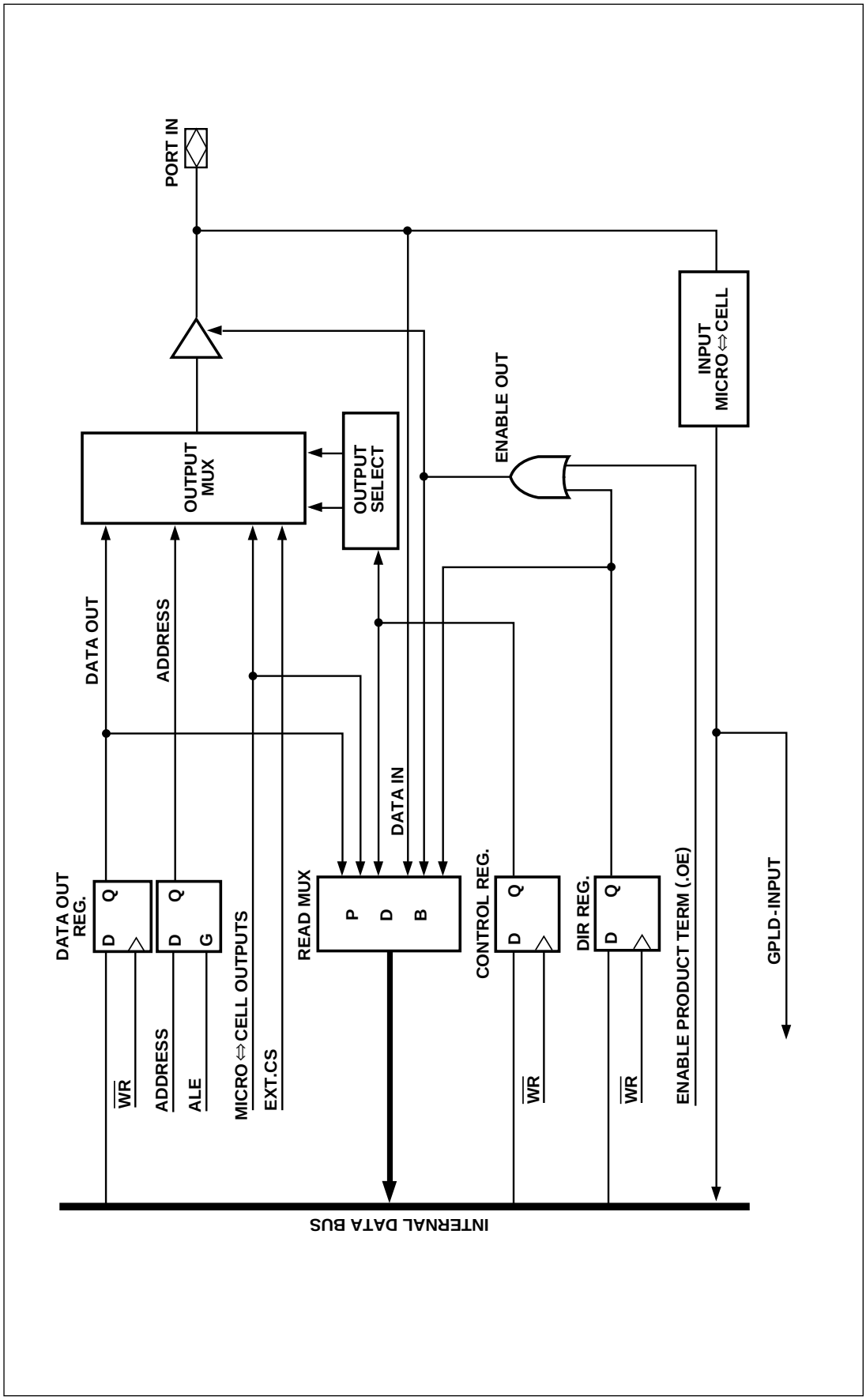
The register contents can be altered by the microcontroller. The PDB feedback path allows the microcontroller to check the contents of the registers.

The A, B and C Ports have embedded Input Micro⇔Cells which can be configured as a latch, a register or direct input to the GPLD. The latch and register are clocked by the address strobe or a product term from the GPLD AND array. The output from the Input Micro⇔Cell drives the ZPLD input bus and can be read by the microcontroller. Refer to the Input Micro⇔Cell description in the ZPLD section.

Port A has additional logic (not shown in Figure 21) that enables it to operate in Peripheral I/O mode when the PIO bit in the VM Register is set.

I/O Ports
(cont.)

Figure 21. General I/O Port Architecture



I/O Ports (cont.)

Port Operating Modes

The I/O Ports have several modes of operation as shown in Table 21. The mode may be selected using the PSDabel tool and programmed into the device using Non-Volatile Memory (NVM) that is active when power is applied and cannot be altered unless the device is reprogrammed. If a mode is not defined in PSDsoft, then other modes can be set by the microcontroller writing to the Port configuration registers. The PLD I/O, Data Port and Address Input modes are NVM configurations. The other modes are initiated by the microcontroller.

If the NVM modes are not selected, the port can be altered dynamically between MCU I/O or Address Out modes by writing to the Control Register. Each bit of the eight-bit Control Register may store a “1”, setting its respective bit in the port to MCU I/O, or to a “0”, setting it to Address Out. The Direction Register or the output enable product term determine if the pin is input or output.

Table 21 summarizes the operating modes of the I/O ports. Not all the functions are available to every port. Table 22 shows how and where the different modes are configured.

Table 21. Port Operating Modes

Port Mode	Port A	Port B	Port C	Port D
MCU I/O	Yes	Yes	Yes	Yes
PLD I/O				
McellAB Outputs	PA7–4	PB7–4	No	No
McellC Outputs	No	No	PC7–3, 1–0	No
ECSPLD Outputs	PA3–0	PB3–0	No	PD2–0
PLD Inputs	Yes	Yes	Yes	Yes
Address Out	Yes (A7–0)	Yes (A7–0, A15–8)	No	No
Address In	Yes	Yes	Yes	No
Data Port	Yes (D7–0)	Yes (D15–8)	No	No
Open Drain	Yes (PA7–4)	Yes (PB7–4)	Yes	No
Slew Rate	Yes (PA3–0)	Yes (PB3–0)	No	No
Peripheral I/O	Yes	No	No	No

I/O Ports (cont.)

Port Operating Modes (cont.)

Table 22. Port Operating Mode Settings

Mode	Defined In PSDabel	Defined In PSDconfiguration	Control Register Setting	Direction Register Setting	VM Register Setting
MCU I/O	Declare pins only	NA	0	1 = output, 0 = input (Note 1)	NA
PLD I/O	Logic equations	NA	NA*	(Note 1)	NA
Data Port (Port A,B)	NA	Specify bus type	NA	NA	NA
Address Out (Port A,B)	Declare pins only	NA	1	1 (Note 1)	NA
Address In (Port A,B,C)	Logic equation for Input Micro⇔Cells	NA	NA	NA	NA
Peripheral I/O (Port A)	Logic equations (PSEL0 & 1)	NA	NA	NA	PIO bit = 1

*NA – Not Applicable

NOTE 1: The direction of the Port A, B, C pins are controlled by the Direction Register ORed with the individual output enable product term (.oe) from the GPLD AND array.

PLD I/O Mode

The PLD I/O mode uses the port as an input to the GPLD Input Micro⇔Cell, and/or as an output from the GPLD, ECSPLD. The Port assignments are shown in Tables 9 and 10. The output can be tri-stated with a control signal defined by a product term (.oe) from the ZPLD, or, by setting a zero in the Direction Register. The Direction Register **must not** be set to “1” if the pin is defined as a ZPLD input pin. The PLD I/O mode is specified in PSDabel by declaring the port pins, then writing an equation assigning it to the port.

MCU I/O Mode

In the MCU I/O Mode the microcontroller uses the ZPSD6XX(V) ports to expand its own I/O ports. The ports on the ZPSD6XX(V) are mapped into the microcontroller address space. The addresses of the ports are listed in Table 27.

A port pin will be put into MCU I/O mode by writing a zero to the corresponding bit in the Control Register. The direction may be changed by writing to the Direction Register for the port where a “1” makes it an output and a “0” an input. The output enable product term also can change the direction of the pin (see Table 19 and 20). When the pin is configured as output, the content of the Data Out Register drives the pins. In input mode, the microcontroller reads the port input through the Data In buffer

Ports C and D do not have a Control Register and are in MCU I/O mode by default for pins that are not configured as PLD I/O.

Address Out Mode

For microcontrollers with a multiplexed address/data bus, the ports in Address Out mode drive latched addresses to external devices. Address [7:0] are always assigned to Port A. See Table 28 for the address output pin assignments on Ports A and B. The Direction Register and the Control Register must be set to a “1” for port pins using Address Out mode.

In non-multiplexed 8 bit bus mode, address[7:0] are available on Port B in Address Out Mode.

I/O Ports (cont.)

Port Operating Modes (cont.)

Address In Mode

For microcontrollers that have more than 16 address lines, the higher addresses can be connected to Port A, B, or C. The address input can be latched in the Input Micro⇔Cell by ALE. Any input that is included in the DPLD equations for the PSD EPROM and SRAM is considered as address input.

Data Port Mode

Port A and B can be used as data bus ports for a microcontroller with a non-multiplexed address/data bus. The Data Port is connected to the data bus of the microcontroller. The general I/O functions are disabled in Port A or B if the port is configured as Data Port.

Peripheral I/O Mode

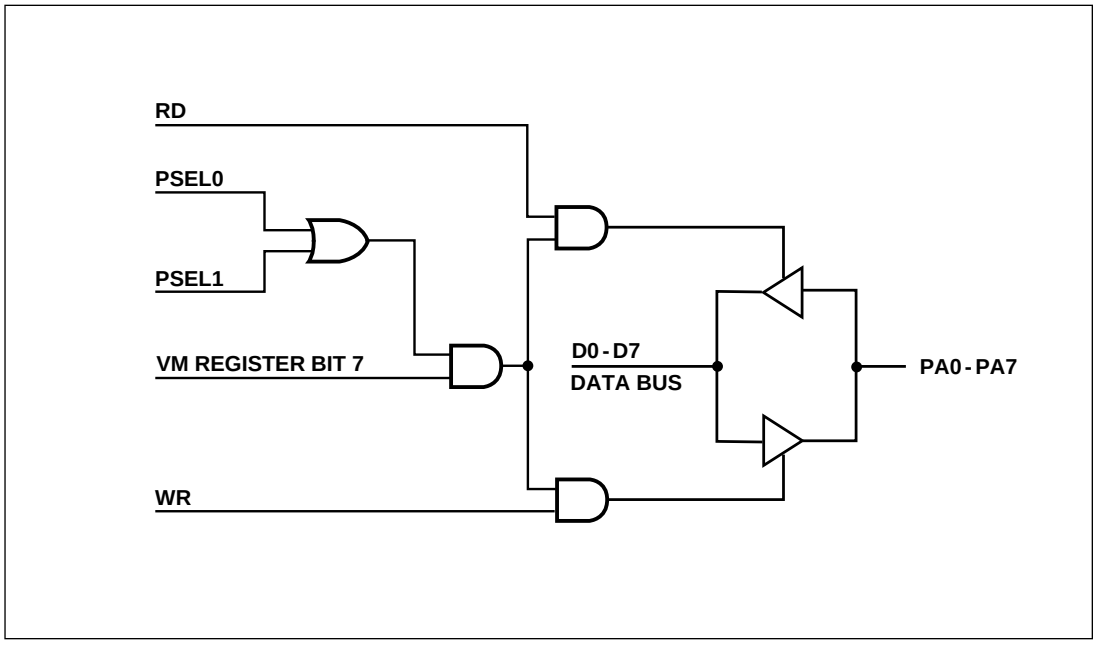
Only Port A supports the Peripheral I/O mode where all of Port A serves as a tri-state capable bi-directional data buffer of the microcontroller's data bus. Peripheral mode is enabled by setting Bit 7 of the VM Register to a "1". Figure 22 shows that when Peripheral mode is enabled and either PSEL0 and PSEL1 from the DPLD is active, Port A acts as a bi-directional buffer for the microcontroller D[7:0] data bus. The buffer is tri-stated when PSEL 0 or 1 is not active. The Peripheral I/O mode can be used to interface with external peripherals.

Open Drain/Slew Rate Mode

Port A (pins PA7-4), Port B (pins PB7-4) or Port C (except PC2) can be configured as an open drain instead of CMOS outputs. The Open Drain configuration is useful for sinking large currents to operate relays or LEDs, for example. The Open Drain mode is enabled by writing a "1" to the corresponding bit in the Drive Register.

Port A (PA3–0), Port B (PB3–0) and Port D can be configured as ECSPLD outputs that have a high slew rate. The high slew rate is enabled by writing a "1" to the corresponding bit in the Drive Register.

Figure 22. Port A Peripheral Mode



I/O Ports (cont.)

Port Registers

Each port has a set of registers used for configuration (PCR, Port Configuration Registers) and data transfers (PDR, Port Data Registers). The contents of the registers can be accessed by the microcontroller through normal read/write bus cycles at the addresses given in Tables 27 and 27A. The register addresses are comprised of the CSIOP output from the DPLD plus an address offset as listed in the tables.

The pins of a port are individually configurable and each bit in the register controls its respective pin. For example, Bit 0 in a register refers to Bit 0 in its port. The three Port Configuration Registers, shown in Table 23, are used for setting the port configuration. Each register is set to zero at power up.

Table 23. Port Configuration Registers

Register Name	Port	MCU Access
Control	A,B	Write/Read
Direction	A,B,C,D	Write/Read
Drive*	A,B,C,D	Write/Read

*Note: See Table 25 for Drive Register bit definition.

Control Register

A zero in the Control Register sets the Port pin to MCU I/O for Port A and B. A “1” sets the Port pin to Address Out mode. The default mode is MCU I/O.

Direction Register

Controls the direction of data flow in the I/O Ports. A “1” configures the port to be an output, and a “0” to an input. The I/O configuration can be read from the Direction Register. The default mode is input.

As shown in the Port Architecture diagram, the direction of data flow in Port A,B and C pins are also controlled by the output enable (.oe) product term from the GPLD AND array. If the .oe product term is not active, the Direction Register has sole control of the pin direction.

An example of a configuration for a port with the three least significant bits set to output and the remainder set to input is shown in Table 24. The Port D register has only the three least significant bits active.

Table 24. Port Direction Assignment Example

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	1	1	1

I/O Ports (cont.)

Port Registers (cont.)

Drive Register

The Drive Register configures the pin driver as Open Drain, or in the case of ECSPLD outputs, sets the pin to operate in high slew rate. An external pull-up resistor is not required when the pin is in the slew rate mode.

For Ports A and B the register sets different functions for the lower and higher nibbles. The four upper bits set the corresponding bits as CMOS (“0”) or Open Drain (“1”) driver. The four lower bits are used for slew rate control. The slew rate is a measurement of the rise and fall times of the output. A higher slew rate means a faster output response while a lower slew rate is a slower, lower slope, response. The pin operates in high slew rate when the corresponding bit in the Drive Register is set to “1”.

Table 25 shows the Drive Registers of Port A, B, C and D and which pin has the Open Drain or Slew Rate configuration.

Table 25. Drive Register Pin Assignment

Drive Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port A	Open Drain	Open Drain	Open Drain	Open Drain	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port B	Open Drain	Open Drain	Open Drain	Open Drain	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port C	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	NA	Open Drain	Open Drain
Port D	NA	NA	NA	NA	NA	Slew Rate	Slew Rate	Slew Rate

NOTE: NA = Not Applicable, bit should set to “0”.

I/O Ports (cont.)

Port Data Registers

The Port Data Registers, shown in Table 26, are used by the microcontroller to write or read data to or from the ports. Table 26 shows the register name, the ports having each register type and microcontroller access for each register. The registers are described below.

Table 26. Port Data Registers

Register Name	Port	MCU Access
Data In	A,B,C,D	Read – the input on pin
Data Out	A,B,C,D	Write/Read
Output Micro⇔Cell	A,B,C	Read – outputs of Micro⇔Cells Write – loading Micro⇔Cells Flip-Flop
Input Micro⇔Cell	A,B,C	Read – outputs of the Input Micro⇔Cells
Enable Out	A,B,C	Read – the output enable control of the port driver

Data In

Port pins are connected directly to the Data In buffer. In MCU I/O input mode, the pin input is read through the Data In buffer.

Data Out Register

Stores output data written by the MCU in the MCU I/O output mode. The contents of the Register are driven out to the pins if the Direction Register or the .oe product term is set to “1”. The contents of the register can also be read back by the microcontroller.

Output Micro⇔Cell

The GPLD Output Micro⇔Cells occupy a location in the microcontroller’s address space. The microcontroller can read the output of the Micro⇔Cells. Writing to the Micro⇔Cell loads data to the Micro⇔Cell Flip-Flops. Refer to the ZPLD section for more detail.

Input Micro⇔Cell

The Input Micro⇔Cells can be used to latch or store external inputs. The outputs of the Input Micro⇔Cells are routed to the ZPLD input bus and also can be read by the microcontroller. Refer to the ZPLD section for detailed description.

Enable Out

The Enable Out buffer allows the microcontroller to read the outputs of the “OR” gate that is the enable input to the port output driver. A “1” indicates the driver is in output mode, a “0” indicates the driver is in tri-state and the pin is in input mode.

I/O Ports (cont.)

Port Data Registers (cont.)

Register I/O Address Offset

The base address of the Registers is defined in the CSIOP equation that occupies 256 bytes of address space and is defined by the user in PSDsoft. The lower address byte A[7:0], or address offset, selects the register. Table 27 shows the address offset for all MCUs except those Motorola microcontrollers with a 16-bit data bus. Table 27A shows the address offset for Motorola MCUs in 16-bit mode.

For example, when the CSIOP is defined to occupy the address range of 1000h to 10FFh in PSDabel, the address of the Port A Control Register is then 1002h.

Table 27. I/O Register Address Offset (relative to CSIOP)

Register Name	Port A	Port B	Port C	Port D
Data In	00	01	10	11
Control	02	03		
Data Out	04	05	12	13
Direction	06	07	14	15
Drive	08	09	16	17
Input Micro⇔Cell	0A	0B	18	
Enable Out	0C	0D	1A	
Output Micro⇔Cell	20	20	21	

Table 27A. Register Address Offset for 16-Bit Motorola Microcontrollers in 16-Bit Mode (relative to CSIOP)

Register Name	Port A	Port B	Port C	Port D
Data In	01	00	11	10
Control	03	02		
Data Out	05	04	13	12
Direction	07	06	15	14
Drive	09	08	17	16
Input Micro⇔Cell	0B	0A	19	
Enable Out	0D	0C	1B	
Output Micro⇔Cell	21	21	20	

I/O Ports (cont.)

Port A and B – Functionality and Structure

Port A and B have similar functionality and structure as shown in Figure 23. The two ports can be configured to perform one or more of the following functions:

- ❏ MCU I/O Mode
- ❏ GPLD Output – Micro⇔Cells McellAB[7:4] can be connected to Port A PA[7:4} or Port B PB[7:4].
- ❏ ECSPLD Output – External chip select output can be connected to either Port A PA[3:0] or Port PB[3:0].
- ❏ Latched Address output – Provide latched address output per Table 28.
- ❏ Address In – Additional high address inputs using the Input Micro⇔Cells.
- ❏ Open Drain/Slew Rate – pins PA[3:0] and PB[3:0] can be configured to Open Drain Mode pins PA[7:4] and PB[7:4] can be configured to fast slew rate
- ❏ Data Port – Port A to D[7:0} for 8 bit non-multiplexed bus Port B to D[15:8] for 16-bit non-multiplexed bus
- ❏ Peripheral Mode – Port A only

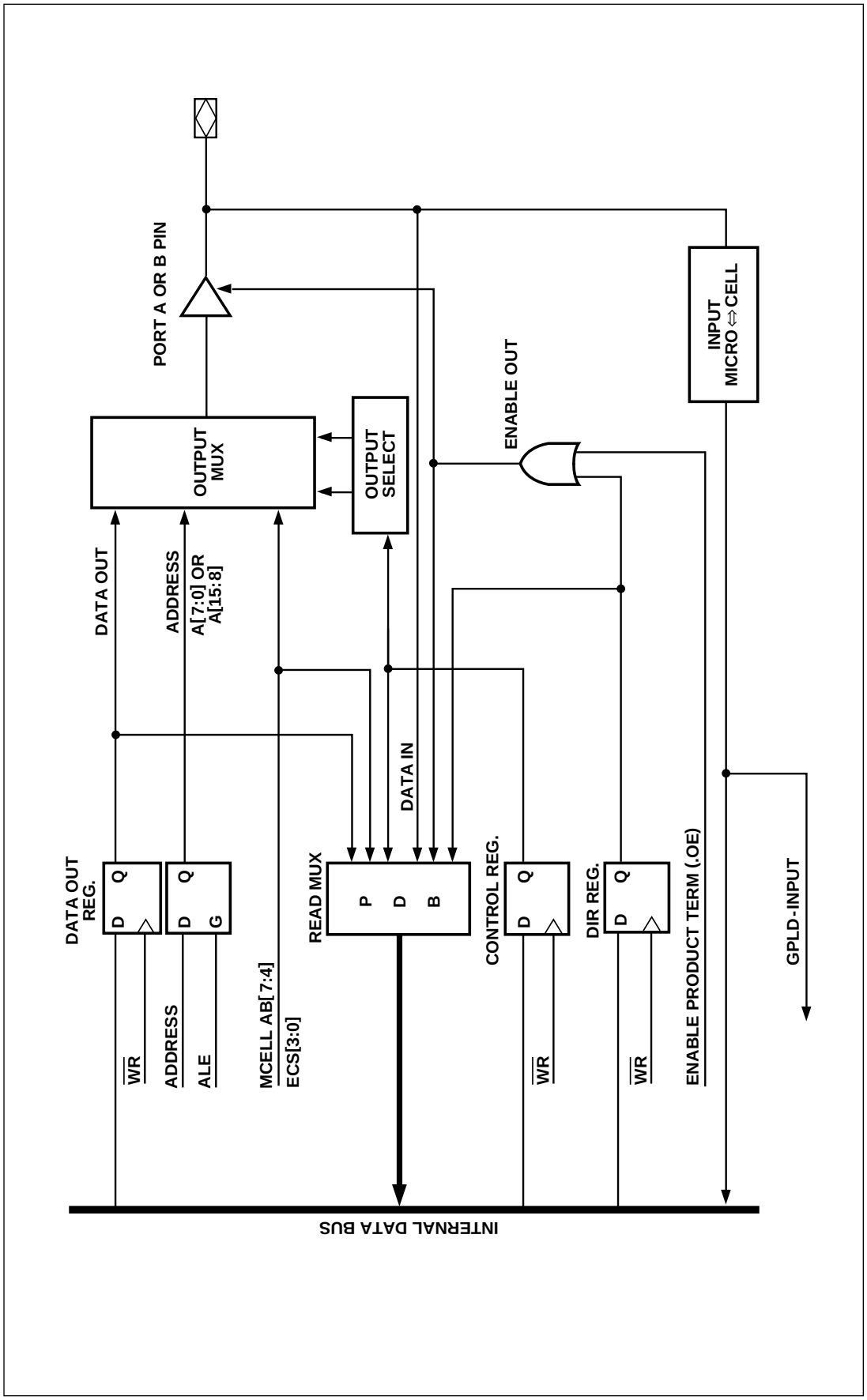
Table 28. I/O Port Latched Address Output Assignments

Microcontroller	Port A (3:0)	Port A (7:4)	Port B (3:0)	Port B (7:4)
8051XA (8-Bit)	N/A*	Address (7:4)	Address (11:8)	N/A
80C251 (Page Mode)	N/A	N/A	Address (11:8)	Address (15:12)
All Other 8-Bit Multiplexed	Address (3:0)	Address (7:4)	Address (3:0)	Address (7:4)
8051XA (16-Bit)	N/A	Address (7:4)	Address (11:8)	Address (15:12)
All Other 16-Bit Multiplexed	Address (3:0)	Address (7:4)	Address (11:8)	Address (15:12)
8-Bit Non-Multiplexed Bus	N/A	N/A	Address (3:0)	Address (7:4)

N/A = Not Applicable.

I/O Ports
(cont.)

Figure 23. Port A and B Structure



I/O Ports (cont.)

Port C – Functionality and Structure

Port C does not support Address Out mode and the Control Register is not required. Port C can be configured to perform one or more of the following functions:

- ❏ MCU I/O Mode
- ❏ GPLD Output – McellC outputs can be connected to Port C pins
- ❏ GPLD Input – Via the eight Input Micro⇔Cells
- ❏ Address In – Additional high address inputs using the Input Micro⇔Cells.
- ❏ Open Drain – Port C pins can be configured in Open Drain Mode

Port C pin PC2 is dedicated as the Vstby pin for SRAM battery backup and can not be used for other functions. Pin PC7 may be configured as the $\overline{WRH}$ input in certain microcontroller interface designs.

Port D – Functionality and Structure

Port D has only three I/O pins, does not support Address Out mode, and no Control Register is required. Port D can be configured to perform one or more of the following functions:

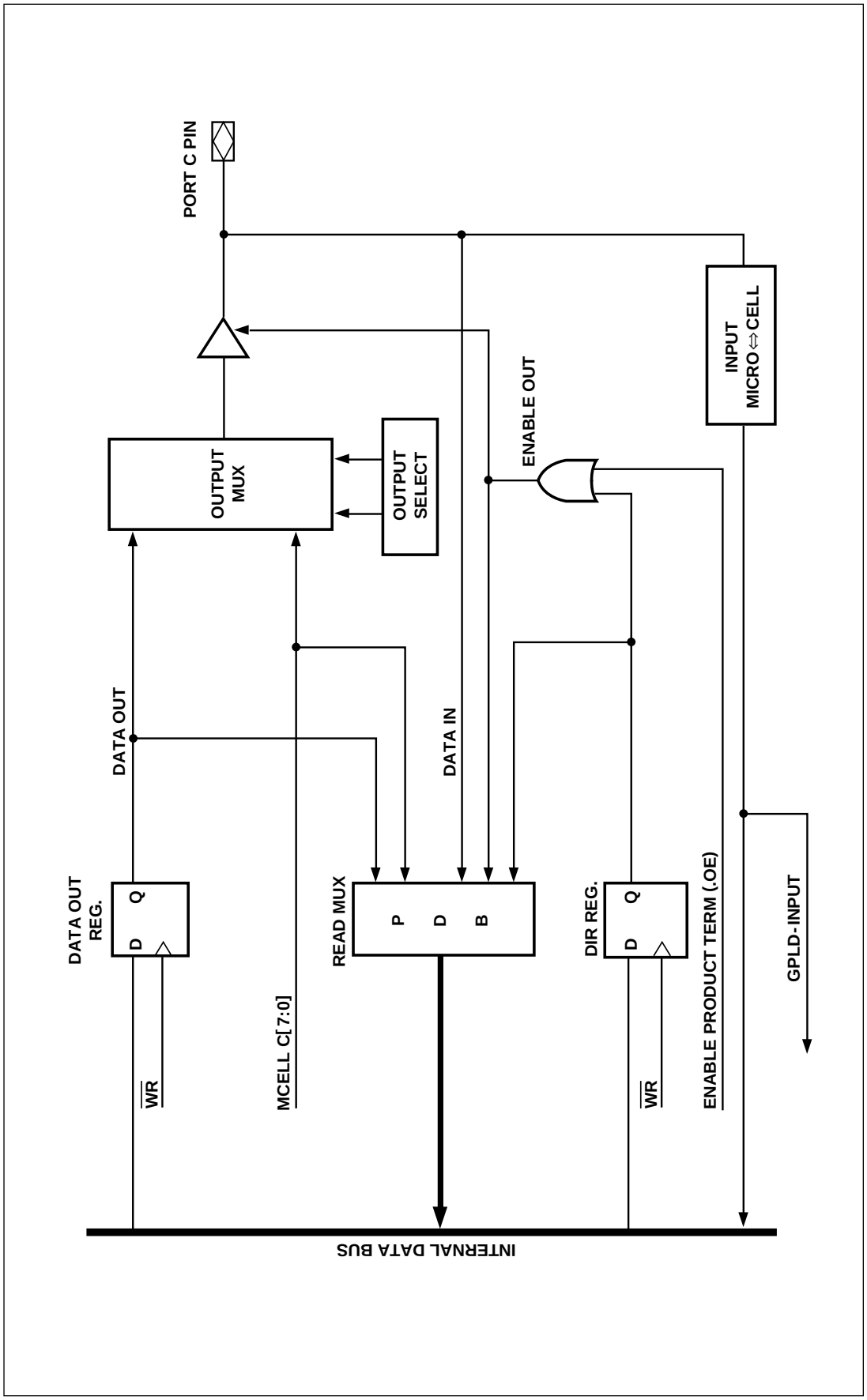
- ❏ MCU I/O Mode
- ❏ ECSPLD Output – External chip select output
- ❏ ZPLD Input – direct input to ZPLD, no Input Micro⇔Cells
- ❏ Slew rate – pins can be set up for fast slew rate

Port D pins can be configured in PSDsoft as input pins for other dedicated functions:

- ❏ PD0 – ALE, as address strobe input
- ❏ PD1 – CLKIN, as clock input to the Micro⇔Cells Flip-Flops and APD counter
- ❏ PD2 – CSI, as active low chip select input. A high input will disable the PSD EPROM/SRAM.

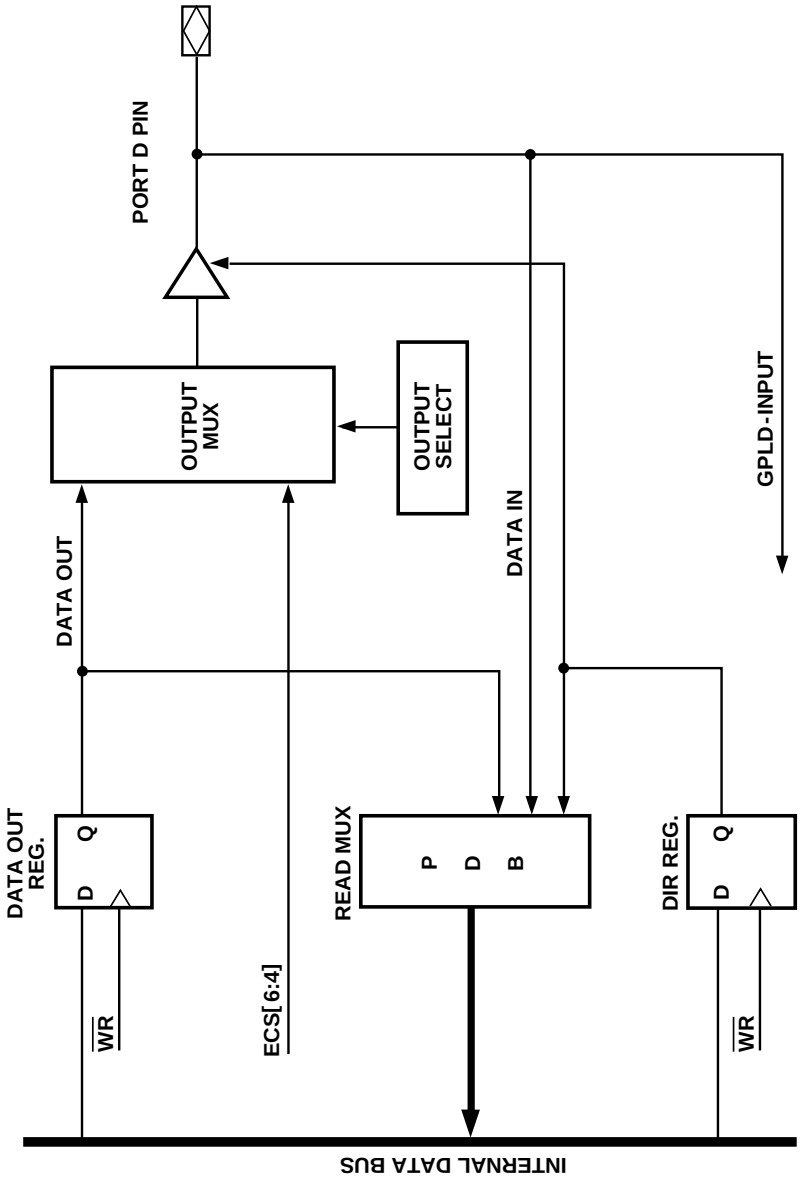
I/O Ports
(cont.)

Figure 24. Port C Structure



I/O Ports
(cont.)

Figure 25. Port D Structure



Memory Blocks

The ZPSD6XX(V) has internal EPROM and SRAM memory blocks. The memory select signals come from the DPLD and are user-defined in the PSDsoft Software.

EPROM

The ZPSD6XX(V) provides three EPROM densities: 256K bit, 512K bit or 1M bit. The EPROM is divided into eight blocks. The EPROM can be configured as 32K x 8, 64K x 8 or 128K x 8 for eight-bit data busses and 16K x 16, 32K x 16 or 64K x 16 for sixteen-bit data buses.

Each block has its own EPROM select. Blocks zero to six have one select (ES0-ES6) and block 7 has two selects, ES7A and ES7B, either of which enables Block 7. The dual selects allow Block 7 to reside in two separate memory spaces.

A typical application would be to store an MCU reset vector residing in the memory space and accessed by ES7B. The rest of the Block 7 memory space would be accessed by ES7A. The same technique can also be used to store the configuration bytes of the Intel 80251 microcontroller which reside at the high end of the memory space.

SRAM

The SRAM has 4K bits of memory that can be configured as 512 x 8 or 256 x 16. The SRAM is enabled from the RS0 output of the DPLD. The SRAM has a battery back-up mode which is automatically invoked when the supply voltage drops under the standby voltage. SRAM write protection is provided in back-up mode.

Memory Select Map

The EPROM and SRAM select are outputs from the DPLD whose equations are defined using PSDabel. The following rules apply to the memory space definitions:

1. EPROM block select space should not be larger than the physical block size
2. EPROM block select space must not overlap
3. SRAM, I/O and Peripheral I/O spaces cannot overlap
4. SRAM, I/O and Peripheral I/O spaces can overlap EPROM with priority given to the SRAM or I/O. This allows the SRAM or I/O to utilize the space that is not used by the EPROM.

Memory Blocks (cont.)

Memory Select for 8031 Microcontrollers

The 8031 family of microcontrollers, including 80C251 and 80C51XA, has a separate address space for code memory (enabled by PSEN) and data memory (enabled by RD). The ZPSD6XX(V) allows the EPROM and SRAM to reside in the program space, data space or both. Three different configurations are possible:

❑ ***Separate Space Mode***

Code memory space is separated from data memory space. The PSEN signal is used to access the program code from the EPROM, and the RD signal is used to access data from the SRAM and I/O Ports. This is the default configuration.

❑ ***Combined Space Mode***

The program and data memory spaces are combined into one 64KB block space that allows the EPROM or SRAM to be accessed by either PSEN or RD. The EPROM and SRAM blocks address space must not overlap. This mode is enabled by the microcontroller by setting the bits in the VM Register as shown in Table 29. If Bit 0 is “1”, either PSEN or RD can access the SRAM. If Bit 1 is a “1”, either RD or PSEN can access the EPROM. Figure 27 shows the memory select logic for Combined Space Mode.

❑ ***Mixed Mode***

Allows individual EPROM blocks to be configured in either Data Space or Program Space. EPROM block chip selects must be qualified with the 8031 RD input in the ES0−ES7 equations. An active low RD will select EPROM blocks in data space and disable the blocks that are in program space. For EPROM blocks that reside in data space, the access time is calculated from RD valid to data valid. This mode is set automatically by PSDsoft whenever the RD signal is included in the EPROM chip select equations.

Table 29. VM Register

Bit 7 PIO_EN	Bit 6*	Bit 5*	Bit 4*	Bit 3*	Bit 2*	Bit 1 RD_EN	Bit 0 PSEN_EN
0 = disable PIO mode						0 = RD access SRAM, I/O	0 = PSEN access EPROM only
1 = enable PIO mode						1 = RD access EPROM, SRAM, I/O	1 = PSEN access EPROM, SRAM, I/O

*Bit 6-2 are not used, set to “0”.

Memory Blocks (cont.)

Figure 26. 8031 Memory Modes – Separate Space Mode

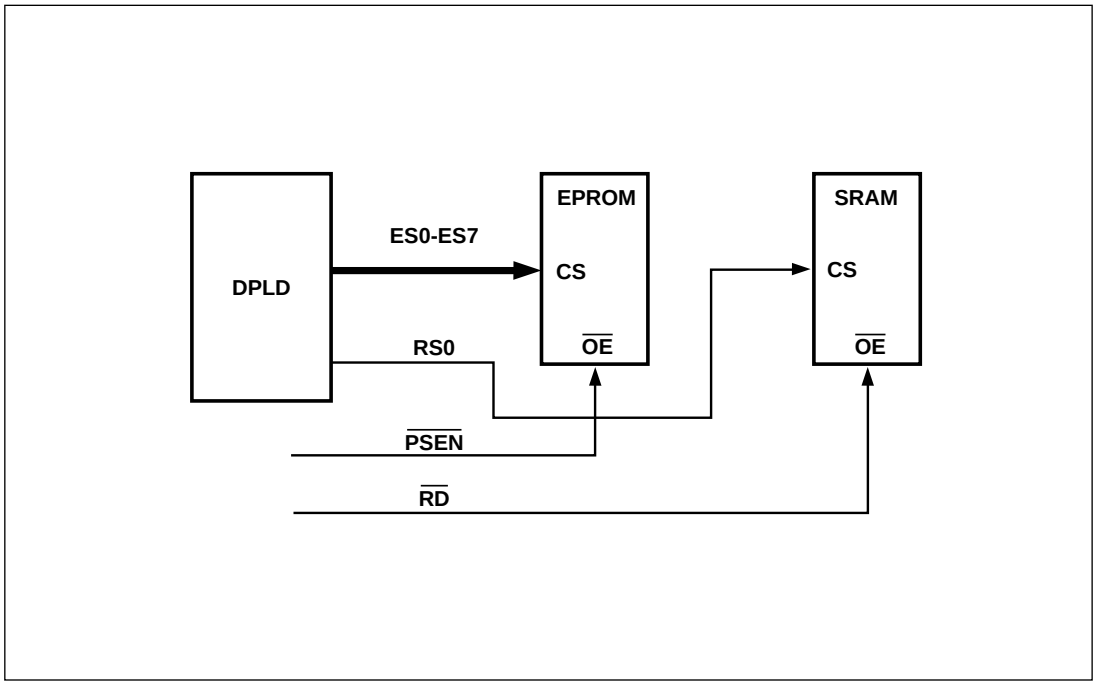
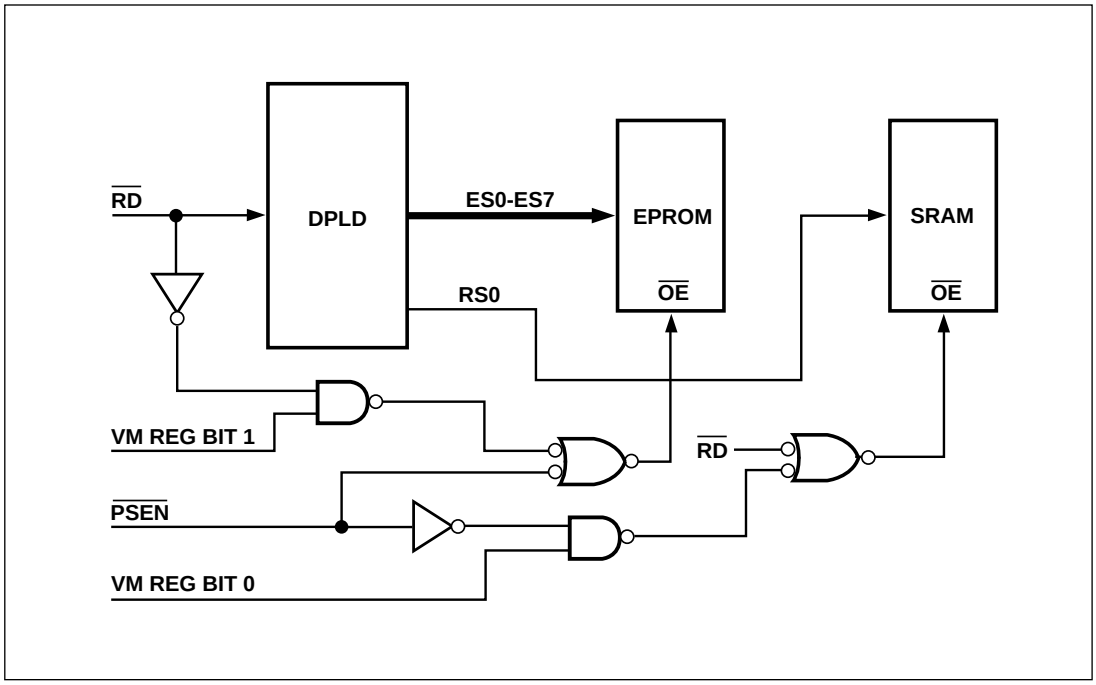


Figure 27. 80C31 Memory Mode – Combined Space Mode



Power Management Unit

The ZPSD6XX(V) offers a number of configurable power saving options which include the Automatic Power Down (APD) Logic and the Power Management Mode Registers (PMMR0 and PMMR1). The APD Logic allows the ZPSD6XX(V) to enter into either Power Down or Sleep Mode automatically, while the PMMRs can be configured at run time by the microcontroller to selectively reduce the power consumption of the PSD functional blocks.

The APD Logic and Power Down Mode

The Automatic Power Down (APD) logic puts the ZPSD6XX(V) into power savings mode by monitoring the activity of the address strobe (ALE/AS). If the APD unit is enabled, the four-bit APD counter starts counting whenever the address strobe is inactive. If the strobe remains inactive for fifteen CLKIN clock periods, the power down (PDN) signal will become active and the ZPSD6XX(V) enter into either Power Down or Sleep Mode. Immediately after ALE starts pulsing the ZPSD6XX(V) will return to normal operation. The APD counter clock source comes from the CLKIN pin which is pin PD1 on Port D. In order to guarantee that the APD counter will not overflow when enabled, there should be less than 15 clocks between two successive ALE pulses.

Usually, microcontrollers entering power down mode will freeze their ALE at logic high or low level. By programming bit 0 of PMMR0, the APD knows when the MCU is in power down mode. If the APD detects the ALE level is in the power down state for 15 CLKIN periods, then the ZPSD6XX(V) will enter a power down mode. To enable the APD operation, the APD bit in the PMMR0 should be set to “1”.

When the address strobe starts pulsing again, or the CSI input switches from high to low, the ZPSD6XX(V) will return to normal activity.

When the PDN signal is set to “1” (active state) in Power Down (or Sleep Mode), the ZPSD6XX(V) MCU bus interface is disabled and all MCU inputs (address, data and control signals) are blocked from entering the device. If the clock input to the ZPLD is not needed in Power Down mode, it should be blocked to save power by setting Bit 4 and 5 in the PMMR0 to “1”.

The ZPLD Power Management

The ZPLD implements a Zero Power Mode, which provides considerable power savings for low to medium frequency operations. To enable this feature, the ZPLD Turbo bit in the Power Management Mode Register 0 (PMMR0) has to be turned off.

If none of the inputs to the ZPLD are switching for a time period of 70 ns, the ZPLD puts itself into Zero Power Mode and the current consumption is minimal. The ZPLD will resume normal operation as soon as one or more of the inputs change state.

Two other features of the ZPLD provide additional power savings:

1. **Clock Disable:**
   Users can disable the clock input to the ZPLD and/or macrocells, thereby reducing AC power consumption.

2. **Product Term Disable:**
   Unused product terms in the ZPLD are disabled by the PSDsoft Software automatically for further power savings.

Power Management Unit (cont.)

Sleep Mode

The Sleep Mode is activated if the Sleep mode bit, the APD bit and the ALE Polarity bit in the PMMRs are set, and the APD Counter has overflowed after 15 CLKIN clocks (see Figure 28). In Sleep Mode the ZPSD6XX(V) consumes less power than the Power Down Mode, with typical I_{CC} reduced to 10µA.

In this mode, the ZPLD still monitors the inputs and responds to them. As soon as the ALE starts pulsing or the CSI input switches from high to low, the ZPSD6XX(V) exits the Sleep Mode. The ZPSD6XX(V) access time from Sleep Mode is specified by tLVDV1. The ZPLD response time to an input transition is specified by tLVDV2.

Table 30. Power Down Effect on Ports

Port Function	Pin Level
MCU I/O	No Change
ZPLD Out	No Change
Address Out	Undefined
Data Port	Three-State
Peripheral I/O	Three-State

Table 31. Summary of ZPSD6XX(V) Timing and Standby Current During Power Down and Sleep Mode

Mode	PLD Propagation Delay	PLD Recovery Time to Normal Operation	Access Time	Access Recovery Time to Normal Access	Typical Standby Current
Power Down	Normal tpd (Note 1)	0	No Access	tLVDV	25µA (Note 4)
Sleep	tLVDV2 (Note 2)	tLVDV3 (Note 3)	No Access	tLVDV1	10µA (Note 5)

NOTES:
1. Power Down does not affect the operation of the ZPLD.The ZPLD operation in this mode is based only on the ZPLD_Turbo Bit.
2. In Sleep Mode any input to the ZPLD will have a propagation delay of tLVDV2.
3. PLD recovery time to normal operation after existing Sleep Mode. An input to the ZPLD during the transition will have a propagation delay of tLVDV3.
4. Typical current consumption assuming CLKIN is disabled and the ZPLD Turbo bit is off.
5. Typical current consumption assuming CLKIN is disabled.

Power Management Unit (cont.)

Figure 28. APD Logic Block

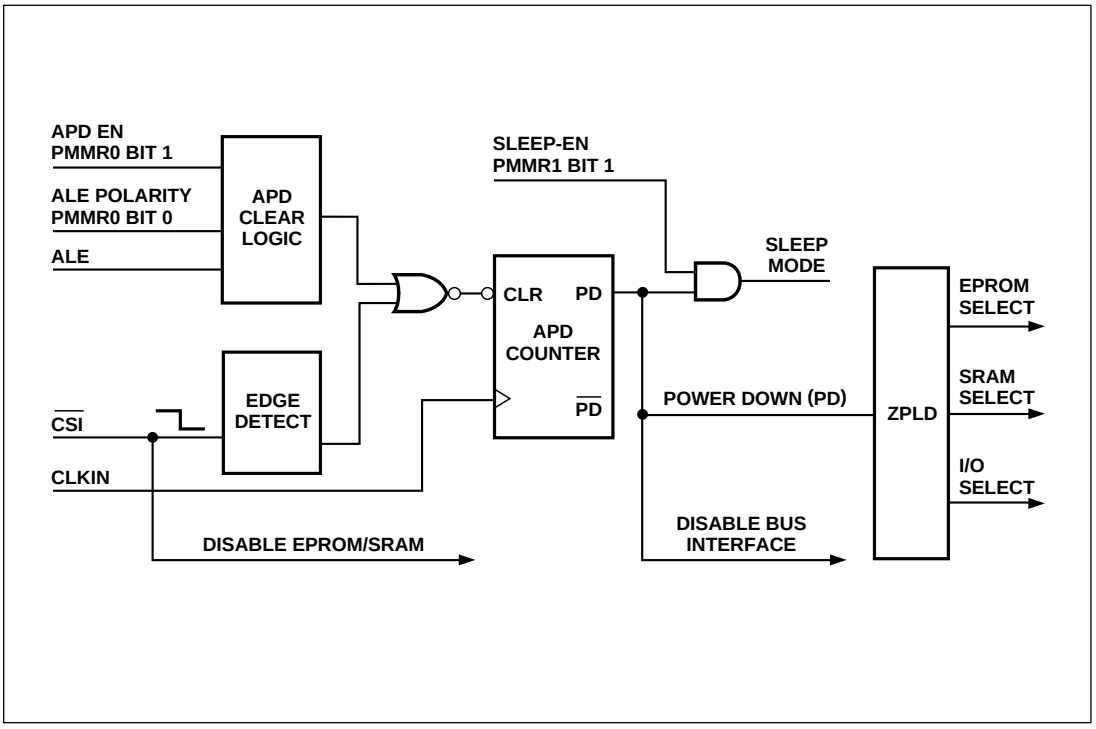
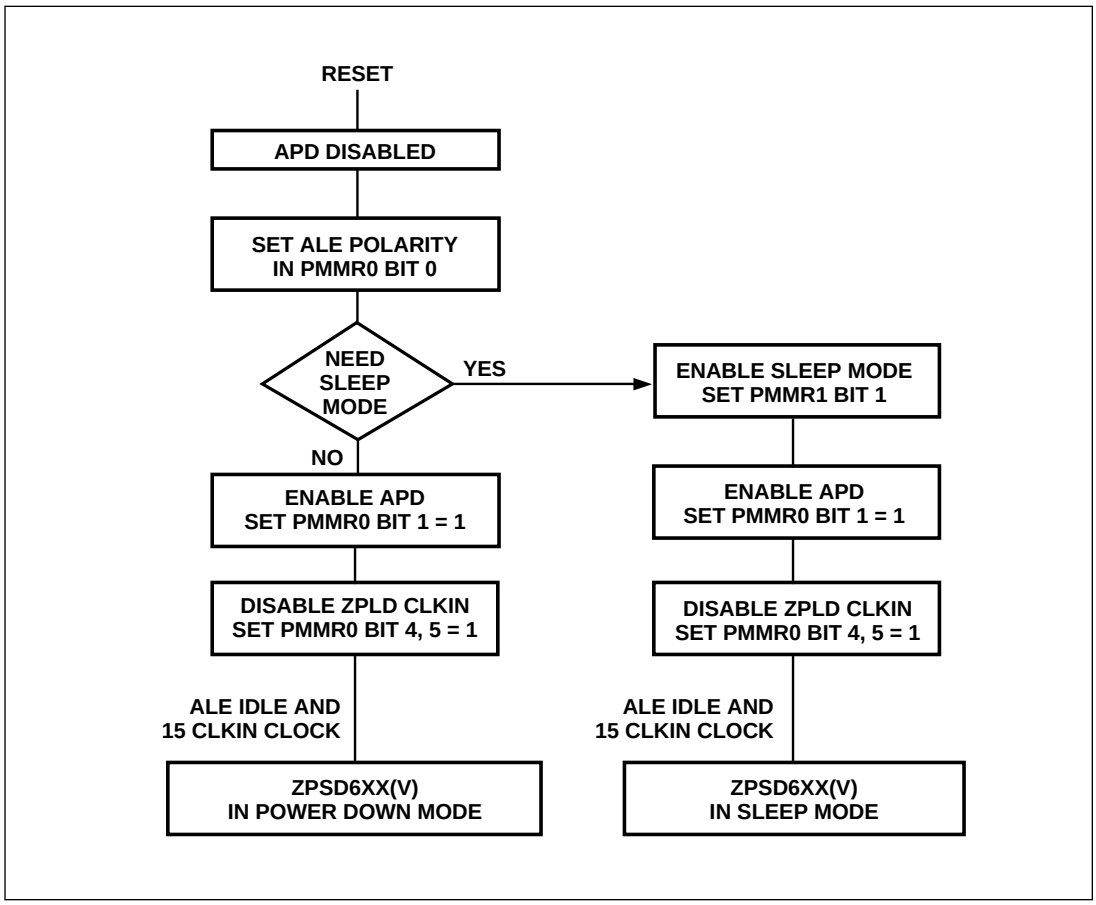


Figure 29. Enable Power Down Flow Chart



Power Management Unit (cont.)

Table 32. Power Management Mode Registers (PMMR0, PMMR1)**

PMMR0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	ZPLD Mcell clk	ZPLD Array clk	ZPLD Turbo	CMiser	APD Enable	ALE PD Polarity
		1 = off	1 = off	1 = off	1 = on	1 = on	1 = high

*Bit 6 and 7 are not used, should set to 0.

**Both the PMMR0 and PMMR1 register bits are clear to zero following power up. Subsequent reset pulses will not clear the registers.

Bit 0 0 = ALE power down polarity low
1 = ALE power down polarity high

Bit 1 0 = Automatic Power Down (APD) is disabled
1 = Automatic Power Down (APD) is enabled

Bit 2 0 = EPROM/SRAM CMiser is off
1 = EPROM/SRAM CMiser is on

Bit 3 0 = ZPLD Turbo is on
1 = ZPLD Turbo is off

Bit 4 0 = CLKIN input to the ZPLD AND array is connected
Every CLKIN change will power up the ZPLD when Turbo bit is off
1 = CLKIN input to ZPLD AND array is disconnected

Bit 5 0 = CLKIN input to the ZPLD Micro⇔Cells is connected
1 = CLKIN input to ZPLD Micro⇔Cells is disconnected

PMMR1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	*	*	Sleep Mode Enable	*
						1 = on	

*Not used bits should be set to 0.

Bit 1 0 = Sleep Mode is Disabled
1 = Sleep Mode is Enabled

Table 33. APD Counter Operation

APD Enable Bit	ALE PD Polarity	ALE Level	APD Counter
0	X	X	Not Counting
1	X	Pulsing	Not Counting
1	1	1	Counting (Generates PDN after 15 Clocks)
1	0	0	Counting (Generates PDN after 15 Clocks)

Power Management Unit (cont.)

Other Power Saving Options

The ZPSD6XX(V) offers other reduced power saving options that are independent of the Power Down or Sleep Mode. Except for the SRAM Standby and CSI input features, they are enabled by setting bits in the PMMR 0 register.

❑ CMiser Bit

The CMiser bit resides in PMMR0. This bit controls the AC power consumption and access time of the EPROM and SRAM. When in 8-bit data bus mode and CMiser is set, the ZPSD6XX(V) will consume the lowest level of AC power. However, the access time will be slower (see CMiser adder in timing parameters). When CMiser bit is off, the AC power is higher and the ZPSD6XX(V) will return to standard access time.

❑ SRAM Standby Mode

The SRAM has a dedicated Vstby pin (PC2) that can be connected to a battery. When V_{CC} becomes lower than Vstby then the ZPSD6XX(V) will automatically connect the Vstby as a power source to the SRAM. The SRAM Standby Current (Istby) is typically 0.5µA. SRAM data retention voltage is 2V minimum.

❑ The CSI Input

Pin PD2 of Port D can be configured in PSDsoft as the CSI input . When low, the signal selects and enables the internal EPROM and SRAM for read or write operations. A high on the CSI pin will disable the EPROM and SRAM and reduce the PSD power consumption. However, the ZPLD remains operational when CSI is high.

❑ Zero Power ZPLD

The power and speed of the ZPLD is controlled by the Turbo bit (bit 3) in the PMMR0. After reset the ZPLD is in Turbo mode and runs at full power and speed. By setting the bit to one, the Turbo mode is disabled and the ZPLD is consuming Zero Power current if the inputs are not switching for an extended time of 70ns. The propagation delay time will be increased by 10ns after the Turbo bit is set to one (turned off) if the inputs change at a frequency of less than 15MHz.

The Turbo bit and CMiser are independent of each other. The Turbo bit controls only the ZPLD DC power and propagation delay. The CMiser bit affects the EPROM and SRAM AC power and access time only.

❑ Input Clock

The ZPSD6XX(V) provides the option to turn off the CLKIN input to the ZPLD to save AC power consumption. The CLKIN is an input to the ZPLD AND array and the Output Micro⇔Cells. During power down or if any of the CLKIN input is not being used as part of the ZPLD logic equation, the clock should be disabled to save AC power.

The CLKIN will be disconnected from the ZPLD AND array or the Micro⇔Cells by setting bit 4 or 5 to “1” in the PMMR0.

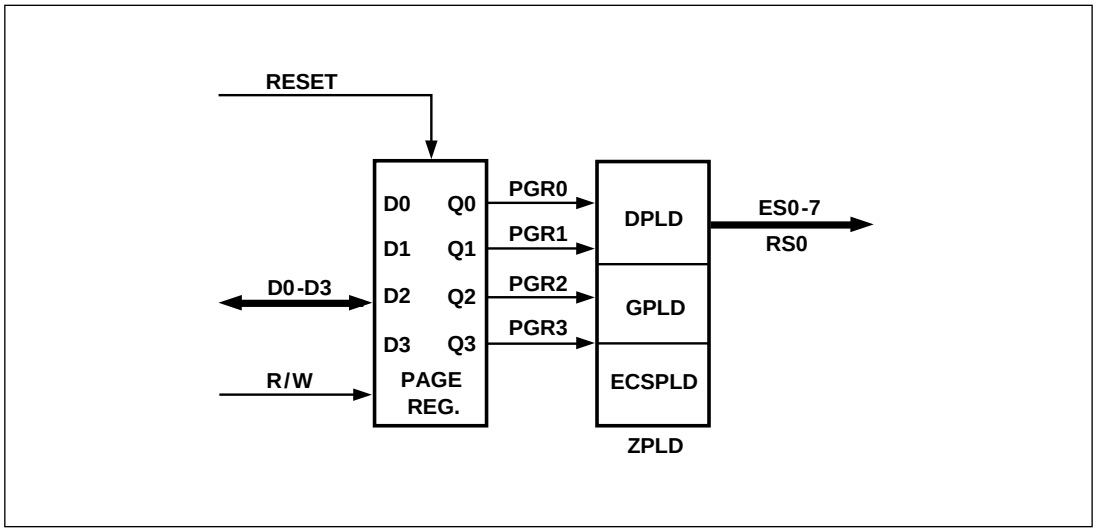
Power Management Unit (cont.)

Page Register

The four-bit Page Register increases the addressing capability of the microcontroller by a factor of 16. The contents of the Register can also be read by the microcontroller. The outputs of the Page Register (PGR0-PGR3) are inputs to the ZPLD and can be included in the EPROM or SRAM chip select equations.

Figure 30 shows the Page Register. The four Flip-Flops in the Register are connected to the internal data bus D0 – D3. The microcontroller can write to or read from the Page Register. The Register can operate as an independent register to the microcontroller if page mode is not implemented.

Figure 30. Page Register



Reset Input

The ZPSD6XX(V) has an active low reset input which loads internal configurations and clear some of the registers. Figure 42 shows the reset timing requirement. The active low range has a minimum tNLNH duration. After the rising edge of reset, the ZPSD6XX(V) remains in the reset state during tOPR range. The device must be reset at power-up prior to use.

While the reset input is active, the ZPLD is active and the outputs are determined by the PSDabel equations. The chip status during reset and power down is shown in Table 34.

Power Management Unit (cont.)

Table 34. Chip Status During Reset and Power Down Mode

Port Configuration	Reset	Power Down Mode
MCU I/O	Input	Unchanged
ZPLD Output	Active	Depends on inputs to the ZPLD
Address Out	Tri-stated	Not defined
Data Port	Tri-stated	Tri-stated
Peripheral I/O	Tri-stated	Tri-stated

Register	Reset	Power Down Mode
PMMR0 & 1	Cleared (power up reset) Unchanged (warm reset)	Unchanged
Micro⇔Cells Flip-Flop	Unchanged*	Unchanged*
All other registers	Cleared to “0”	Unchanged

*The Micro⇔Cell Flip-Flop can be cleared or set by the reset input or the PDN (Power Down) signal, depending on the .re and .pr equations that are defined in the PSDabel file.

Battery Backup

The ZPSD6XX(V) supports a battery backup operation that retains the contents of the SRAM in the event of a power loss. The Port PC2 pin is dedicated as the input pin for an external power source. If the supply voltage falls below a reference voltage (Vstby), an internal power-switch occurs so that PC2 provides power to the internal SRAM. The SRAM contents are retained down to a level of 2V.

Security Protection

The ZPSD6XX(V) has a programmable security bit which inhibits duplication. When the bit is set, the contents of the EPROM, non-volatile configuration bits, and ZPLD cannot be read by device programmers.

The security bit is set through the PSDsoft Software and is embedded in the compiled output file. The security bit is UV erasable and a secured ZPSD6XX(V) in a windowed package can be erased and re-programmed.

Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CLDCC	– 65	+ 150	°C
		PLDCC	– 65	+ 125	°C
	Operating Temperature	Commercial	0	+ 70	°C
		Industrial	– 40	+ 85	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection		>2000		V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance				
			-70	-90	-15	-20	-25
Commercial	0° C to +70°C	+ 5 V	± 10%		± 10%		
Industrial	–40° C to +85°C	+ 5 V		± 10%	± 10%		
Commercial	0° C to +70°C	+ 3 V				± 10%	± 10%
Industrial	–40° C to +85°C	+ 3 V					± 10%

Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V_{CC}	Supply Voltage	V-Versions All Speeds	2.7		5.5	V

AC/DC Parameters

The following tables describe the AD/DC parameters of the ZPSD6XX(V) family:

- ❏ DC Electrical Specification
- ❏ AC Timing Specification
  - ZPLD Timing
    - – Combinatorial Timing
    - – Synchronous Clock Mode
    - – Asynchronous Clock Mode
    - – Input Micro⇔Cell Timing
  - Microcontroller Timing
    - – Read Timing
    - – Write Timing
    - – Peripheral Mode Timing
    - – Power Down and Reset Timing

Following are some issues concerning the parameters presented:

- ❏ In the DC specification the Supply Current is given for different modes of operation. Before calculating the total power consumption, determine the percentage of time that the ZPSD6XX(V) is in each mode. Also the supply power is considerably different if the ZPLD_TURBO bit is "OFF" and EPROM_CMISER is "ON".
- ❏ The AC power component gives the ZPLD, EPROM, and SRAM mA/MHz specification. Figures 31 and 31a show the ZPLD mA/MHz as a function of the number of Product Terms (PT) used.
- ❏ In the ZPLD timing parameters add the required delay when ZPLD_TURBO is "OFF".
- ❏ In the MCU timing specification add the required time delay when EPROM_CMISER is "ON".

Figure 31. ZPLD I_{CC}/Frequency Consumption

(V_{CC} = 5 V ± 10%)

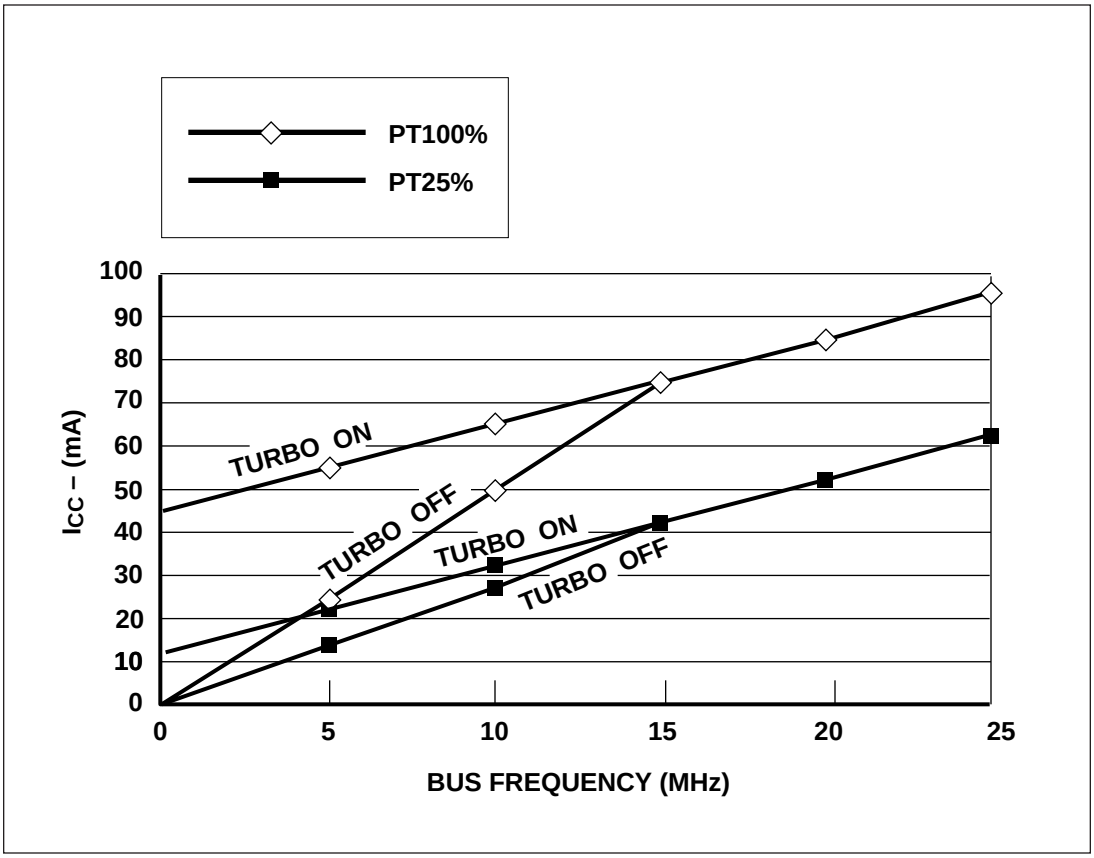
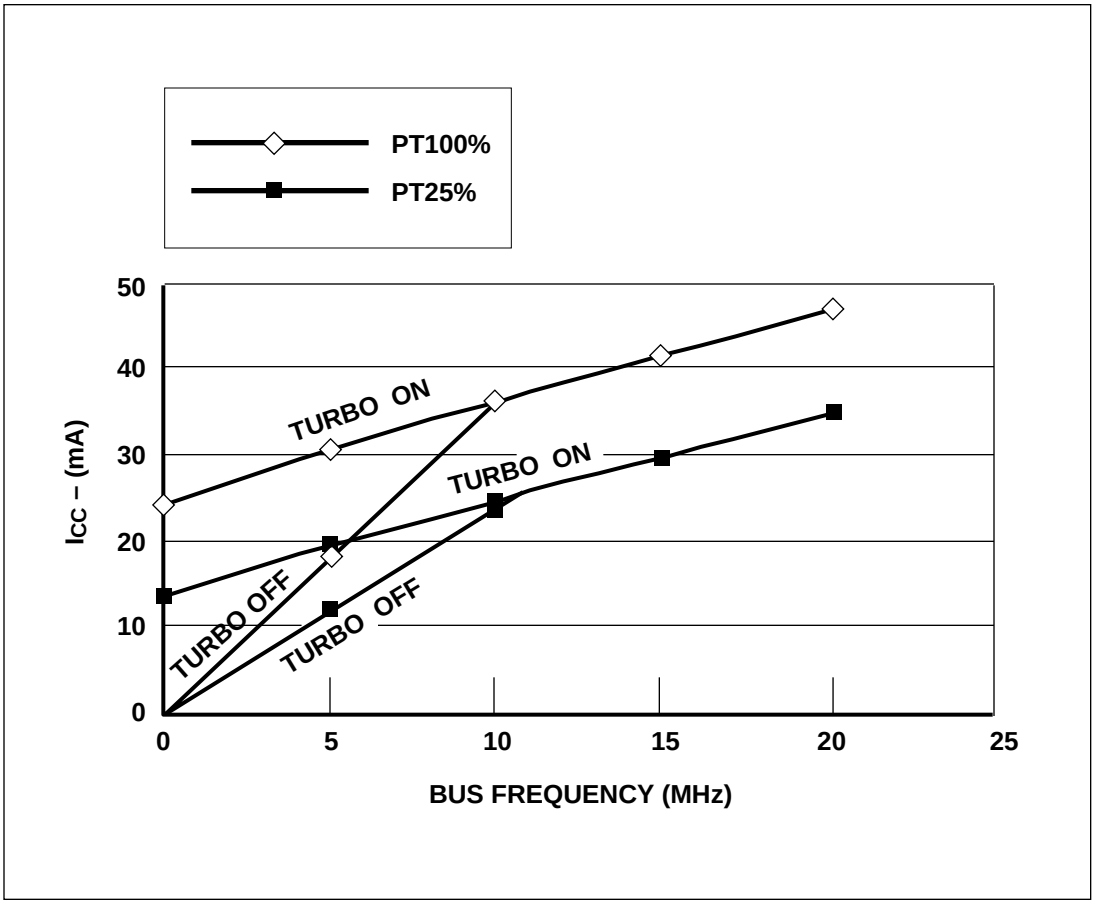


Figure 31a. ZPLD I_{CC}/Frequency Consumption

(ZPSD6XXV Versions, V_{CC} = 3 V ± 10%)



DC Characteristics (5 V ± 10% Versions)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		All Speeds	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		4.5 V < V_{CC} < 5.5 V	2		V_{CC} +.5	V
V_{IL}	Low Level Input Voltage		4.5 V < V_{CC} < 5.5 V	–0.5		0.8	V
V_{IH1}	Reset High Level Input Voltage		(Note 1)	.8 V_{CC}		V_{CC} +.5	V
V_{IL1}	Reset Low Level Input Voltage		(Note 1)	–.5		.2 V_{CC} –.1	V
V_{HYS}	Reset Pin Hysteresis			0.3			V
V_{OL}	Output Low Voltage		I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
			I_{OL} = 8 mA, V_{CC} = 4.5 V		0.15	0.45	V
V_{OH}	Output High Voltage		I_{OH} = –20 µA, V_{CC} = 4.5 V	4.4	4.49		V
			I_{OH} = –2 mA, V_{CC} = 4.5 V	2.4	3.9		V
V_{SBY}	SRAM Standby Voltage			2.0		V_{CC}	V
I_{SBY}	SRAM Standby Current		V_{CC} = 0 V		0.5	1	µA
I_{IDLE}	Idle Current (V_{STBY} Pin)		V_{CC} > V_{SBY}	–0.1		0.1	µA
V_{DF}	SRAM Data Retention Voltage		Only on V_{STBY}	2			V
I_{SB}	Standby Supply Current	Power Down Mode	$\overline{CSI}$ >V_{CC} –.3 V (Note 2)		25	50	µA
		Sleep Mode	$\overline{CSI}$ >V_{CC} –.3 V (Note 3)		10	20	µA
I_{LI}	Input Leakage Current		V_{SS} < V_{IN} > V_{CC}	–1	±.1	1	µA
I_{LO}	Output Leakage Current		.45 < V_{IN} > V_{CC}	–10	±5	10	µA
I_{CC} (DC) (Note 4a)	Operating Supply Current	ZPLD Only	ZPLD_TURBO = OFF, f = 0 MHz (Note 4)				Figure 31
			ZPLD_TURBO = ON, f = 0 MHz		400	700	µA/PT
I_{CC} (AC) (Note 4a)	ZPLD AC Base						Figure 31
	EPROM AC Adder		CMiser = ON, 8-Bit Bus Mode		0.8	2	mA/MHz
			All Other Cases		1.8	4	mA/MHz
	SRAM AC Adder		CMiser = ON, 8-Bit Bus Mode		1.4	2.7	mA/MHz
			CMiser = ON, 16-Bit Bus Mode		2	4	mA/MHz
			CMiser = OFF		3.8	7.5	mA/MHz

NOTES: 1. Reset input has hysteresis. V_{IL1} is valid at or below .2V_{CC} –.1. V_{IH1} is valid at or above .8V_{CC}.
2. $\overline{CSI}$ deselected or internal PD is active.
3. Sleep mode bit is set and internal PD is active.
4. See ZPLD ICC/Frequency Power Consumption graph for details.
4a. I_{OUT} = 0 mA

GPLD and ECSPLD Combinatorial Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-70		-90		-15		PT Aloc	TURBO OFF	Slew Rate	Unit
			Min	Max	Min	Max	Min	Max				
t_{PD1}	ECSPLD Input Pin to ECSPLD Combinatorial Output	(Notes 1 & 2)		18		20		24		Add 10	Add 3	ns
t_{PD2}	GPLD Input Pin/Feedback to GPLD Combinatorial Output Port C	(Note 2a)		25		28		32	Add 2	Add 10		ns
t_{PD3}	GPLD Input Pin/Feedback to GPLD Combinatorial Output Port A or B	(Note 2a)		27		30		34		Add 10		ns
t_{EA}	GPLD Input to ECSPLD Output Enable	(Notes 2 & 2a)		23		25		29		Add 10	Add 3	ns
	GPLD Input to GPLD Output Enable	(Notes 2a & 2b)		26		28		32		Add 10		ns
t_{ER}	GPLD Input to ECSPLD Output Disable	(Notes 2 & 2a)		23		25		29		Add 10	Add 3	ns
	GPLD Input to GPLD Output Disable	(Notes 2a & 2b)		26		28		32		Add 10		ns
t_{ARP}	GPLD Register Clear or Preset Delay	Any Micro⇔Cell (Notes 2a & 2b)		26		29		33		Add 10		ns
t_{ARPW}	GPLD Register Clear or Preset Pulse Width	Any Micro⇔Cell (Notes 2a & 2b)	20		25		29					ns
t_{ARD}	GPLD Array Delay	Any Micro⇔Cell		16		18		22	Add 2			ns

NOTES:1. ECSPLD Input pins are A(0:15), PGR(0:3), CNTL(0:2), PDN.
2. ECSPLD Outputs are PA(0:3), PB(0:3), PD(0:2).
2a. GPLD Inputs are A(0:15), PGR(0:3), CNTL(0:2), PA(0:7), PB(0:7), PC(0:7), PD(0:2), ALE, PDN. Add 25ns for propagation delay from $\overline{\text{RESET}}$ pin.
2b. GPLD Outputs are PA(4:7), PB(4:7), PC(0:7).

ZPSD6XX(V) AC/DC Parameters – GPLD and ECSPLD Timing Parameters

(5 V ± 10% Versions)

GPLD Micro⇔Cell Synchronous Clock Mode Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-70		-90		-15		PT Aloc	TURBO OFF	Slew Rate	Unit
			Min	Max	Min	Max	Min	Max				
f_{MAX}	Maximum Frequency External Feedback	$1/(t_S+t_{CO})$		30.30		27.03		25.00				MHz
	Maximum Frequency Internal Feedback (f_{CNT})	$1/(t_S+t_{CO}-10)$		43.48		37.04		31.25				MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH}+t_{CL})$		50.00		41.67		35.71				MHz
t_S	Input Setup Time	(Note 2a)	15		17		20		Add 2	Add 10		ns
t_H	Input Hold Time	(Note 2a)	0		0		0					ns
t_{CH}	Clock High Time	Clock Input	10		12		15					ns
t_{CL}	Clock Low Time	Clock Input	10		12		15					ns
t_{CO}	Clock to Output Delay	Clock Input		18		20		22				ns
t_{ARD}	GPLD Array Delay	Any Micro⇔Cell		16		18		22	Add 2			ns
t_{MIN}	Minimum Clock Period	$t_{CH}+t_{CL}$	20		24		29					ns

NOTES: 2a. GPLD Inputs are A(0:15), PGR(0:3), CNTL(0:2), PA(0:7), PB(0:7), PC(0:7), PD(0:2), ALE, PDN. Add 25ns for propagation delay from $\overline{\text{RESET}}$ pin.
2c. CLKIN $t_{CLCL} = t_{CH} + t_{CL}$.

ZPSD6XX(V) AC/DC Parameters – GPLD and ECSPLD Timing Parameters

(5 V ± 10% Versions)

GPLD Micro⇔Cell Asynchronous Clock Mode Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-70		-90		-15		PT Aloc	TURBO OFF	Slew Rate	Unit
			Min	Max	Min	Max	Min	Max				
f_{MAXA}	Maximum Frequency External Feedback	$1/(t_{SA}+t_{COA})$		26.32		25.00		21.74				MHz
	Maximum Frequency Internal Feedback (f_{CNTA})	$1/(t_{SA}+t_{COA}–10)$		35.71		33.33		27.78				MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH}+t_{CL})$		41.67		41.67		35.71				MHz
t_{SA}	Input Setup Time	(Note 2a)	8		8		12		Add 2	Add 10		ns
t_{HA}	Input Hold Time	(Note 2a)	8		8		12					ns
t_{CHA}	Clock Input High Time	(Note 2a)	12		12		15					ns
t_{CLA}	Clock Input Low Time	(Note 2a)	12		12		15					ns
t_{COA}	Clock to Output Delay	(Note 2a)		30		32		37		Add 10		ns
t_{ARD}	GPLD Array Delay	Any Micro⇔Cell		16		18		22	Add 2			ns
t_{MINA}	Minimum Clock Period	$1/f_{CNTA}$	28		30		43					ns

NOTES: 2a. GPLD Inputs are A(0:15), PGR(0:3), CNTL(0:2), PA(0:7), PB(0:7), PC(0:7), PD(0:2), ALE, PDN. Add 25ns for propagation delay from $\overline{\text{RESET}}$ pin.
2c. CLKIN $t_{CLCL} = t_{CH} + t_{CL}$.

ZPSD6XX(V) AC/DC Parameters – GPLD and ECSPLD Timing Parameters

(5 V ± 10% Versions)

Input Micro⇔Cell Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-70		-90		-15		PT Aloc	TURBO OFF	Unit
			Min	Max	Min	Max	Min	Max			
t_{IS}	Input Setup Time	(Note 2d)	0		0		0			Add 10	ns
t_{IH}	Input Hold Time	(Note 2d)	20		22		26				ns
t_{INH}	NIB Input High Time	(Note 2d)	12		14		18				ns
t_{INL}	NIB Input Low Time	(Note 2d)	12		14		18				ns
t_{INO}	NIB Input to Combinatorial Output Delay	(Note 2d)		46		51		59	Add 2	Add 10	ns

NOTES: 2d. Inputs from Port A, B and C relative to register/latch clock from the PLD. ALE latch timings refer to t_{AVLX} and t_{LXAX}.

Microcontroller Interface – AC/DC Parameters

(5V ± 10% Versions)

Explanation of AC Symbols for Non ZPLD Timing.

Example: t_{AVLX} – Time from Address Valid to ALE Invalid.

Signal Letters

A – Address Input
C – CEout Output
D – Input Data
E – E Input
G – Internal WDOG_ON signal
I – Interrupt Input
L – ALE Input
N – Reset Input or Output
P – Port Signal Output
Q – Output Data
R – $\overline{WR}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{DS}$, IORD, $\overline{PSEN}$ Inputs
S – Chip Select Input
T – R/$\overline{W}$ Input
W – Internal PDN Signal
B – Vstby Output
M – Output Micro⇔Cell

Signal Behavior

t – Time
L – Logic Level Low or ALE
H – Logic Level High
V – Valid
X – No Longer a Valid Logic Level
Z – Float
PW – Pulse Width

Microcontroller Interface – AC/DC Parameters

(5V ± 10% Versions)

Read Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-70		-90		-15		CMiser ON	Unit
			Min	Max	Min	Max	Min	Max		
t_{LVLX}	ALE or AS Pulse Width		18		20		28		0	ns
t_{AVLX}	Address Setup Time	(Note 4)	5		6		10		0	ns
t_{LXAX}	Address Hold Time	(Note 4)	7		8		11		0	ns
t_{AVQV}	Address Valid to Data Valid	(Note 4)		70		90		150	Add 10	ns
t_{SLQV}	CS Valid to Data Valid			80		100		150	Add 10	ns
t_{RLQV}	$\overline{RD}$ to Data Valid 8/16-Bit Bus	(Note 3)		20		32		40	0	ns
	$\overline{RD}$ to Data Valid 8-Bit Bus, 8031, 80251 Separate Mode	(Note 3a)		32		38		45	0	ns
t_{RHQX}	$\overline{RD}$ Data Hold Time	(Note 3)	0		0		0		0	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	(Note 3)	30		32		38		0	ns
t_{RHQZ}	$\overline{RD}$ to Data High-Z	(Note 3)		22		25		33	0	ns
t_{EHEL}	E Pulse Width		30		32		38		0	ns
t_{THEH}	R/$\overline{W}$ Setup Time to Enable		8		10		18		0	ns
t_{ELTL}	R/$\overline{W}$ Hold Time After Enable		0		0		0		0	ns
t_{AVPV}	Address Input Valid to Address Output Delay	In 16-Bit Bus Mode (Note 5)		20		30		38	0	ns
		In 8-Bit Bus Mode (Note 5)		22		32		48	0	ns

NOTES: 3. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, PSEN (in 8031 combined mode) signals.

3a. $\overline{RD}$ and $\overline{PSEN}$ have the same timing for 8031 separate mode.

4. Any input used to select an internal ZPSD6XX(V) function.

5. In multiplexed mode latched address generated from ADIO delay to address output on any Port.

Write Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-70		-90		-15		Unit
			Min	Max	Min	Max	Min	Max	
t_{LVLX}	ALE or AS Pulse Width		18		20		28		ns
t_{AVLX}	Address Setup Time	(Note 4)	5		6		10		ns
t_{LXAX}	Address Hold Time	(Note 4)	7		8		11		ns
t_{AVWL}	Address Valid to Leading Edge of $\overline{WR}$	(Notes 4 and 6)	18		20		30		ns
t_{SLWL}	$\overline{CS}$ Valid to Leading Edge of $\overline{WR}$	(Note 6)	22		25		35		ns
t_{DVWH}	$\overline{WR}$ Data Setup Time	(Note 6)	12		15		22		ns
t_{WHDX}	$\overline{WR}$ Data Hold Time	(Note 6)	5		5		5		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	(Note 6)	18		20		28		ns
t_{WHAX}	Trailing Edge of $\overline{WR}$ to Address Invalid	(Note 6)	0		0		0		ns
t_{WHPV}	Trailing Edge of $\overline{WR}$ to Port Output Valid Using I/O Port Data Register	(Note 6)		25		30		38	ns
t_{WLMV}	$\overline{WR}$ Valid to Port Output Valid Using Micro⇔Cell Register Load	(Notes 6 and 6a)		25		30		38	ns
t_{DVMV}	Data Valid to Port Output Valid Using Micro⇔Cell Register Data In	(Notes 6 and 6b)		25		30		38	ns
t_{AVPV}	Address Input Valid to Address Output Delay	In 16-Bit Bus Mode (Note 5)		20		30		38	ns
		In 8-Bit Bus Mode (Note 5)		22		32		48	ns

NOTE: 6. $\overline{WR}$ timing has the same timing as E, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{WRL}$, $\overline{WRH}$ signals.
6a. Assuming data is stable before active write signal.
6b. Assuming write is active before data becomes valid.

Port A Peripheral Data Mode Read Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90		-15		TURBO OFF	Unit
			Min	Max	Min	Max	Min	Max		
$t_{AVQV\ (PA)}$	Address Valid to Data Valid	(Note 7)		45		55		62	Add 10	ns
$t_{SLQV\ (PA)}$	$\overline{CS}$ Valid to Data Valid			55		55		62	Add 10	ns
$t_{RLQV\ (PA)}$	$\overline{RD}$ to Data Valid	(Notes 3, 8)		22		32		40		ns
	$\overline{RD}$ to Data Valid 8031 Mode			32		38		45		ns
$t_{DVQV\ (PA)}$	Data In to Data Out Valid			22		22		26		ns
$t_{QXRH\ (PA)}$	$\overline{RD}$ Data Hold Time	(Note 3)	0		0		0			ns
$t_{RLRH\ (PA)}$	$\overline{RD}$ Pulse Width	(Note 3)	30		32		38			ns
$t_{RHQZ\ (PA)}$	$\overline{RD}$ to Data High-Z	(Note 3)		20		25		33		ns

Port A Peripheral Data Mode Write Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90		-15		TURBO OFF	Unit
			Min	Max	Min	Max	Min	Max		
$t_{WLQV\ (PA)}$	$\overline{WR}$ to Data Propagation Delay	(Note 6)		25		27		35		ns
$t_{DVQV\ (PA)}$	Data to Port A Data Propagation Delay	(Note 9)		22		22		26		ns
$t_{WHQZ\ (PA)}$	$\overline{WR}$ Invalid to Port A Tri-state	(Note 6)		20		25		33		ns

NOTES: 7. Any input used to select Port A Data Peripheral Mode.
8. Data is already stable on Port A.
9. Data stable on ADIO pins to data on Port A.

Power Down Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90		-15		TURBO OFF	Unit
			Min	Max	Min	Max	Min	Max		
t_{LVDV}	ALE Access Time from Power Down			100		120		150	Add 10	ns
t_{LVDV1}	ALE or $\overline{CSI}$ Access Time from Sleep			120		150		200		ns
t_{PD4}	GPLD and ECSPLD Propagation Delay in Sleep Mode			600		600		600		ns
t_{PD5}	GPLD and ECSPLD Recovery Time After Sleep Mode			250		250		250		ns
t_{CLWH}	Maximum Delay from APD Enable to Internal PDN Valid Signal	Using CLKIN Input	15* t_{CLCL} (µs)							µs

NOTES: 10. t_{CLCL} is the CLKIN clock period. See Fig 37.

Reset Timing (5 V ± 10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_1	RESET Active Low Time		150			ns
t_2	RESET High to Operational Device				120	ns

DC Characteristics (3 V ± 10% ZPSD6XXV Versions)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		All Speeds	2.7	3	5.5	V
V_{IH}	High Level Input Voltage		2.7 V < V_{CC} < 5.5 V	0.7 V_{CC}		V_{CC} +.5	V
V_{IL}	Low Level Input Voltage		2.7 V < V_{CC} < 5.5 V	–0.5		0.8	V
V_{IH1}	Reset High Level Input Voltage		(Note 1)	.8 V_{CC}		V_{CC} +.5	V
V_{IL1}	Reset Low Level Input Voltage		(Note 1)	–.5		.2 V_{CC} –.1	V
V_{HYS}	Reset Pin Hysteresis			0.3			V
V_{OL}	Output Low Voltage		I_{OL} = 20 µA, V_{CC} = 2.7 V		0.01	0.1	V
			I_{OL} = 4 mA, V_{CC} = 2.7 V		0.15	0.45	V
V_{OH}	Output High Voltage		I_{OH} = –20 µA, V_{CC} = 2.7 V	2.9	2.99		V
			I_{OH} = –1 mA, V_{CC} = 2.7 V	2.4	2.6		V
V_{SBY}	SRAM Standby Voltage			2.0		V_{CC}	V
I_{SBY}	SRAM Standby Current		V_{CC} = 0 V		0.5	1	µA
I_{IDLE}	Idle Current (V_{STBY} Pin)		V_{CC} > V_{SBY}	–0.1		0.1	µA
V_{DF}	SRAM Data Retention Voltage		Only on V_{STBY}	2			V
I_{SB}	Standby Supply Current	Power Down Mode	$\overline{CSI}$ >V_{CC} –.3 V (Note 2)		5	15	µA
		Sleep Mode	$\overline{CSI}$ >V_{CC} –.3 V (Note 3)		1	5	µA
I_{LI}	Input Leakage Current		V_{SS} < V_{IN} > V_{CC}	–1	±.1	1	µA
I_{LO}	Output Leakage Current		.45 < V_{IN} > V_{CC}	–10	±5	10	µA
I_{CC} (DC) (Note 4a)	Operating Supply Current	ZPLD Only	ZPLD_TURBO = OFF, f = 0 MHz (Note 4)				
			ZPLD_TURBO = ON, f = 0 MHz		200	400	µA/PT
I_{CC} (AC) (Note 4a)	ZPLD AC Base						
	EPROM AC Adder		CMiser = ON, 8-Bit Bus Mode		0.4	1.0	mA/MHz
			All Other Cases		0.9	1.7	mA/MHz
	SRAM AC Adder		CMiser = ON, 8-Bit Bus Mode		0.7	1.3	mA/MHz
			CMiser = ON, 16-Bit Bus Mode		1	2	mA/MHz
			CMiser = OFF		1.9	3.8	mA/MHz

NOTES: 1. Reset input has hysteresis. V_{IL1} is valid at or below .2V_{CC} –.1. V_{IH1} is valid at or above .8V_{CC}.
2. $\overline{CSI}$ deselected or internal PD is active.
3. Sleep mode bit is set and internal PD is active.
4. See ZPLD ICC/Frequency Power Consumption graph for details.
4a. I_{OUT} = 0 mA

ZPSD6XX(V) AC/DC Parameters – GPLD and ECSPLD Timing Parameters

(3 V ± 10% Versions)

GPLD and ECSPLD Combinatorial Timing (3 V ± 10% Versions)

Symbol	Parameter	Conditions	-20		-25		PT Aloc	TURBO OFF	Slew Rate	Unit
			Min	Max	Min	Max				
t_{PD1}	ECSPLD Input Pin to ECSPLD Combinatorial Output	(Notes 1 & 2)		34		39		Add 20	Add 6	ns
t_{PD2}	GPLD Input Pin/Feedback to GPLD Combinatorial Output Port C	(Note 2a)		55		63	Add 4	Add 20		ns
t_{PD3}	GPLD Input Pin/Feedback to GPLD Combinatorial Output Port A or B	(Note 2a)		55		63		Add 20		ns
t_{EA}	GPLD Input to ECSPLD Output Enable	(Notes 2 & 2a)		36		41		Add 20	Add 6	ns
	GPLD Input to GPLD Output Enable	(Notes 2a & 2b)		50		58		Add 20		ns
t_{ER}	GPLD Input to ECSPLD Output Disable	(Notes 2 & 2a)		36		41		Add 20	Add 6	ns
	GPLD Input to GPLD Output Disable	(Notes 2a & 2b)		50		58		Add 20		ns
t_{ARP}	GPLD Register Clear or Preset Delay	Any Micro⇔Cell (Notes 2a & 2b)		55		63		Add 20		ns
t_{ARPW}	GPLD Register Clear or Preset Pulse Width	Any Micro⇔Cell (Notes 2a & 2b)	35		40					ns
t_{ARD}	GPLD Array Delay	Any Micro⇔Cell		33		38	Add 4			ns

NOTES:1. ECSPLD Input pins are A(0:15), PGR(0:3), CNTL(0:2), PDN.
2. ECSPLD Outputs are PA(0:3), PB(0:3), PD(0:2).
2a. GPLD Inputs are A(0:15), PGR(0:3), CNTL(0:2), PA(0:7), PB(0:7), PC(0:7), PD(0:2), ALE, PDN. Add 25ns for propagation delay from $\overline{\text{RESET}}$ pin.
2b. GPLD Outputs are PA(4:7), PB(4:7), PC(0:7).

ZPSD6XX(V) AC/DC Parameters – GPLD and ECSPLD Timing Parameters

(3 V ± 10% Versions)

GPLD Micro⇔Cell Synchronous Clock Mode Timing (3 V ± 10% Versions)

Symbol	Parameter	Conditions	-20		-25		PT Aloc	TURBO OFF	Slew Rate	Unit
			Min	Max	Min	Max				
f_{MAX}	Maximum Frequency External Feedback	$1/(t_S+t_{CO})$		14.71		12.82				MHz
	Maximum Frequency Internal Feedback (f_{CNT})	$1/(t_S+t_{CO}-10)$		17.24		14.71				MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH}+t_{CL})$		31.25		27.78				MHz
t_S	Input Setup Time	(Note 2a)	35		40		Add 4	Add 20		ns
t_H	Input Hold Time	(Note 2a)	0		0					ns
t_{CH}	Clock High Time	Clock Input	16		18					ns
t_{CL}	Clock Low Time	Clock Input	16		18					ns
t_{CO}	Clock to Output Delay	Clock Input		33		38				ns
t_{ARD}	GPLD Array Delay	Any Micro⇔Cell		24		28	Add 4			ns
t_{MIN}	Minimum Clock Period	$t_{CH}+t_{CL}$	30		35					ns

NOTES: 2a. GPLD Inputs are A(0:15), PGR(0:3), CNTL(0:2), PA(0:7), PB(0:7), PC(0:7), PD(0:2), ALE, PDN. Add 25ns for propagation delay from $\overline{\text{RESET}}$ pin.
2c. CLKIN $t_{CLCL} = t_{CH} + t_{CL}$.

GPLD Micro⇔Cell Asynchronous Clock Mode Timing (3 V ± 10% Versions)

Symbol	Parameter	Conditions	-20		-25		PT Aloc	TURBO OFF	Slew Rate	Unit
			Min	Max	Min	Max				
f_{MAXA}	Maximum Frequency External Feedback	$1/(t_{SA}+t_{COA})$		14.71		12.82				MHz
	Maximum Frequency Internal Feedback (f_{CNTA})	$1/(t_{SA}+t_{COA}-10)$		17.24		14.71				MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH}+t_{CL})$		31.25		27.78				MHz
t_{SA}	Input Setup Time	(Note 2a)	13		15		Add 4	Add 20		ns
t_{HA}	Input Hold Time	(Note 2a)	13		15					ns
t_{CHA}	Clock Input High Time	(Note 2a)	16		18					ns
t_{CLA}	Clock Input Low Time	(Note 2a)	16		18					ns
t_{COA}	Clock to Output Delay	(Note 2a)		55		63		Add 20		ns
t_{ARD}	GPLD Array Delay	Any Micro⇔Cell		33		38	Add 4			ns
t_{MINA}	Minimum Clock Period	$1/f_{CNTA}$	58		67					ns

NOTES: 2a. GPLD Inputs are A(0:15), PGR(0:3), CNTL(0:2), PA(0:7), PB(0:7), PC(0:7), PD(0:2), ALE, PDN. Add 25ns for propagation delay from $\overline{\text{RESET}}$ pin.

ZPSD6XX(V) AC/DC Parameters – GPLD and ECSPLD Timing Parameters

(3 V ± 10% Versions)

Input Micro⇔Cell Timing (3 V ± 10% Versions)

Symbol	Parameter	Conditions	-20		-25		PT Aloc	TURBO OFF	Unit
			Min	Max	Min	Max			
t_{IS}	Input Setup Time	(Note 2d)	0		0			Add 20	ns
t_{IH}	Input Hold Time	(Note 2d)	35		40				ns
t_{INH}	NIB Input High Time	(Note 2d)	15		17				ns
t_{INL}	NIB Input Low Time	(Note 2d)	15		17				ns
t_{INO}	NIB Input to Combinatorial Output Delay	(Note 2d)		100		115	Add 4	Add 20	ns

NOTES:2d. Inputs from Port A, B and C relative to register/latch clock from the PLD. ALE latch timings refer to t_{AVLX} and t_{LXAX}.

Microcontroller Interface – ZPSD6XX(V) AC/DC Parameters

(3V ± 10% Versions)

Explanation of AC Symbols for Non ZPLD Timing.

Example: t_{AVLX} – Time from Address Valid to ALE Invalid.

Signal Letters

- **A** – Address Input
- **C** – CEout Output
- **D** – Input Data
- **E** – E Input
- **G** – Internal WDOG_ON signal
- **I** – Interrupt Input
- **L** – ALE Input
- **N** – Reset Input or Output
- **P** – Port Signal Output
- **Q** – Output Data
- **R** – $\overline{WR}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{DS}$, IORD, $\overline{PSEN}$ Inputs
- **S** – Chip Select Input
- **T** – R/$\overline{W}$ Input
- **W** – Internal PDN Signal
- **B** – Vstby Output
- **M** – Output Micro⇔Cell

Signal Behavior

- **t** – Time
- **L** – Logic Level Low or ALE
- **H** – Logic Level High
- **V** – Valid
- **X** – No Longer a Valid Logic Level
- **Z** – Float
- **PW** – Pulse Width

Microcontroller Interface – ZPSD6XX(V) AC/DC Parameters

(3V ± 10% Versions)

Read Timing (3 V ± 10% Versions)

Symbol	Parameter	Conditions	-20		-25		CMiser ON	Unit
			Min	Max	Min	Max		
t_{LVLX}	ALE or AS Pulse Width		30		35			ns
t_{AVLX}	Address Setup Time	(Note 4)	12		14			ns
t_{LXAX}	Address Hold Time	(Note 4)	12		14			ns
t_{AVQV}	Address Valid to Data Valid	(Note 4)		200		250	Add 20	ns
t_{SLQV}	$\overline{CS}$ Valid to Data Valid			200		250	Add 20	ns
t_{RLQV}	$\overline{RD}$ to Data Valid 8/16-Bit Bus	(Note 3)		50		58		ns
	$\overline{RD}$ to Data Valid 8-Bit Bus, 8031, 80251 Separate Mode	(Note 3a)		57		66		ns
t_{RHQX}	$\overline{RD}$ Data Hold Time	(Note 3)	0		0			ns
t_{RLRH}	$\overline{RD}$ Pulse Width	(Note 3)	40		46			ns
t_{RHQZ}	$\overline{RD}$ to Data High-Z	(Note 3)		45		52		ns
t_{EHEL}	E Pulse Width		40		46			ns
t_{THEH}	R/$\overline{W}$ Setup Time to Enable		20		23			ns
t_{ELTL}	R/$\overline{W}$ Hold Time After Enable		0		0			ns
t_{AVPV}	Address Input Valid to Address Output Delay	In 16-Bit Bus Mode (Note 5)		40		46		ns
		In 8-Bit Bus Mode (Note 5)		50		58		ns

NOTES: 3. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, PSEN (in 8031 combined mode) signals.

3a. $\overline{RD}$ and $\overline{PSEN}$ have the same timing for 8031 separate mode.

4. Any input used to select an internal ZPSD6XX(V) function.

5. In multiplexed mode latched address generated from ADIO delay to address output on any Port.

Write Timing (3 V ± 10% Versions)

Symbol	Parameter	Conditions	-20		-25		Unit
			Min	Max	Min	Max	
t_{LVLX}	ALE or AS Pulse Width		30		35		ns
t_{AVLX}	Address Setup Time	(Note 4)	12		14		ns
t_{LXAX}	Address Hold Time	(Note 4)	12		14		ns
t_{AVWL}	Address Valid to Leading Edge of $\overline{WR}$	(Notes 4 and 6)	35		40		ns
t_{SLWL}	$\overline{CS}$ Valid to Leading Edge of $\overline{WR}$	(Note 6)	40		46		ns
t_{DVWH}	$\overline{WR}$ Data Setup Time	(Note 6)	25		29		ns
t_{WHDX}	$\overline{WR}$ Data Hold Time	(Note 6)	5		6		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	(Note 6)	30		35		ns
t_{WHAX}	Trailing Edge of $\overline{WR}$ to Address Invalid	(Note 6)	0		0		ns
t_{WHPV}	Trailing Edge of $\overline{WR}$ to Port Output Valid Using I/O Port Data Register	(Note 6)		40		46	ns
t_{WLMV}	$\overline{WR}$ Valid to Port Output Valid Using Micro⇔Cell Register Load	(Notes 6 and 6a)		40		46	ns
t_{DVMV}	Data Valid to Port Output Valid Using Micro⇔Cell Register Data In	(Notes 6 and 6b)		40		46	ns
t_{AVPV}	Address Input Valid to Address Output Delay	In 16-Bit Bus Mode (Note 5)		40		46	ns
		In 8-Bit Bus Mode (Note 5)		50		58	ns

NOTE: 6. $\overline{WR}$ timing has the same timing as E, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{WRL}$, $\overline{WRH}$ signals.
6a. Assuming data is stable before active write signal.
6b. Assuming write is active before data becomes valid.

Port A Peripheral Data Mode Read Timing (3 V ± 10%)

Symbol	Parameter	Conditions	-20		-25		TURBO OFF	Unit
			Min	Max	Min	Max		
$t_{AVQV\ (PA)}$	Address Valid to Data Valid	(Note 7)		65		75	Add 20	ns
$t_{SLQV\ (PA)}$	$\overline{CS}$ Valid to Data Valid			80		92	Add 20	ns
$t_{RLQV\ (PA)}$	$\overline{RD}$ to Data Valid	(Notes 3 and 8)		45		52		ns
	$\overline{RD}$ to Data Valid 8031 Mode			50		58		ns
$t_{DVQV\ (PA)}$	Data In to Data Out Valid			35		40		ns
$t_{QXRH\ (PA)}$	$\overline{RD}$ Data Hold Time	(Note 3)	0		0			ns
$t_{RLRH\ (PA)}$	$\overline{RD}$ Pulse Width	(Note 3)	40		46			ns
$t_{RHQZ\ (PA)}$	$\overline{RD}$ to Data High-Z	(Note 3)		35		40		ns

Port A Peripheral Data Mode Write Timing (3 V ± 10%)

Symbol	Parameter	Conditions	-20		-25		TURBO OFF	Unit
			Min	Max	Min	Max		
$t_{WLQV\ (PA)}$	$\overline{WR}$ to Data Propagation Delay	(Note 6)		50		58		ns
$t_{DVQV\ (PA)}$	Data to Port A Data Propagation Delay	(Note 9)		40		46		ns
$t_{WHQZ\ (PA)}$	$\overline{WR}$ Invalid to Port A Tri-state	(Note 6)		35		40		ns

NOTES: 7. Any input used to select Port A Data Peripheral Mode.
8. Data is already stable on Port A.
9. Data stable on ADIO pins to data on Port A.

Power Down Timing (3 V ± 10%)

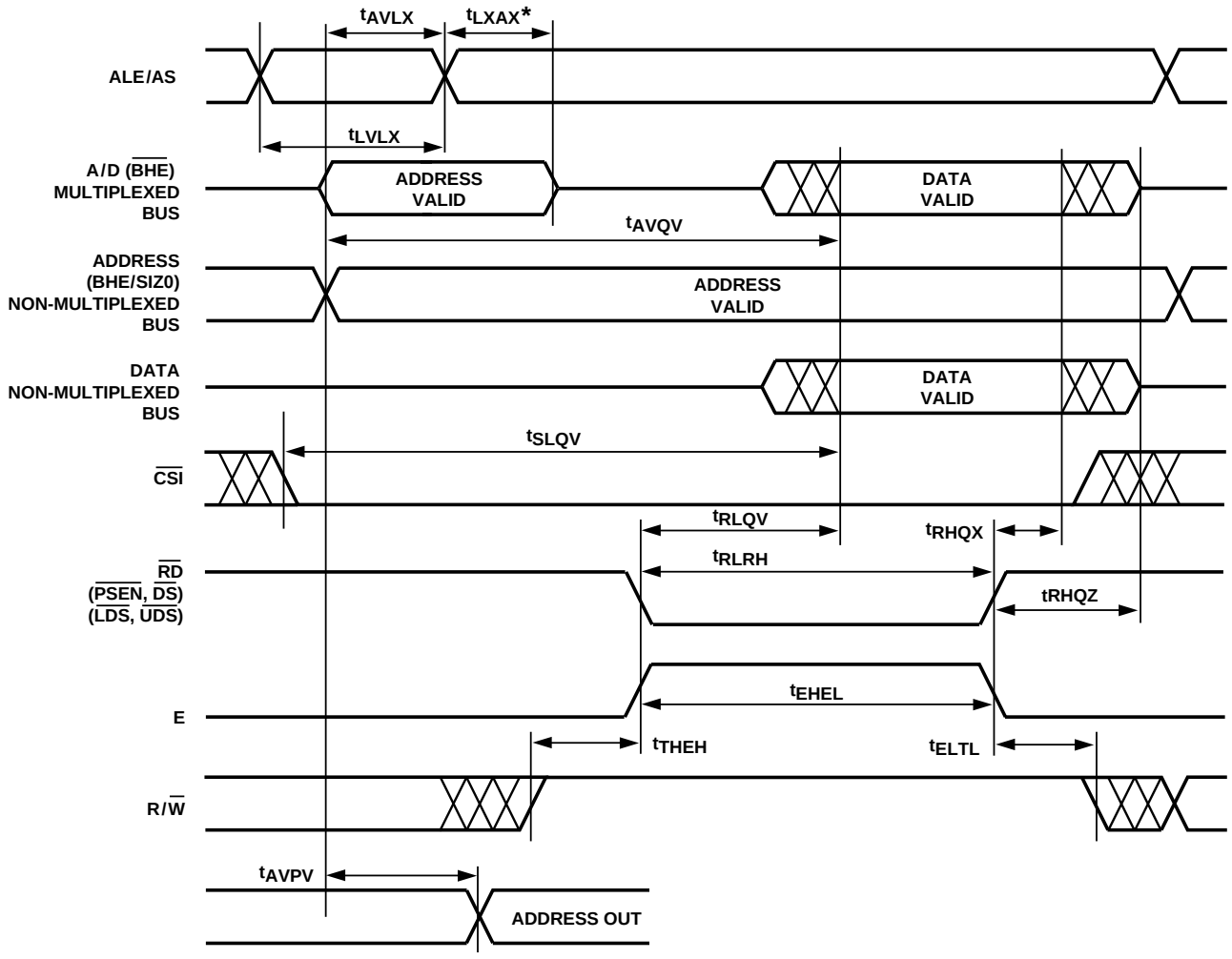
Symbol	Parameter	Conditions	-20		-25		TURBO OFF	Unit
			Min	Max	Min	Max		
t_{LVDV}	ALE Access Time from Power Down			200		250	Add 20	ns
t_{LVDV1}	ALE or $\overline{CSI}$ Access Time from Sleep			200		250		ns
t_{PD4}	GPLD and ECSPLD Propagation Delay in Sleep Mode			600		600		ns
t_{PD5}	GPLD and ECSPLD Recovery Time After Sleep Mode			250		250		ns
t_{CLWH}	Maximum Delay from APD Enable to Internal PDN Valid Signal	Using CLKIN Input	15* t_{CLCL} (µs)					µs

NOTE: 10. t_{CLCL} is the CLKIN clock period. See Figure 37.

Reset Timing (3 V ± 10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_1	RESET Active Low Time		300			ns
t_2	RESET High to Operational Device				300	ns

Figure 32. Read Timing



*t_{AVLX} and t_{LXAX} are not required for 80C251 in Page Mode or 80C51XA in Burst Mode.

Figure 33. Write Timing

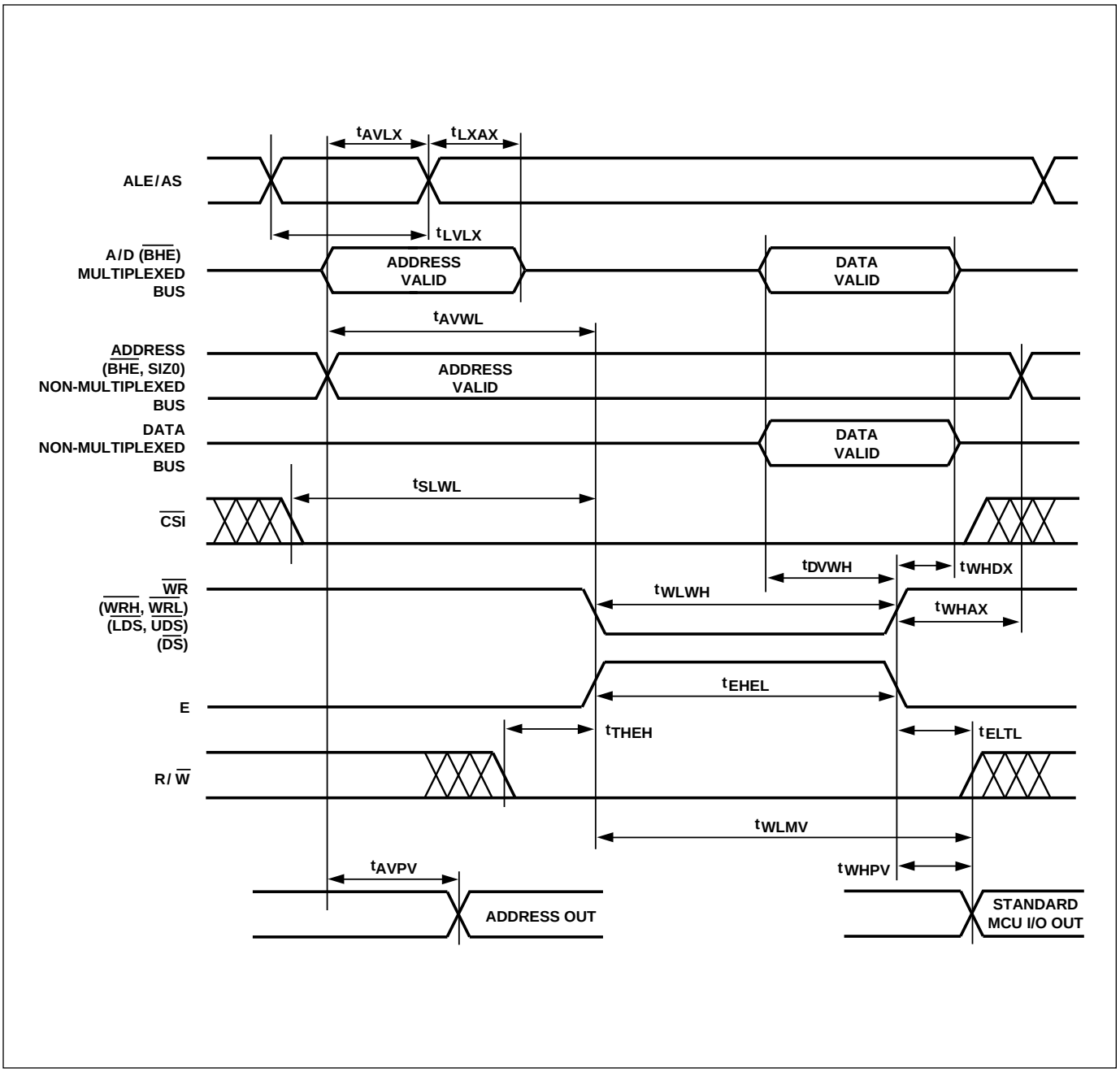


Figure 34. Peripheral I/O Read Timing

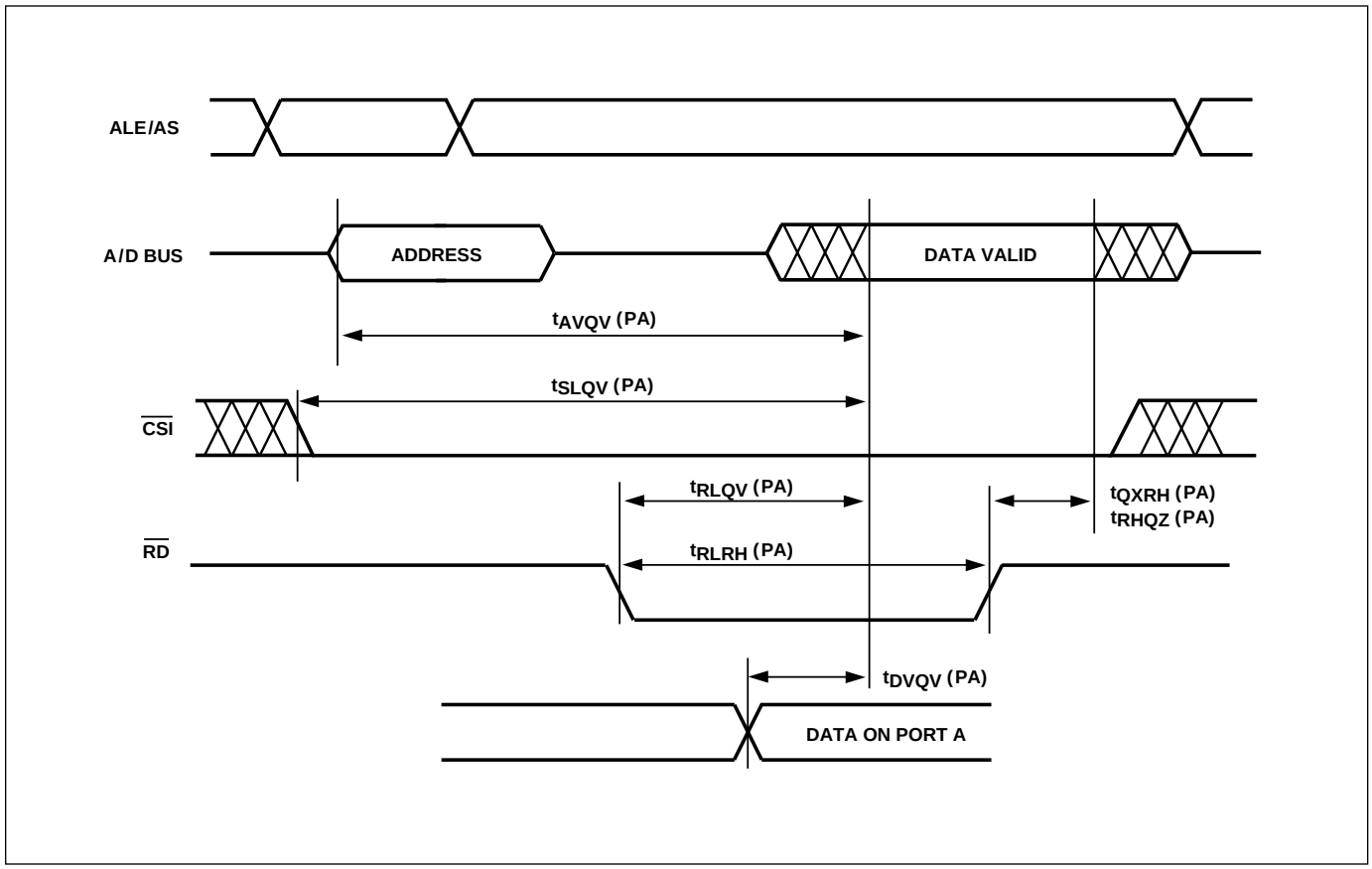


Figure 35. Peripheral I/O Write Timing

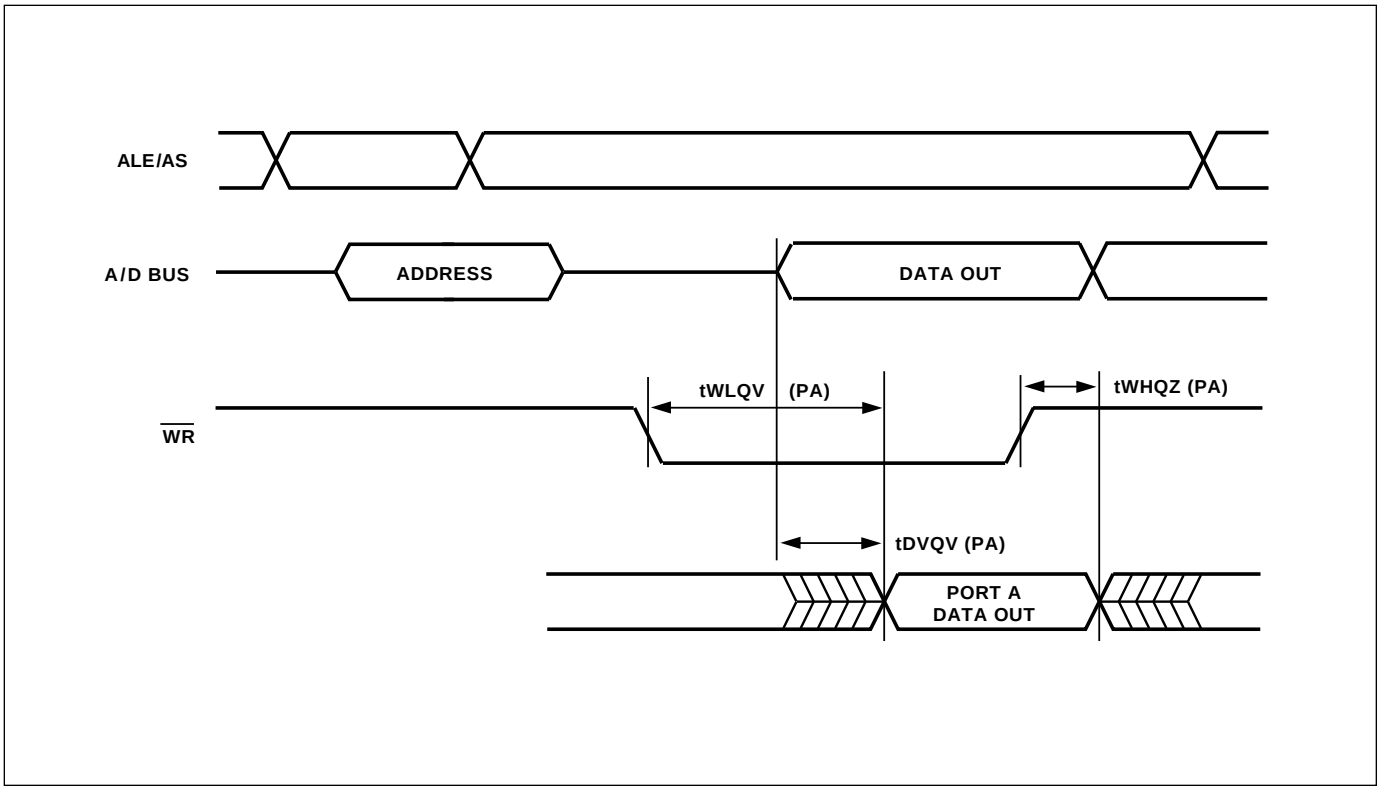


Figure 36. Combinatorial Timing – ZPLD

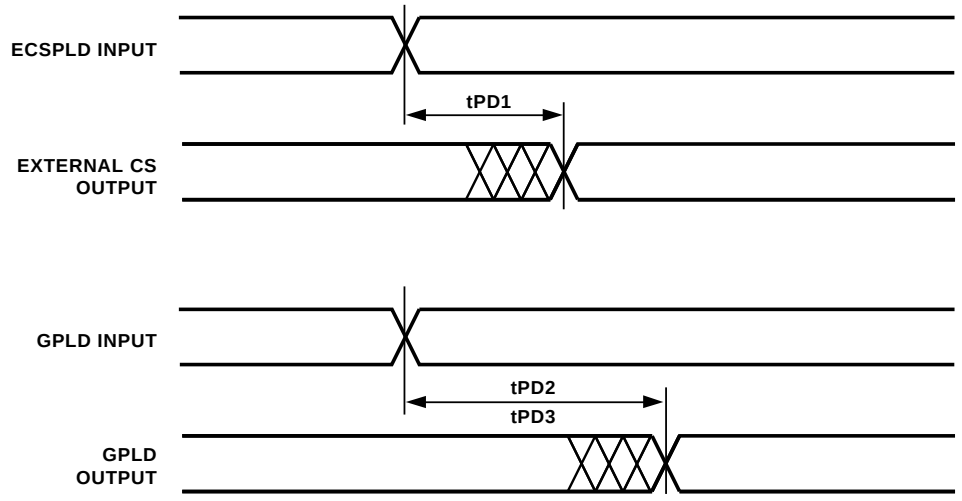


Figure 37. Synchronous Clock Mode Timing – ZPLD

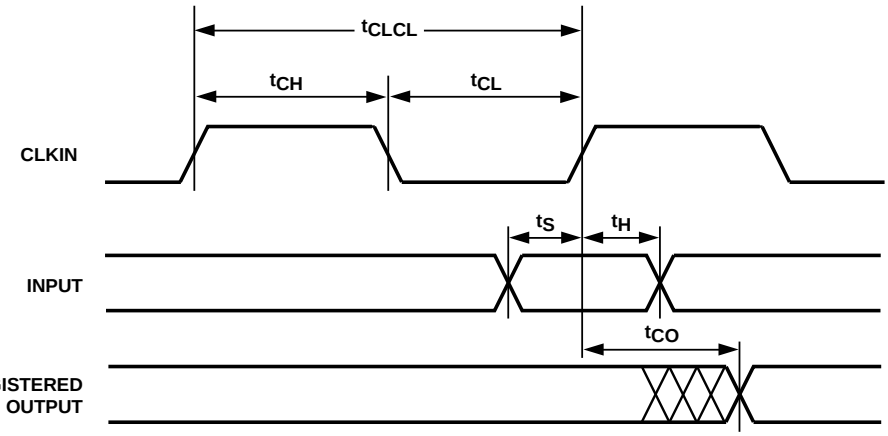


Figure 38. Asynchronous Clock Mode Timing (Product-Term Clock)

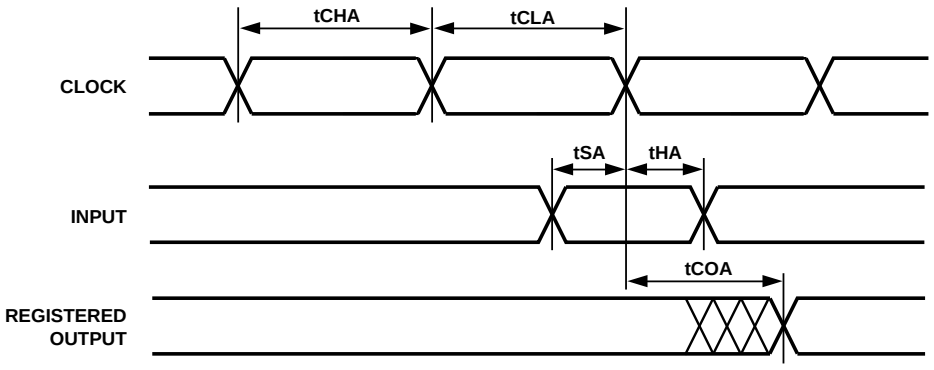


Figure 39. Input Micro⇔Cell Timing (Product-Term Clock)

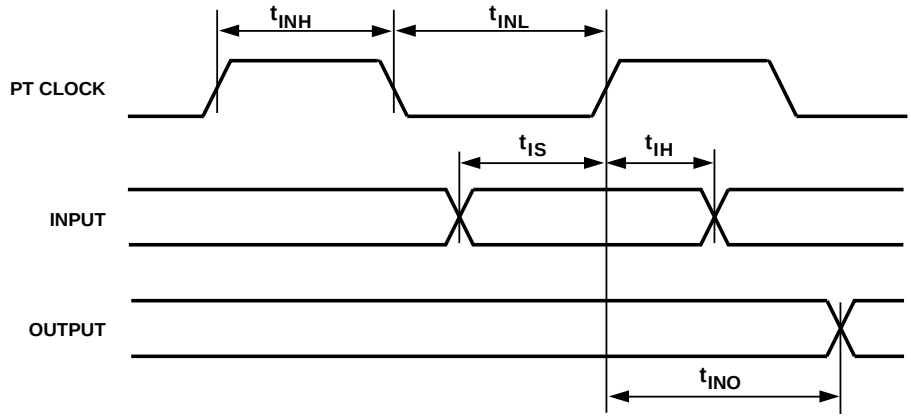


Figure 40. Input to Output Disable/Enable

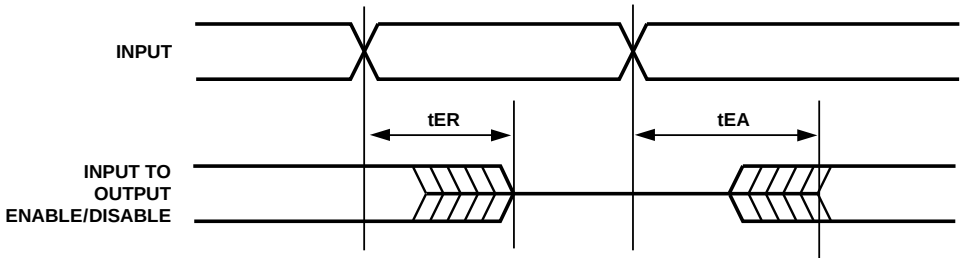


Figure 41. Asynchronous Reset/Preset

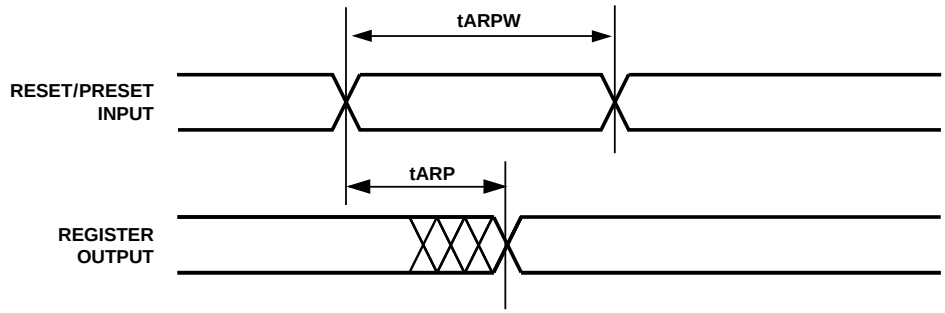


Figure 42. Reset Timing

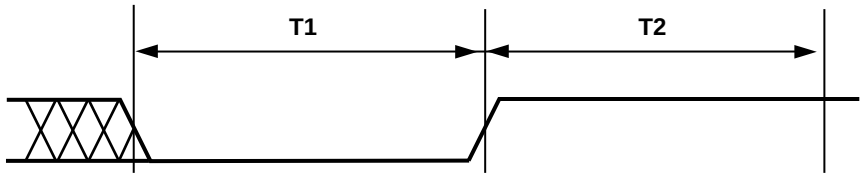
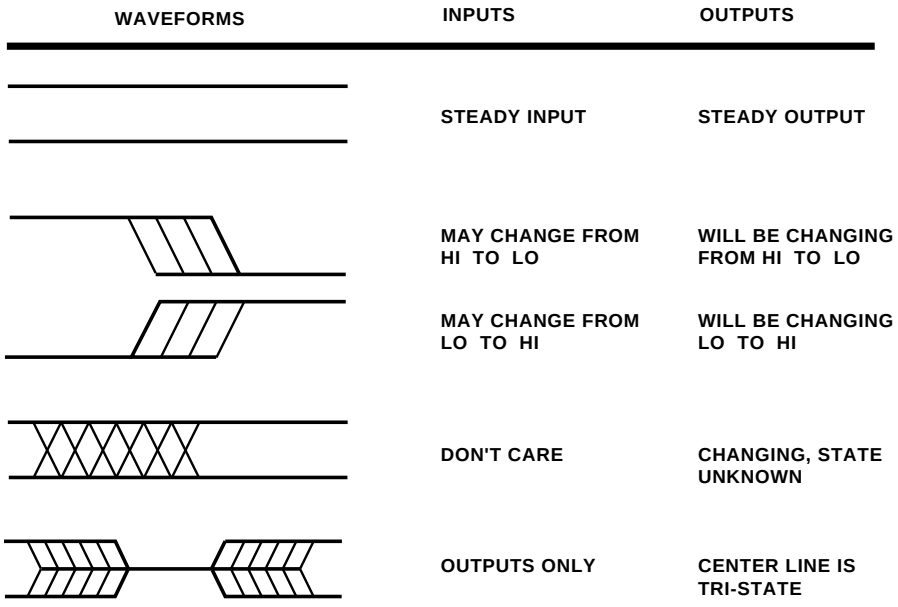


Figure 43. Key to Switching Waveforms



Pin Capacitance

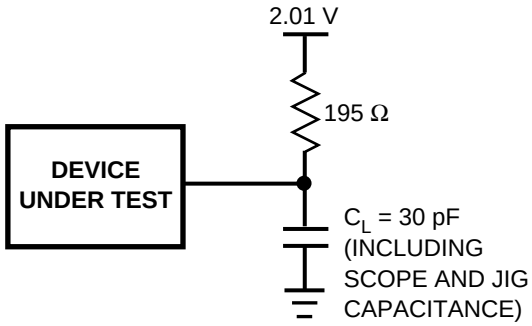
T_A = 25 °C, f = 1 MHz

Symbol	Parameter[1]	Conditions	Typical[2]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 1. These parameters are only sampled and are not 100% tested.
2. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 44. AC Testing Input/Output Waveform

Figure 45. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the window packaged device to an ultra-violet light source. A dosage of 30 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 40 to 45 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure. OTP products are programmed once and cannot be erased.

The ZPSD6XX(V) and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the ZPSD6XX(V) device has all bits in the PAD and EPROM in the “1” or high state. The configuration bits are in the “0” or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.

ZPSD6XX(V) Pin Assignments

Pin No.	Pin Assignments	Pin No.	Pin Assignments
52-Pin PLDCC/ CLDCC	52-Pin PLDCC/CLDCC	52-Pin PLDCC/ CLDCC	52-Pin PLDCC/CLDCC
1	GND	27	PA2
2	PB5	28	PA1
3	PB4	29	PA0
4	PB3	30	AD0
5	PB2	31	AD1
6	PB1	32	AD2
7	PB0	33	AD3
8	PD2	34	AD4
9	PD1	35	AD5
10	PD0	36	AD6
11	PC7	37	AD7
12	PC6	38	V_{CC}
13	PC5	39	AD8
14	PC4	40	AD9
15	V_{CC}	41	AD10
16	GND	42	AD11
17	PC3	43	AD12
18	PC2 (VSTBY)	44	AD13
19	PC1	45	AD14
20	PC0	46	AD15
21	PA7	47	CNTL0
22	PA6	48	$\overline{\text{RESET}}$
23	PA5	49	CNTL2
24	PA4	50	CNTL1
25	PA3	51	PB7
26	GND	52	PB6

ZPSD6XX(V) Package Information

Figure 46. Drawing J7 – 52-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

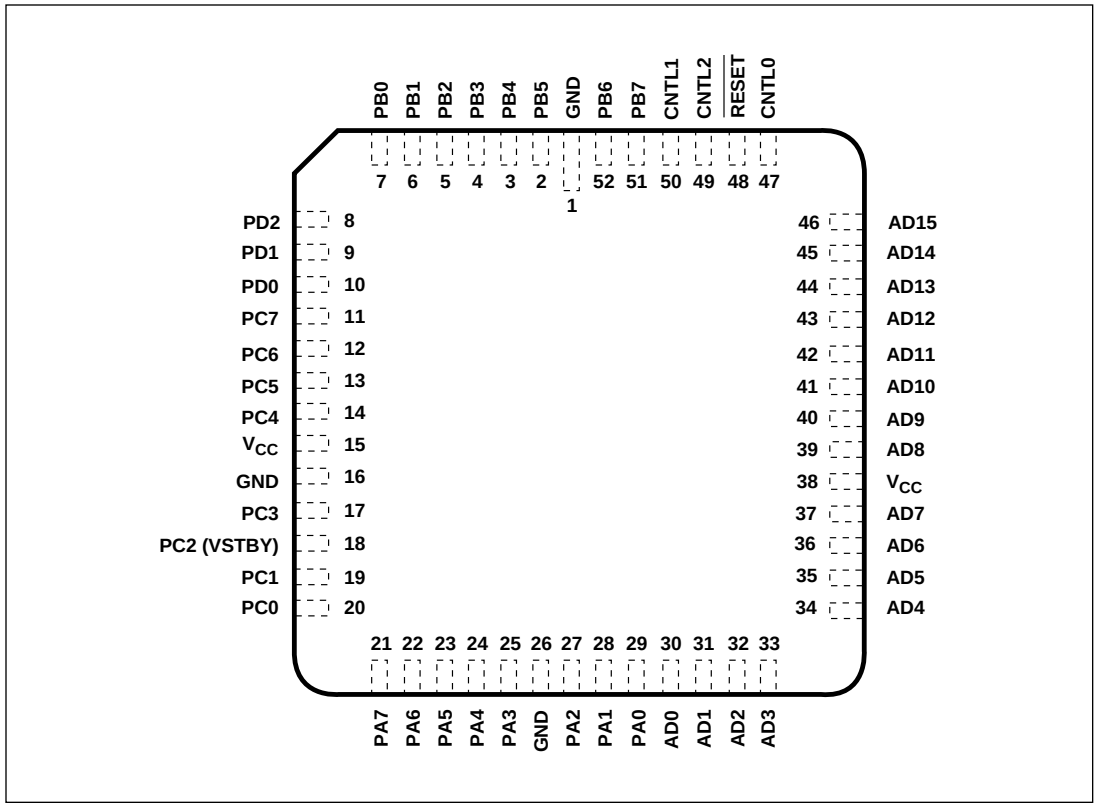
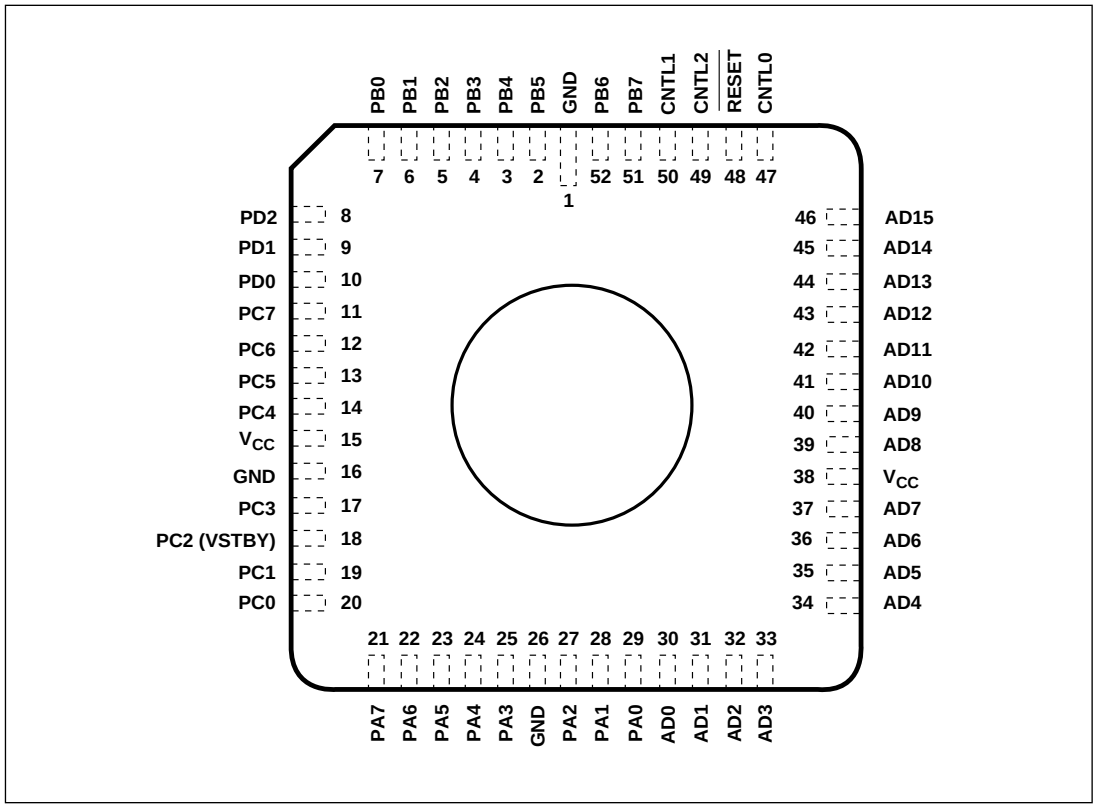


Figure 47 Drawing L6 – 52-Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)



ZPSD6XX(V) Product Errata

Errata specifications for product shipping in 1997 are listed below. Product fully meeting specification (no errata parameters) is scheduled to ship in Q1, 1998. Contact your WSI representative or check our web page at www.wsipsd.com for updated information.

5.0V ± 10% Only

ZPSD6XX-70	Specification	Errata Value	Unit
t_{AVLX}	5	7	nsec
t_{LXAX}	7	8	nsec
t_{RLQV}	20	24	nsec
t_{WLMV}	25	30	nsec
$t_{WLQV\ (PA)}$	25	32	nsec
$t_{WLQZ\ (PA)}$	20	26	nsec
t_{WHAX}	0	18	nsec
t_{ARP}	26	40	nsec
t_{HA}	8	14	nsec
t_{LVDV}	100	180	nsec
ZPSD6XX-90			
t_{AVLX}	6	7	nsec
$t_{WLQV\ (PA)}$	27	32	nsec
$t_{WLQZ\ (PA)}$	25	26	nsec
t_{WHAX}	0	18	nsec
t_{ARP}	29	40	nsec
t_{HA}	8	14	nsec
t_{LVDV}	120	180	nsec
ZPSD6XX-15			
t_{WHAX}	0	18	nsec
t_{ARP}	31	40	nsec
t_{HA}	8	14	nsec
t_{LVDV}	140	180	nsec

3.0V ± 10% Only (Operating Voltage Errata 3.0 V to 5.5 V)

ZPSD6XXV-20		Specification	Errata Value	Unit
t_{ARP}		55	60	nsec
t_{ARPW}		35	45	nsec
t_{CHA}		13	30	nsec
t_{HA}		13	30	nsec
t_{LVDV}		170	150	nsec
t_{RLQV}	(Normal)	50	65	nsec
	(8031)	57	65	nsec

Product Revisions

Product Revisions	Revision Reason	Data Sheet Changes
Original ZPSD6XX(V)	Initial release	–