LSP6501

1.6A, 1.3MHz, Boost DC-DC Converter With Internal Switch

GENERAL DESCRIPTION

The LSP6501 is a current mode step up converter that can carry out 1.6A. LSP6501 also builds up a internal switch with 0.23Ω to provide a high efficient regulator with fast response. The LSP6501 can be operated at 640KHz or 1.3MHz allowing for small filter solution and low noise. An external compensation pin gives the user flexibility in setting up loop compensation, which allows to use a low- ESR ceramic output capacitors. Internal Soft-start function results in small inrush current and the sofe-start can be programmed with an external capacitor.

The LSP6501 device includes under-voltage lockout, and current limiting protection preventing damage in the event of an output overload. A low profile 8-pin MSOP packages is available in the LSP6501.

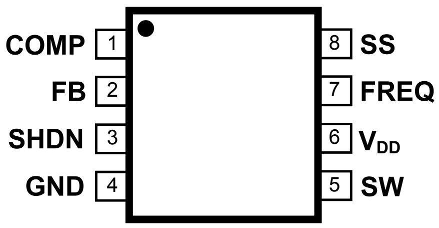
FEATURES

1. **1.6A, 0.23Ω, Internal Switch**
2. **Input Range: +2.6V to +5.5V**
3. **Low Shutdown Current: 0.1uA**
4. **Adjustable Frequency: 640kHz or 1.3MHz**
5. **Small 8-Pin MSOP Package**

TYPICAL APPLICATIONS

- **TFT-LCD Power Management**
- **Portable DVD Player Power Management**

PIN ASSIGNMENT

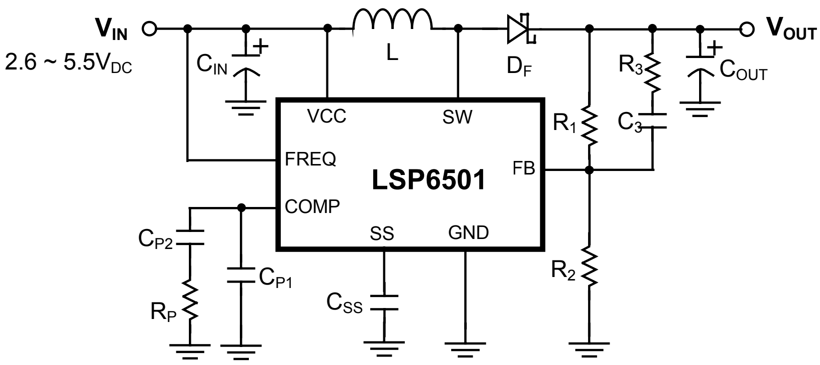


MSOP-8
(Top View)

PIN DESCRIPTION

Pin	Name	Function
1	COMP	Compensation Pin for Error Amplifier
2	FB	Feedback Pin with a Typical Reference Voltage of 1.24V, $V_{OUT} = 1.24 \times (1+ R1/R2)$.
3	SHDN	Shutdown Control Pin. When SHDN is Low, the LSP6501 Will Turn Off
4	GND	Ground
5	SW	Switch Pin
6	V_{DD}	Power Supply Pin
7	FREQ	Frequency Select Pin. Oscillator Frequency to 640kHz When FREQ is Low, and 1.3MHz When FREQ is High
8	SS	Soft-Start Control Pin.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Parameters	Value	Unit
SW to GND	18	V
Input Voltage: SHDN / V_{DD} / FREQ to GND	6	V
SS to GND	-0.3 ~ V_{DD} + 0.3	V
SW pin maximum current	2.3	A
Operating temperature	-20 ~ +85	°C
Maximum Operating Junction Temperature, T_J	150°	°C
Storage Temperature Range	-45 to 125	°C
Lead Temperature (Soldering, 10 seconds)	260	°C
Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.		

THERMAL IMPEDIENCE

Thermal Resistance from Junction to Ambient, θ_{JA}	152°C /W

ELECTRICAL CHARACTERISTICS

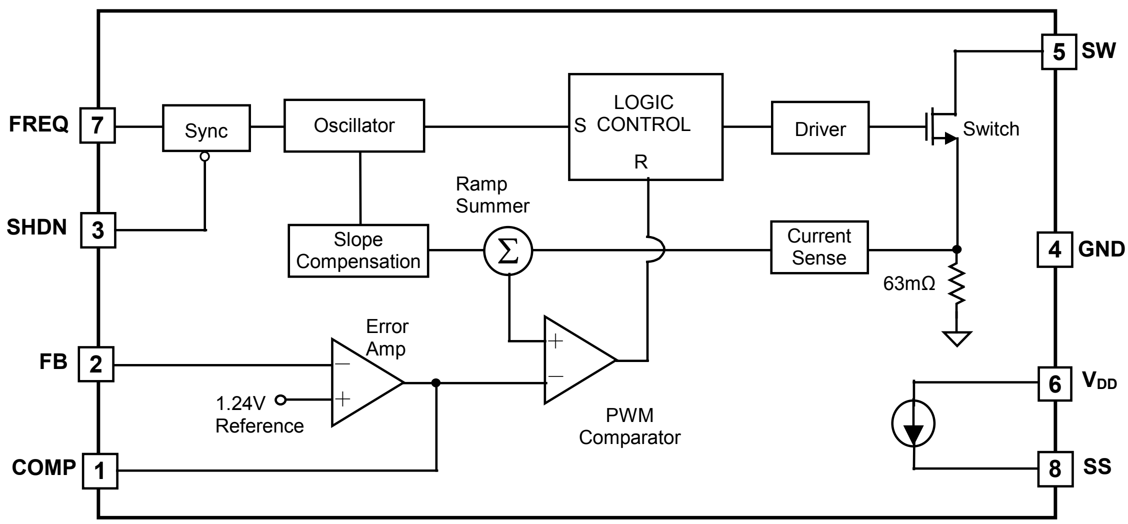
(V_{DD}=$\overline{SHDN}$=3V, FREQ=GND; T_A=25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{DD}		2.6		5.5	V
V_{DD} Under voltage Lockout	UVLO	When V_{DD} is rising, typical hysteresis is 40mV; SW remains off below this level	2.25	2.38	2.52	V
Quiescent Current	I_{DD}	V_{FB}=1.3V, Not switching V_{FB}=1.0V, switching		0.21 1.2	0.35 5.0	mA mA

Shutdown Current	I_{SC}	$\overline{SHDN}$ = GND		0.1	10	uA
FB Reference Voltage	V_{FB}		1.228	1.24	1.252	V
FB Input Current	I_{bias}	$V_{FB}=V_{REF}$		1	40	nA
FB Voltage Line Regulation		COMP=FB, 2.6V $<V_{DD}<$ 5.5V	-	0.1	0.15	%/V
Error Amp Transconductance*	Gm	$I_{COMP}=\pm5uA$	70	105	240	uA/V
Error Amp Gain*	A_V		-	1500	-	V/V
Oscillated Frequency	Fosc	FREQ=GND	540	640	740	kHz
		FREQ=V_{DD}	1100	1320	1600	
Maximum Duty Cycle	D_{MAX}	FREQ=GND	79	85	92	%
		FREQ=V_{DD}		85		
Current Limit	I_{LIM}	V_{DD}=1V, D=0.65	1.2	1.6	2.3	A
ON-Resistance	R_{ON}	Isw=1.2A		0.23	0.5	Ω
Leakage Current	I_{SWOFF}	V_{SW}=12V		0.01	20	uA
Reset Switch Resistance					300	Ω
Soft Start Charge current	Iss	Vss=1.2V	1.5	4	7	uA
Input Low Voltage	V_{IL}	$\overline{SHDN}$, FREQ; V_{DD}=2.6V to 5.5V.			0.3V_{DD}	V
Input High Voltage	V_{IH}	$\overline{SHDN}$, FREQ; V_{DD}=2.6V to 5.5V.	0.7V_{DD}			V
Hysteresis		$\overline{SHDN}$, FREQ;		0.1V_{DD}		V
FREQ Pull-Down Current	I_{FREQ}		1.8	5.0	9.0	uA
SHDN Input Current	$I_{shutdown}$			0.001	1	uA

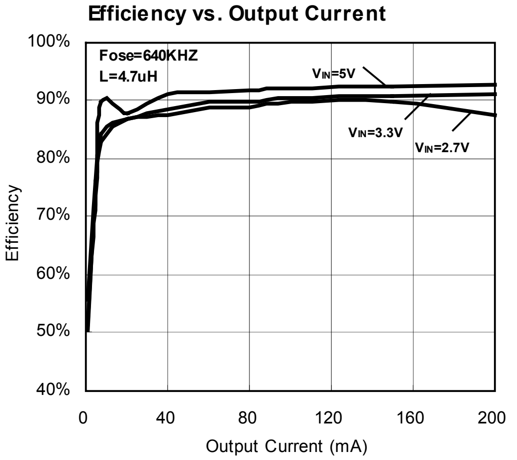
*: Guaranteed by design, not 100% tested in production.

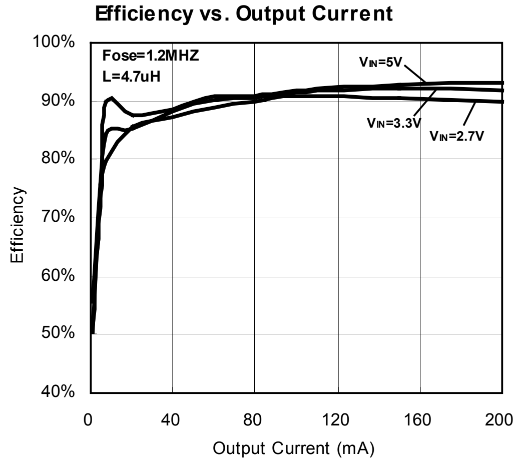
FUNCTIONAL BLOCK DIAGRAM

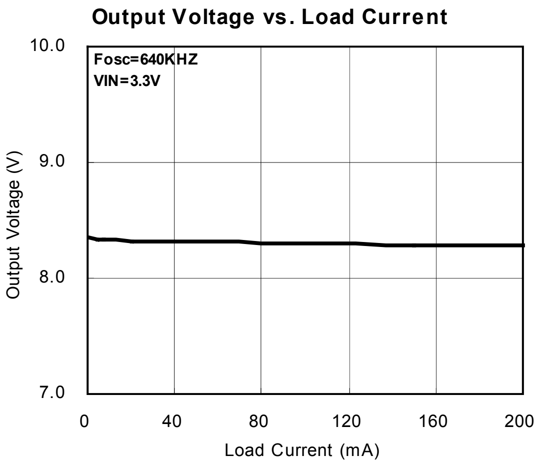


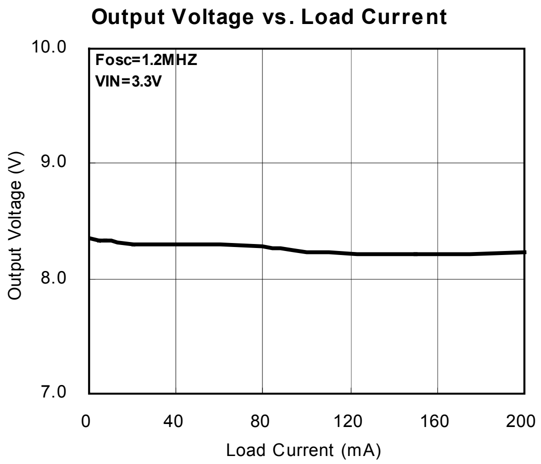
TYPICAL CHARACTERISTICS

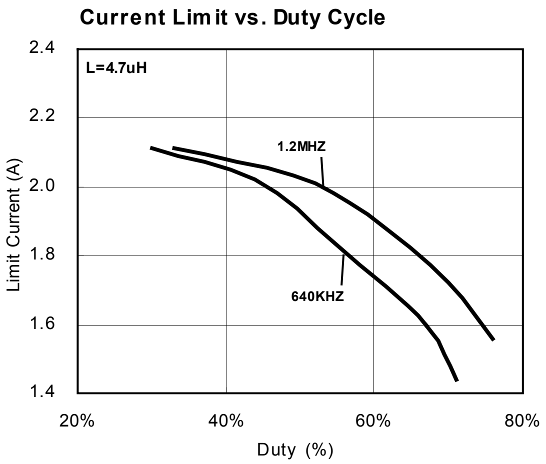
Unless otherwise specified, T_A = 25°C.

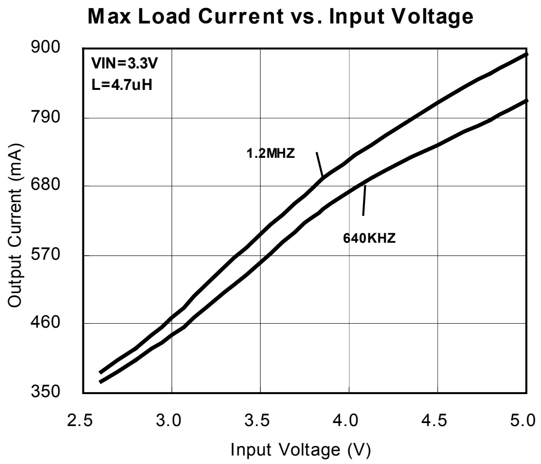




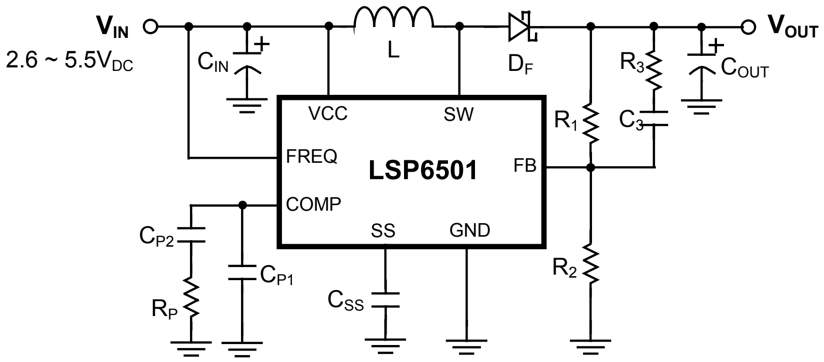








FUNCTION DESCRIPTION



C.R NO	Q'TY	Value	Description	Package
IC	1	-	LSP6501	MSOP-8
D_F	1	-	Schottky Diode 40V/2A	SMA
C_{IN}	1	10uF / 10V	CAP CER SMD	SMD 1206
C_{OUT}	2	10uF / 25V	CAP CER SMD	SMD 1206
L	1	4.7uH	1.0A NR4018-100M	SMD
R_1	1	*NOTE 1	Chip Resistor / 1%	SMD 0603
R_2	1	12K	Chip Resistor / 1%	SMD 0603
R_P	1	10K	Chip Resistor / 1%	SMD 0603
(R_3) *NOTE 2	1	(Optional)	Chip Resistor / 1%	SMD 0603
(C_3) *NOTE 2	1	(Optional)	CAP CER X7R	SMD 0603
(C_{P1})	1	(Optional)	CAP CER X7R	SMD 0603
C_{P2}	1	10nF	CAP CER X7R	SMD 0603
C_{SS}	1	1uF	CAP CER X7R	SMD 0603

*NOTE 1: $V_{OUT}=V_{FB}(1+R_1/R_2)$

*NOTE 2: R_3 & C_3 & C_{P1} are used for improving the transient performance. Because the components are not ideal, sometimes the system needs R_3 & C_3 & C_{P1} to get better transient. The value is determined according to real load conditions.

1. Setting the Output Voltage

FB pin is used to set the output voltage V_{OUT} of the LSP6501. By using the resistor divider, R_1 and R_2, to divide V_{OUT} to the FB pin as feedback signal, the output voltage is determined by:

$$V_{FB} = V_{OUT} \cdot \frac{R_2}{R_1 + R_2}$$

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R_1}{R_2}\right) = 1.24V \cdot \left(1 + \frac{R_1}{R_2}\right)$$

Where, the feedback pin voltage, V_{FB}, is fixed at 1.24V.

2. Selection of Output Capacitor

It is recommended to select output capacitors that the capacitance is high enough and the ESR (Effective Series Resistance) is low enough. These (high capacitance & low ESR) are very important for the Boost Converter to be able to meet the V_{OUT} ripple and load transient specifications.

Ceramic capacitors often have low ESR and can meet the Boost Converter requirements as long as the capacitance values are enough. Note that the capacitance values of all kinds of ceramic capacitor drop when there are DC voltages bias on them. The higher the DC bias, the lower the effective capacitance. The Zxx series capacitors (ex: Z5U) often drop more capacitance than what Yxx series capacitors (ex: Y5V) will drop. And Yxx series are usually worse than Xxx series (ex: X5R). Therefore, it is better to use X5R/X7R type of ceramic capacitors and don't use Yxx series (ex: Y5V) or Zxx series (ex: Z5U) types of capacitor. Although they could be cheaper than X5R or X7R, Yxx series and Zxx series' permanence is not as good as X5R/X7R and is easier to have problems like audio noise problem.

The lifetime of a ceramic capacitor is shorter if the DC-bias is close to its maximum DC rating. For example, to a V_{OUT}=12V application, a $25V_{DC}$ capacitor should have a longer lifetime than a $16V_{DC}$ capacitor does, even when other characteristics of these two capacitors are similar.

Electrolytic capacitors have higher ESR than what ceramic capacitors do. If electrolytic capacitors are used as output capacitors, the ESR should be low enough to meet the V_{OUT} ripple voltage requirement:

$$ESR << \frac{V_{OUT}\ Ripple\,(Peak\ to\ Peak\ Voltage)}{I_{OUT}\ Ripple}$$

For example, if the V_{OUT} ripple voltage of a 5V output DC/DC converter should be smaller than $250mV_{Peak\text{-}to\text{-}Peak}$ and if the ripple current is 0.5A, an capacitor whose ESR is << (0.25V/0.5A)   500mΩ should be chosen. A 680uF of ESR<500 mΩ capacitor can be used in this case.

Note that the ESR of electrolytic capacitor is highly dependent on the temperature - the lower the temperature the higher the ESR and vice versa. This temperature dependence causes V_{OUT} ripple problem and system stability problem sometimes. It may need to use tantalum capacitors or other capacitors that the ESR are temperature independent for applications that temperature ranges are wide.

It is important to ensure the ripple current rating of the output capacitor is enough or the capacitor might burn out during operation. To most electrolytic capacitors, the body temperatures should not be higher than environment temperature plus 10°C. If the body temperature of the capacitor is too high, the ripple current could be higher than the rating of the capacitor. For example, if the air temperature that close to the input capacitor is 45°C, it is better that the body temperature is << (45°C + 10°C) = 55°C.

3. Selection of Input Capacitor

It is recommended to put a ceramic capacitor(s) of several uF to 10uF as input capacitor of the Boost Converter. The capacitor(s) is better to be X7R/X5R type.

4. Selection of Inductor

It is recommended to use ferrite core as the chock material. Don't use iron powder core because the core loss will be too high for applications that the operation frequency is larger than 300KHz, although the cost of an iron powder core could be cheaper. The DC-R of the chock wire should be as low as possible to reduce the power loss.

Below is an equation about the inductor value:

$$L = \left(\frac{V_{IN,MIN}}{V_{OUT}}\right)^2 \cdot \left(\frac{V_{OUT} - V_{IN,MIN}}{I_{OUT,MAX} \cdot f_{SW}}\right) \cdot (3 \cdot \eta)$$

Where,

$L : Inductor\ \ Value\ (H)$

$V_{IN,MIN}\ : Minimum\ Input\ Voltage\ (V)$

$V_{OUT}\ : Typical\ Output\ Voltage\ (V)$

$I_{OUT,MAX}\ : Maximum\ Output\ Current\ (A)$

$f_{SW}\ : Switching\ \ Frequency\ (Hz)$

$\eta : Typical\ \ Efficiency$

Using a higher value inductor can reduce the power loss of the Boost converter. Anyway, a higher value inductor often is bigger in size or has higher DC-R, and the higher DC-R may increase the inductor power loss. Shielding inductor has better EMI performance but the DC-R is often higher than non-shielding inductors of the same size.

It is recommended to adopt an inductor value that the DC/DC converter will not transfer from

Discontinue-Current-Mode (DCM) to Continue-Current-Mode (CCM) or vise versa when V_{IN} or I_{OUT} change. Such mode changing will cause the duty cycle of the Boost DC/DC converter becomes unstable.

5. Selection of Flywheel Diode

An Schottky diode that the voltage rating larger than 20V and the current rating larger than I_{OUT} is recommended. Adopt a Schottky diode of lower dropout voltage can improve the system efficiency. Please also check the leakage current specification of the Schottky diode at the same time.

Note that the maximum working temperatures of many Schottky diodes are only 120 ° C. Please double check the working temperature of the Schottky diode to ensure it is within the specification.

6. Minimum & Maximum Duty Cycle Limitation

PWM ICs often have trouble to convert a V_{OUT} from a V_{IN} if the duty cycle is too small (close to 0%) or too big (close to 100%). Small duty cycle happens when V_{OUT}/V_{IN} is low and big duty cycle happens when V_{OUT}/V_{IN} is High. DC/DC converter designers need to carefully examine whether the DC/DC converter under design has such duty cycle limit problem, especially when the nominal V_{OUT}/V_{IN} is already <1.2 or >5.

Note that factors like V_{IN} deviation, component value deviation, temperature change, switching frequency deviation…etc, can push the duty cycle to be much higher/lower than what we expect from the nominal V_{OUT}/V_{IN} values. For example, the duty of a 3.3V input, 12V output DC/DC converter seems to be around 72.5%, but the actual duty cycle could be up to 80% if we include the voltage drops of output Schottky, V_{IN} trace drop, V_{IN} ripple voltage drop, inductor line drop …etc.

LAYOUT GUIDE LINE

PCB layout is an important stage for power circuit, especially the switching type DC/DC converter that providing high current/voltage and using high switching frequency. If PCB layout is not carefully done, the Boost converter may be unstable or cause serious EMI problems.

Use wide, short, and straightforward traces for high current paths. About the input capacitors, two or more ceramic capacitors of several uF or bigger are recommended to be used. Place one of them very close to the V_{IN} pin of IC and ground, and at least one another very close to the inductor.

It is very important to keep the loop of the SW pin, Schottky diode, output capacitor, and the GND pin of LSP6501 as small as possible, and also minimize the length of the traces between these components, as shown in the following Fig. 1. This is because the *di/dt* at these traces is very high and according to the formula of

$$v = L \cdot \frac{di}{dt}$$

the related voltage spikes will be very high if the trace inductance is high. Such voltage spikes not just cause EMC problems, but may interfere or even damage the IC sometimes.

The most important is, it is better NOT to use via holes in the loop described above, because via holes have high inductance.

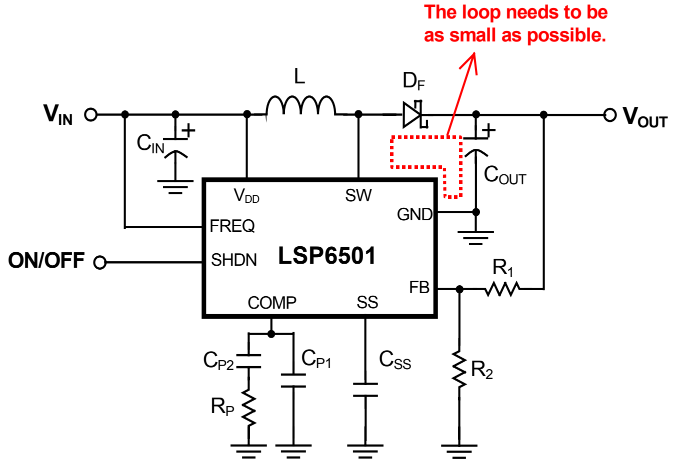


Fig. 1

Second, keep all the analog components and signal traces, for example the V_{OUT} sense trace, far away from the noisy areas, that is, the areas near inductor, LSP6501 switch pin, and Schottky diode. If the V_{OUT} sense trace is close to the noisy area, large noise may be coupled into FB pin and cause V_{OUT} value not accurate or unstable. Please refer to Fig. 2.

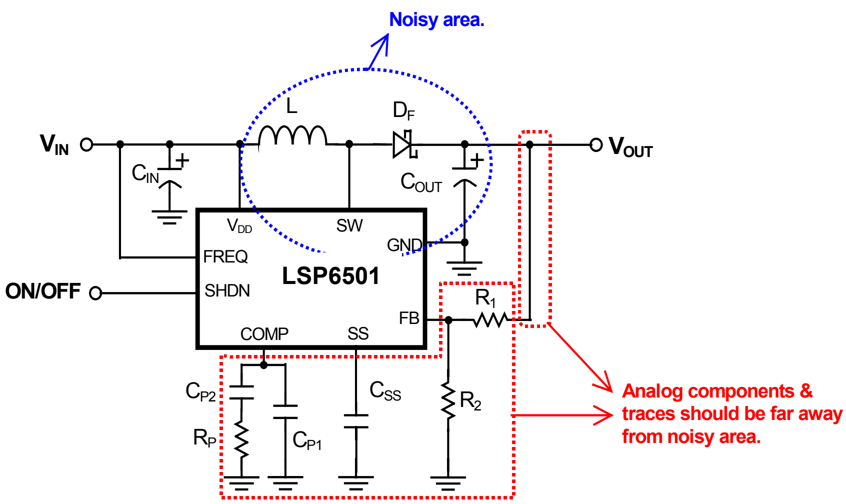


Fig. 2

About analog ground (the ground for feedback resistors, soft start capacitor, V_{OUT} sensing resisters, and compensation components), it is recommended to use short traces to connect these ground points and then directly connect these traces to the GND pin of the IC. Please refer to Fig. 3 & Fig. 4.

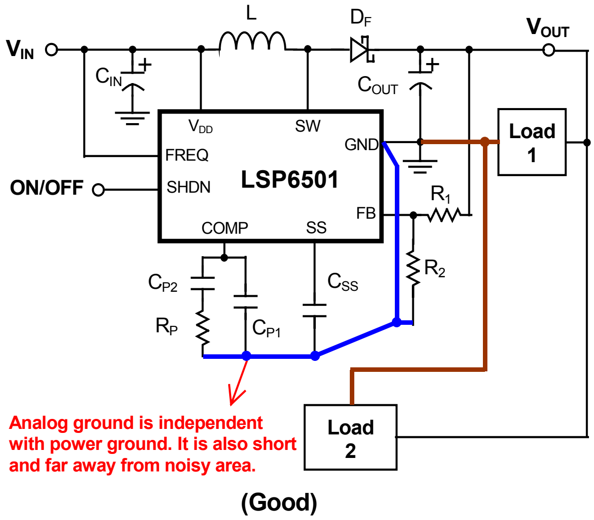


Fig. 3

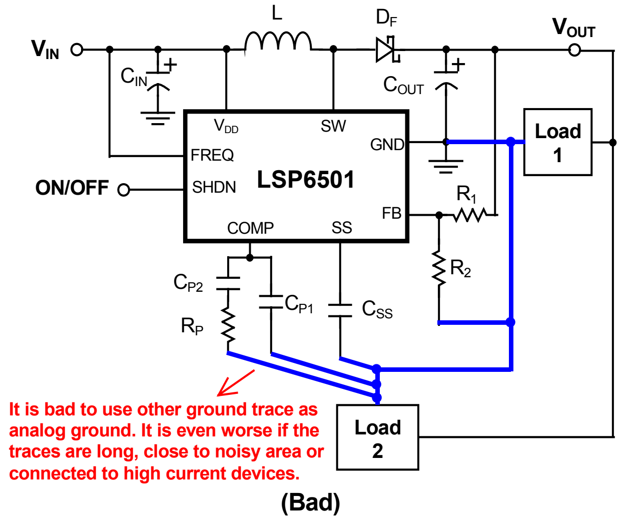


Fig. 4

A big ground plane (form input to out put) can help almost all the performance of the chip. Beside the ground trace on the top layer, please use another layer as the ground layer.

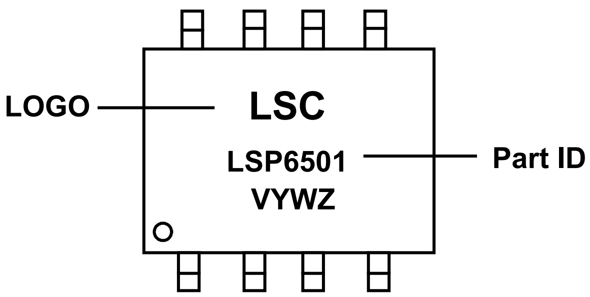
ORDERING INFORMATION

LSP6501X X X X

Package:	Output Voltage:	Packing:	Temperature Grade:
MS: MSOP8L	Blank: Adj	A: Tape & Real	C: -20～85℃

MARKING INFORMATION

MSOP-8



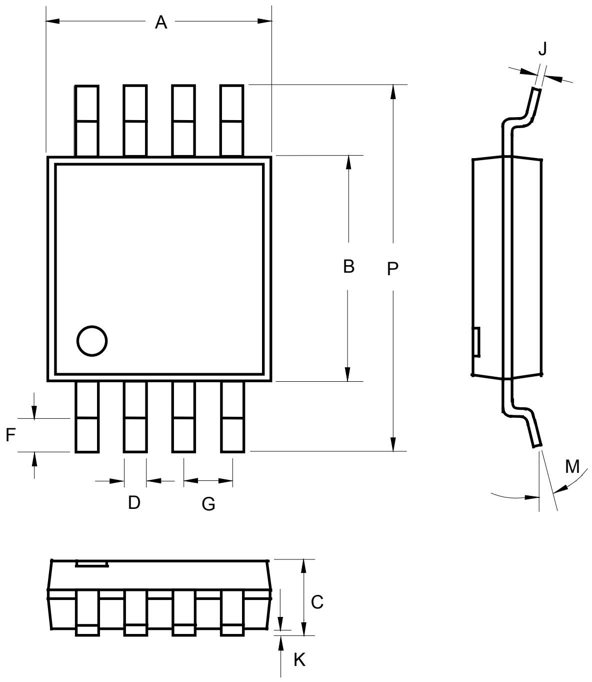
V YW Z

- Z: Internal Code
- YW: Date Code
  - Y : Year(09=2009,10=2010,11=2011,12=2012...)
  - W : Week

Week	1	2	3	4	5	6	7	8	9	10	11	12	13
Code#	1	2	3	4	5	6	7	8	9	A	B	C	D
Week	14	15	16	17	18	19	20	21	22	23	24	25	26
Code#	E	F	G	H	J	K	L	M	N	P	Q	R	S
Week	27	28	29	30	31	32	33	34	35	36	37	38	39
Code#	T	U	V	W	X	Y	Z	a	b	c	d	e	f
Week	40	41	42	43	44	45	46	47	48	49	50	51	52/53
Code#	g	h	l	m	n	p	q	s	t	u	v	w	x

- V: Output Voltage
  - Blank=ADJ

PACKAGE INFORMATION



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.114	0.118	0.122	2.9	3	3.1
B	0.114	0.118	0.122	2.9	3	3.1
C			0.043			1.1
D		0.012			0.3	
F	0.016	0.021	0.031	0.4	0.53	0.8
G		0.026BSC			0.65BSC	
J		0.006			0.15	
K	0	-	0.006	0	-	0.15
M	0º	-	8º	0º	-	8º
P	0.185	0.193	0.201	4.7	4.9	5.1