

Document Title

**64Kx16 Bit High-Speed CMOS Static RAM(3.3V Operating)
Operated at Commercial and Industrial Temperature Ranges.**

Revision History

Rev. No.	History	Draft Data	Remark																			
Rev. 0.0	Initial release with Preliminary.	Aug. 5. 1998	Preliminary																			
Rev. 1.0	Release to Final Data Sheet. 1.1. Delete Preliminary. 1.2. Changed DC characteristics.	Sep. 7. 1998	Final																			
	<table><tr><td colspan="2">Item</td><td>Previous</td><td>Changed</td></tr><tr><td rowspan="3">Icc</td><td>12ns</td><td>85mA</td><td>95mA</td></tr><tr><td>15ns</td><td>83mA</td><td>93mA</td></tr><tr><td>20ns</td><td>80mA</td><td>90mA</td></tr></table>	Item		Previous	Changed	Icc	12ns	85mA	95mA	15ns	83mA	93mA	20ns	80mA	90mA							
Item		Previous	Changed																			
Icc	12ns	85mA	95mA																			
	15ns	83mA	93mA																			
	20ns	80mA	90mA																			
Rev. 2.0	Added 48-fine pitch BGA.	Sep. 17. 1998	Final																			
Rev. 2.1	Changed device part name for FP-BGA.	Nov. 5. 1998	Final																			
	<table><tr><td colspan="2">Item</td><td>Previous</td><td>Changed</td></tr><tr><td colspan="2">Symbol</td><td>Z</td><td>F</td></tr></table> ex) K6R1016V1C-Z -> K6R1016V1C-F	Item		Previous	Changed	Symbol		Z	F													
Item		Previous	Changed																			
Symbol		Z	F																			
Rev. 2.2	Changed device ball name for FP-BGA.	Dec. 10. 1998	Final																			
	<table><tr><td colspan="2">Previous</td><td colspan="2">Changed</td></tr><tr><td colspan="2">I/O1 ~ I/O8</td><td colspan="2">I/O9 ~ I/O16</td></tr><tr><td colspan="2">I/O9 ~ I/O16</td><td colspan="2">I/O1 ~ I/O8</td></tr></table>	Previous		Changed		I/O1 ~ I/O8		I/O9 ~ I/O16		I/O9 ~ I/O16		I/O1 ~ I/O8										
Previous		Changed																				
I/O1 ~ I/O8		I/O9 ~ I/O16																				
I/O9 ~ I/O16		I/O1 ~ I/O8																				
Rev. 3.0	1. Added 10ns speed for FP-BGA only. 2. Changed Standby Current.	Mar. 2. 1999	Final																			
	<table><tr><td colspan="2">Item</td><td>Previous</td><td>Changed</td></tr><tr><td colspan="2">Standby Current(I_{sb1})</td><td>0.3mA</td><td>0.5mA</td></tr></table> 3. Added Data Retention Characteristics.	Item		Previous	Changed	Standby Current(I _{sb1})		0.3mA	0.5mA													
Item		Previous	Changed																			
Standby Current(I _{sb1})		0.3mA	0.5mA																			
Rev. 3.1	Added 10ns speed for all packages(44SOJ / 44TSOP2 / 48FPBGA)	Apr. 24. 2000	Final																			
Rev. 3.2	Supply Voltage Change 1. Only 10ns Bin : 3.15V ~ 3.6V 2. The Rest Bin : 3.0V ~ 3.6V	Aug. 25. 2000	Final																			
Rev. 3.3	V _{IH} /V _{IL} Change	Oct. 2. 2000	Final																			
	<table><tr><td rowspan="2">Item</td><td colspan="2">Previous</td><td colspan="2">Changed</td></tr><tr><td>Min</td><td>Max</td><td>Min</td><td>Max</td></tr><tr><td>V_{IH}</td><td>2.0</td><td>V_{CC}+0.5</td><td>2.0</td><td>V_{CC}+0.3</td></tr><tr><td>V_{IL}</td><td>-0.5</td><td>0.8</td><td>-0.3</td><td>0.8</td></tr></table>	Item	Previous		Changed		Min	Max	Min	Max	V _{IH}	2.0	V _{CC} +0.5	2.0	V _{CC} +0.3	V _{IL}	-0.5	0.8	-0.3	0.8		
Item	Previous		Changed																			
	Min	Max	Min	Max																		
V _{IH}	2.0	V _{CC} +0.5	2.0	V _{CC} +0.3																		
V _{IL}	-0.5	0.8	-0.3	0.8																		
Rev. 4.0	Delete 20ns speed bin	Sep. 24. 2001	Final																			

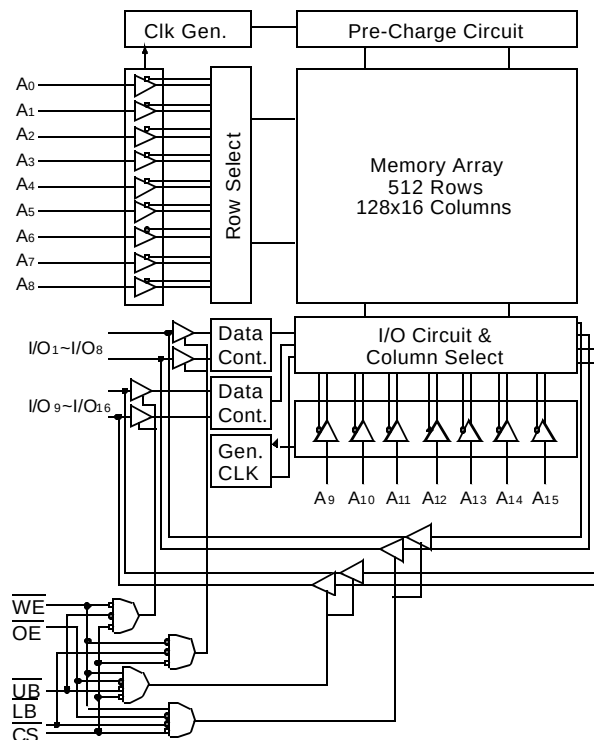
The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

64K x 16 Bit High-Speed CMOS Static RAM(3.3V Operating)**FEATURES**

- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 30mA(Max.)
 - (CMOS) : 5mA(Max.)
 - 0.5mA(Max.) L-ver. only
- Operating *K6R1016V1C-10: 105mA(Max.)
- K6R1016V1C-12: 95mA(Max.)
- K6R1016V1C-15: 93mA(Max.)
- Single 3.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention: L-ver. only
- Center Power/Ground Pin Configuration
- Data Byte Control: $\overline{LB}$: I/O₁~ I/O₈, $\overline{UB}$: I/O₉~ I/O₁₆
- Standard Pin Configuration:
 - K6R1016V1C-J: 44-SOJ-400
 - K6R1016V1C-T: 44-TSOP2-400BF
 - K6R1016V1C-F: 48-Fine pitch BGA with 0.75 Ball pitch

GENERAL DESCRIPTION

The K6R1016V1C is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The K6R1016V1C uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R1016V1C is packaged in a 400mil 44-pin plastic SOJ or TSOP2 forward or 48-Fine pitch BGA.

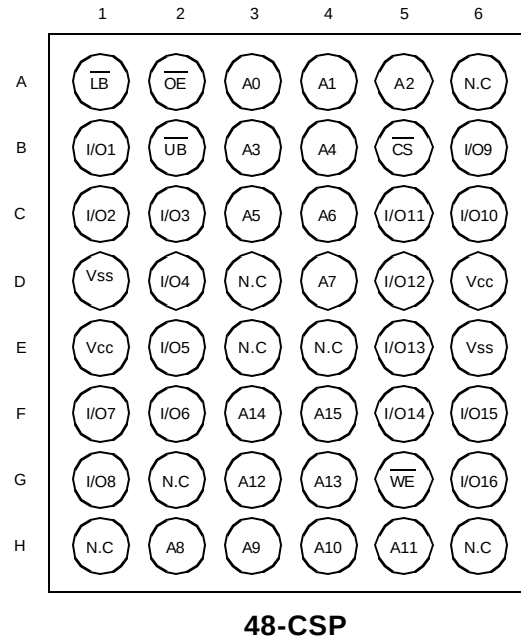
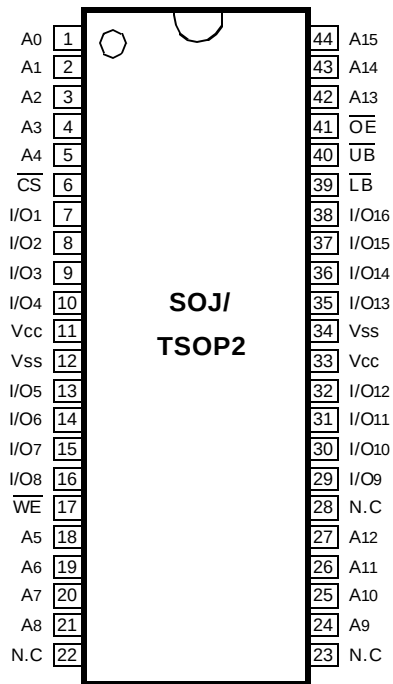
FUNCTIONAL BLOCK DIAGRAM**ORDERING INFORMATION**

K6R1016V1C-C10/C12/C15	Commercial Temp.
K6R1016V1C-I10/I12/I15	Industrial Temp.

PIN FUNCTION

Pin Name	Pin Function
A ₀ - A ₁₅	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O ₁ ~I/O ₈)
$\overline{UB}$	Upper-byte Control(I/O ₉ ~I/O ₁₆)
I/O ₁ ~ I/O ₁₆	Data Inputs/Outputs
V _{CC}	Power(+3.3V)
V _{SS}	Ground
N.C	No Connection

PIN CONFIGURATION (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V _{IN} , V _{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V _{CC}	-0.5 to 4.6	V
Power Dissipation		P _d	1	W
Storage Temperature		T _{STG}	-65 to 150	°C
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC} ⁽¹⁾	3.15	3.3	3.6	V
Supply Voltage	V _{CC} ⁽²⁾	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ⁽³⁾	V
Input Low Voltage	V _{IL}	-0.3 ⁽⁴⁾	-	0.8	V

(1) For K6R1016V1C-10 only.

(2) For all speed grades except K6R1016V1C-10.

(3) V_{IH}(Max) = V_{CC} + 2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA

(4) V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS ($T_A=0$ to 70°C , $V_{CC}=3.3\text{V}+0.3\text{V}/-0.15\text{V}$, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}		-2	2	μA
Output Leakage Current	I _{LO}	CS=V _{IH} or OE=V _{IH} or WE=V _{IL} V _{OUT} =V _{SS} to V _{CC}		-2	2	μA
Operating Current	I _{CC}	Min. Cycle, 100% Duty CS=V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} =0mA	10ns	-	105	mA
			12ns	-	95	
			15ns	-	93	
Standby Current	I _{SB}	Min. Cycle, CS=V _{IH}		-	30	mA
	I _{SB1}	f=0MHz, CS ≥V _{CC} -0.2V, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V	Normal	-	5	mA
			L-Ver.	-	0.5	
Output Low Voltage Level	V _{OL}	I _{OL} =8mA		-	0.4	V
Output High Voltage Level	V _{OH}	I _{OH} =-4mA		2.4	-	V

* The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE* ($T_A=25^\circ\text{C}$, $f=1.0\text{MHz}$)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$	-	8	pF
Input Capacitance	C_{IN}	$V_{IN}=0\text{V}$	-	6	pF

* Capacitance is sampled and not 100% tested.

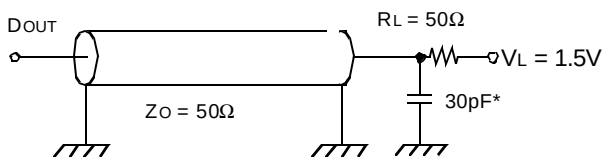
AC CHARACTERISTICS ($T_A=0$ to 70°C , $V_{CC}=3.3\text{V}+0.3\text{V}/-0.15\text{V}$, unless otherwise noted.)

TEST CONDITIONS*

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

* The above test conditions are also applied at industrial temperature range.

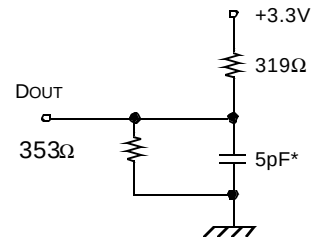
Output Loads(A)



* Capacitive Load consists of all components of the test environment.

Output Loads(B)

for t_{HZ} , t_{LZ} , t_{WHZ} , t_{OW} , t_{OLZ} & t_{OHZ}



* Including Scope and Jig Capacitance

READ CYCLE*

Parameter	Symbol	K6R1016V1C-10		K6R1016V1C-12		K6R1016V1C-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	10	-	12	-	15	-	ns
Address Access Time	t _{AA}	-	10	-	12	-	15	ns
Chip Select to Output	t _{CO}	-	10	-	12	-	15	ns
Output Enable to Valid Output	t _{OE}	-	5	-	6	-	7	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ Access Time	t _{BA}	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	t _{LZ}	3	-	3	-	3	-	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ Enable to Low-Z Output	t _{BLZ}	0	-	0	-	0	-	ns
Output Enable to Low-Z Output	t _{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t _{HZ}	0	5	0	6	-	7	ns
Output Disable to High-Z Output	t _{OHZ}	0	5	0	6	-	7	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ Disable to High-Z Output	t _{BHZ}	0	5	0	6	-	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t _{PU}	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t _{PD}	-	10	-	12	-	15	ns

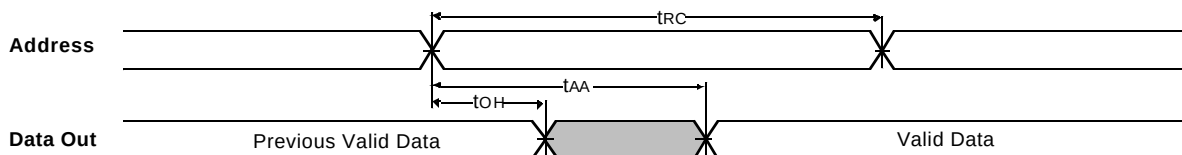
* The above parameters are also guaranteed at industrial temperature range.

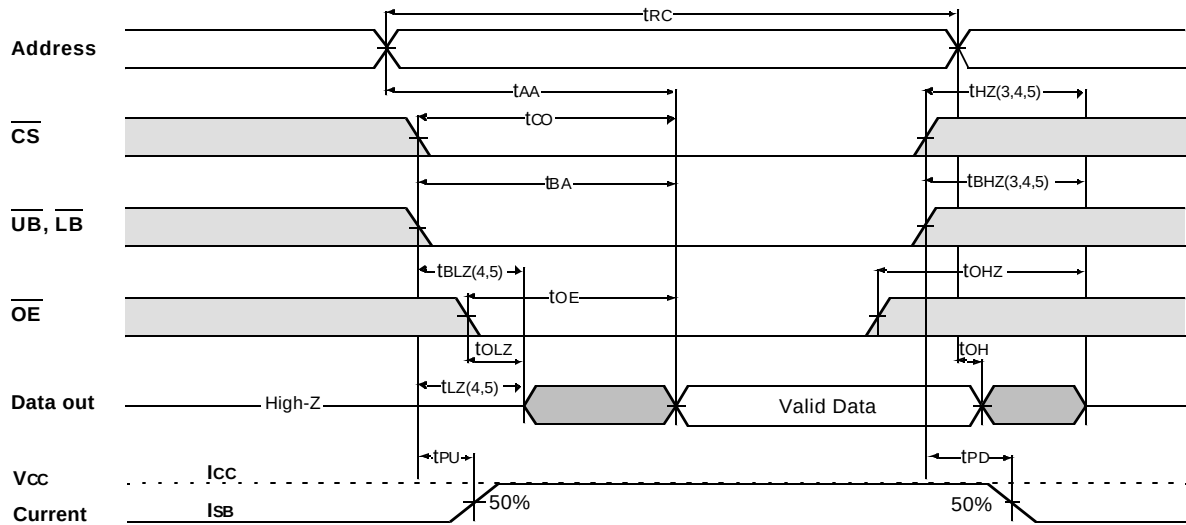
WRITE CYCLE*

Parameter	Symbol	K6R1016V1C-10		K6R1016V1C-12		K6R1016V1C-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	ns
Chip Select to End of Write	t _{CW}	7	-	8	-	9	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t _{AW}	7	-	8	-	9	-	ns
Write Pulse Width($\overline{\text{OE}}$ High)	t _{WP}	7	-	8	-	9	-	ns
Write Pulse Width($\overline{\text{OE}}$ Low)	t _{WP1}	10	-	12	-	15	-	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ Valid to End of Write	t _{BW}	7	-	8	-	9	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	5	0	6	0	7	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	7	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t _{OW}	3	-	3	-	3	-	ns

* The above parameters are also guaranteed at industrial temperature range.

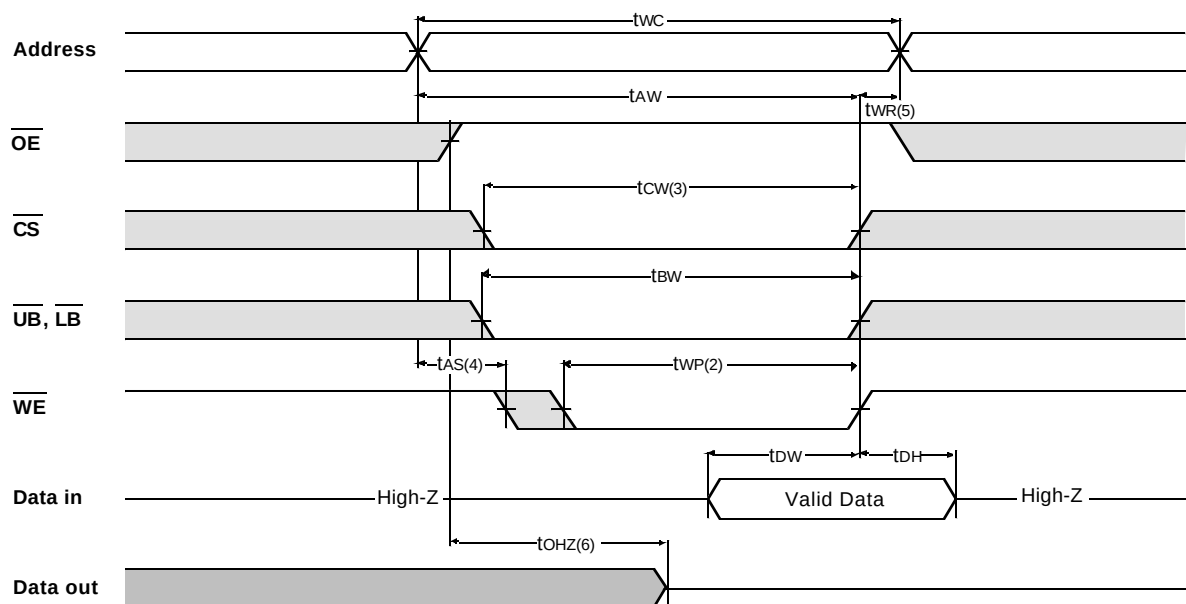
TIMING DIAGRAMS

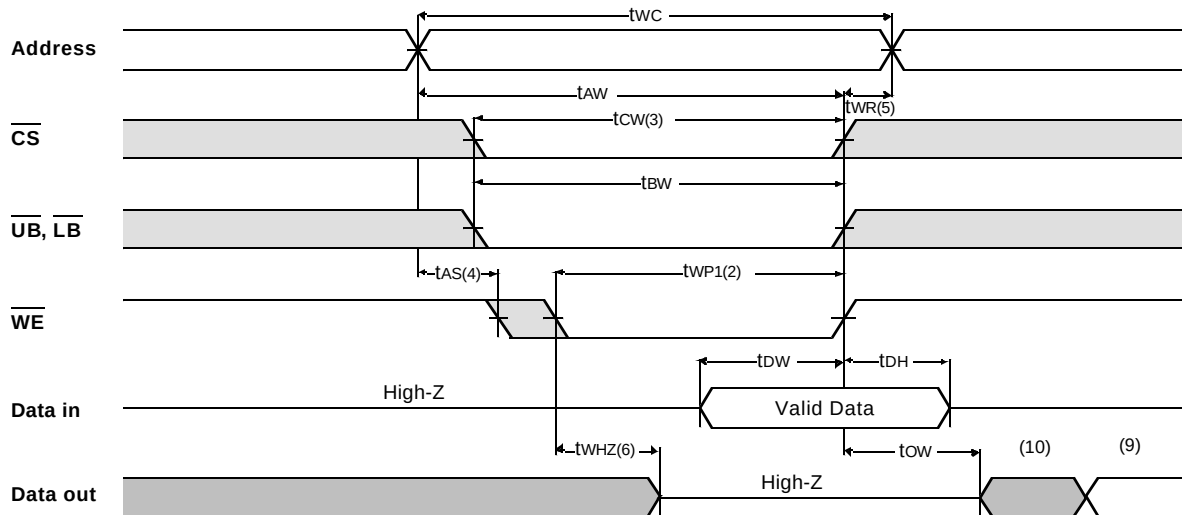
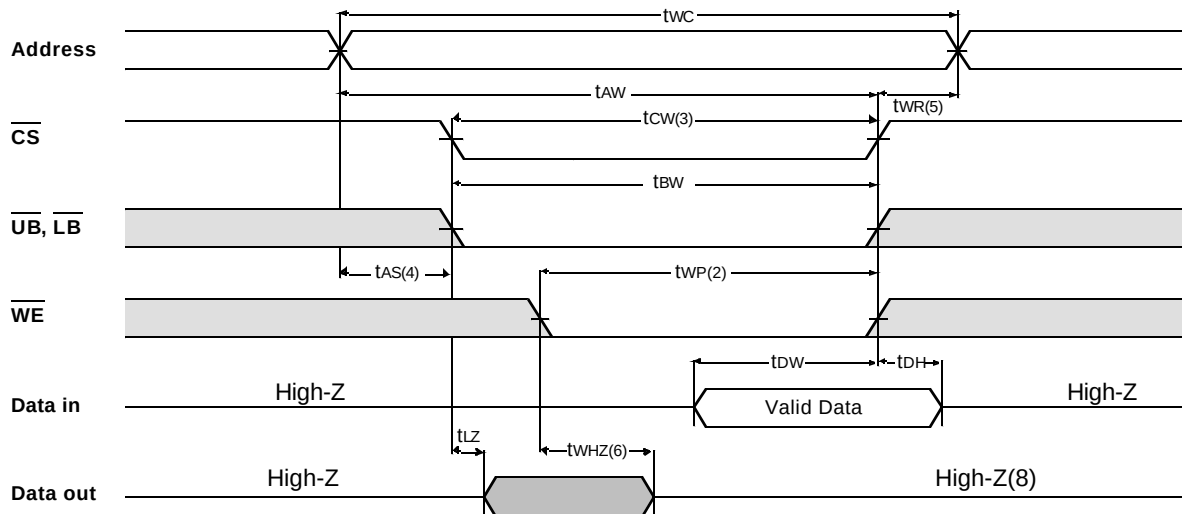
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{\text{CS}}=\overline{\text{OE}}=V_{\text{IL}}$, $\overline{\text{WE}}=V_{\text{H}}$, $\overline{\text{UB}}$, $\overline{\text{LB}}=V_{\text{L}}$)

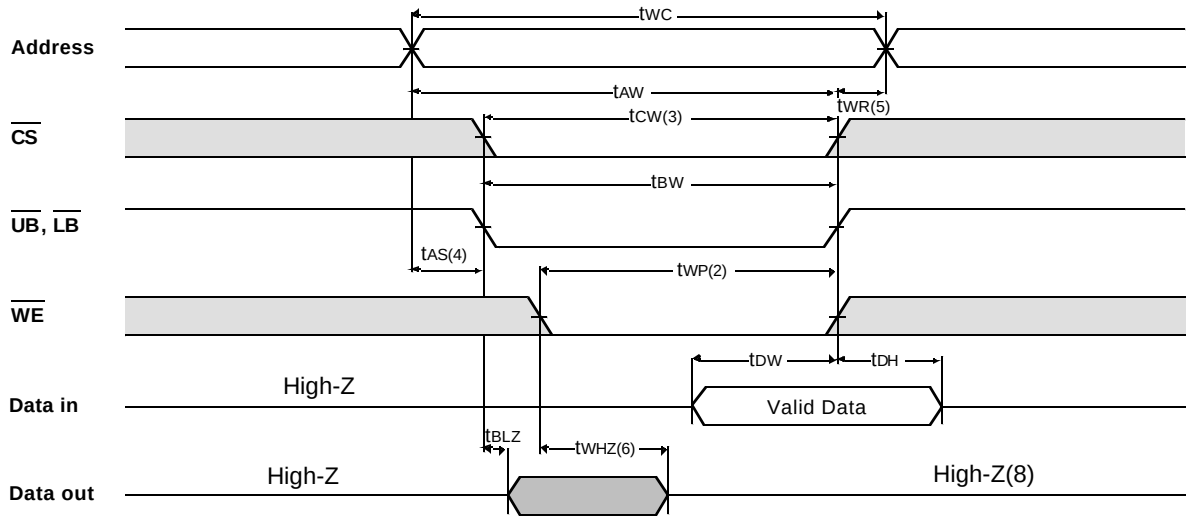
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}=\text{Clock}$)

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ = Low fixed)TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}$ =Controlled)

TIMING WAVEFORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. DOUT is the read data of the new address.
10. When $\overline{CS}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	Icc
L	X	X	H	H	Read	DOUT	High-Z	Icc
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	Icc
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

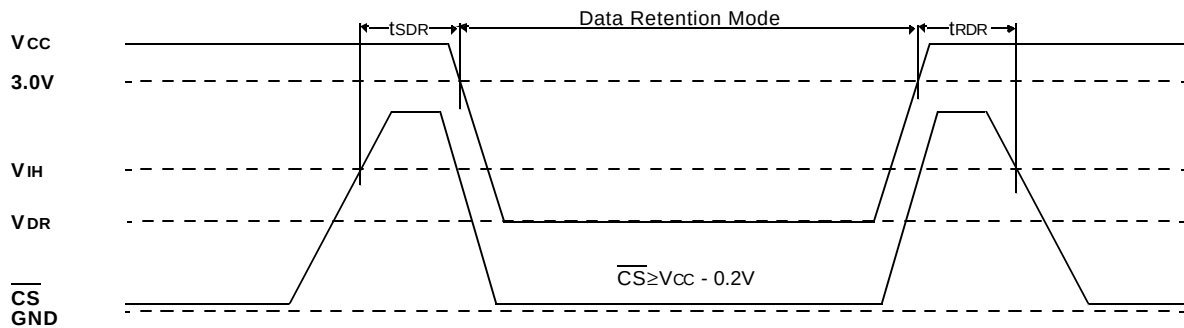
* X means Don't Care.

DATA RETENTION CHARACTERISTICS* (T_A=0 to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V _{CC} for Data Retention	V _{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} =3.0V, $\overline{CS} \geq V_{CC} - 0.2V$ V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	-	-	0.4	mA
		V _{CC} =2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	-	-	0.3	
Data Retention Set-Up Time	t _{SDR}	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	t _{RDR}		5	-	-	ms

* The above parameters are also guaranteed at industrial temperature range.
Data Retention Characteristic is for L-ver only.

DATA RETENTION WAVE FORM

 $\overline{CS}$ controlled

CMOS SRAM

Units:millimeters/Inches

44-TSOP2-400BF

The drawing illustrates the mechanical specifications of a 48-pin LQFP package. The top view shows a square body with pins on all four sides, labeled #1 through #48. Key dimensions include a body width of 18.81 ± 0.10 mm (max 18.81 mm) and a pin pitch of 0.725 ± 0.004 mm. The side view shows a package height of 11.76 ± 0.20 mm and a pin height of 0.463 ± 0.008 mm. A detail view of the pin shows a thickness of 0.25 ± 0.010 mm (typical), a width of $0.45 \sim 0.75$ mm ($0.018 \sim 0.030$ mm), and a lead angle of $0 \sim 8^\circ$. The bottom view shows a pin width of 0.80 ± 0.0315 mm, a pin thickness of 0.05 ± 0.002 mm (min 0.05 mm), and a pin-to-pin spacing of 0.30 ± 0.10 mm (0.012 ± 0.004 mm).

PACKAGE OUTLINE

(Units : millimeter)

