

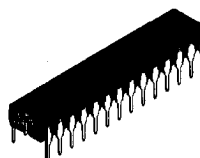
SONY**CXK5971P/M/J** 25/30/35**8192-word × 9-bit High Speed CMOS Static RAM****Description**

CXK5971P/M/J are 73,728 bits high speed CMOS static RAMs organized as 8,192-word by 9-bit and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

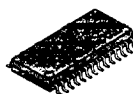
Features

- Fast access time 25ns/30ns/35ns (Max.)
- Low power standby 5 μ W (Typ.)
- Low power operation 150mW (Typ.)
- Single + 5V supply: $5V \pm 10\%$
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output three state output.
- Directly TTL compatible all inputs and outputs.
- Low voltage data retention 2.0V (Min.)
- Full CMOS.
- Available in 28 pin 300mil DIP, 450mil SOP and 300 mil SOJ.

CXK5971P
28 pin DIP (Plastic)



CXK5971M
28 pin SOP (Plastic)



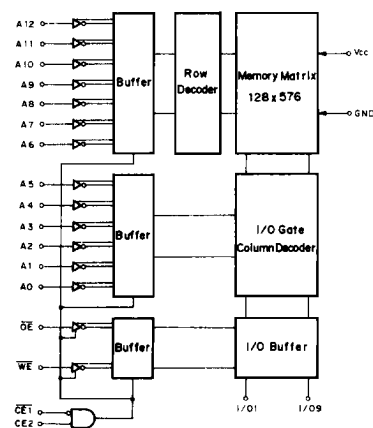
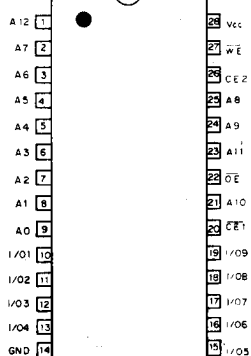
CXK5971J
28 pin SOJ (Plastic)

**Structure**

Silicon gate CMOS IC

Function

8192-word × 9-bit static RAM

Block Diagram**Pin Configuration
(Top View)****Pin Description**

Symbol	Description
A0 to A12	Address input
I/O0 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V Power supply
GND	Ground

Absolute Maximum Ratings

Ta = 25°C, GND = 0V

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 * to + 7.0	V
Input voltage	V _{IN}	- 0.5 * to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5 * to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK5971P/J	1.0
		CXK5971M	0.7
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

*Note) V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O9	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions

Ta = 0 to + 70°C, GND = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3 *	—	0.8	V

*Note) V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

 $V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0$ to $+70^\circ C$

Item	Symbol	Test condition	- 25/30/35			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	$V_{IN} = GND$ to V_{CC}	- 1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O} = GND$ to V_{CC} , $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	- 1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OUT} = 0mA$	—	30	60	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100 %, $I_{OUT} = 0mA$	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	1	100	μA
	I_{SB2}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH}	—	10	25	mA
Output high voltage	V_{OH}	$I_{OH} = -4.0mA$	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0mA$	—	—	0.4	V

* $V_{CC} = 5V$, $T_a = 25^\circ C$

I/O capacitance

 $T_a = 25^\circ C$, $f = 1MHz$

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF

(Note) This parameter is sampled and is not 100 % tested.

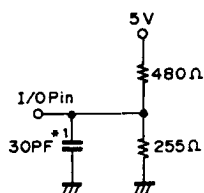
AC characteristics

● AC test conditions

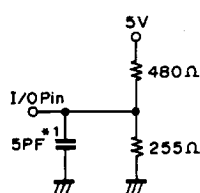
 $V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ C$

Item	Condition
Input pulse high level	$V_{IH} = 3.0V$
Input pulse low level	$V_{IL} = 0V$
Input rise time	$t_r = 5ns$
Input fall time	$t_f = 5ns$
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



* 1. including scope and jig capacitance

* 2. for t_{LZ1} , t_{LZ2} , t_{OLZ} , t_{HZ1} , t_{HZ2} , t_{OHZ} , t_{OW} , t_{WHZ}

Fig. 1

1) Read cycle

Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time (CE1)	t _{CO1}	—	25	—	30	—	35	ns
Chip enable access time (CE2)	t _{CO2}	—	25	—	30	—	35	ns
Output enable to output valid	t _{OE}	—	15	—	15	—	20	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LEZ1} * t _{LEZ2} *	5	—	5	—	5	—	ns
Output enable to output in low Z (OE)	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} * t _{HZ2} *	0	15	0	15	0	20	ns
Chip disable to output in high Z (OE)	t _{OHZ} *	0	13	0	13	0	15	ns
Chip enable to power up time (CE1, CE2)	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time (CE1, CE2)	t _{PD}	—	20	—	20	—	20	ns

2) Write cycle

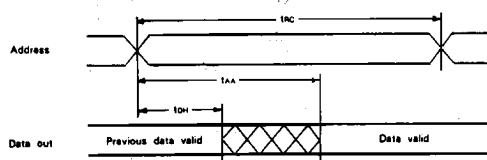
Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	20	—	20	—	30	—	ns
Chip enable to end of write	t _{CW}	20	—	20	—	30	—	ns
Data to write time overlap	t _{DW}	12	—	12	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	20	—	20	—	25	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	13	0	13	0	15	ns

* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

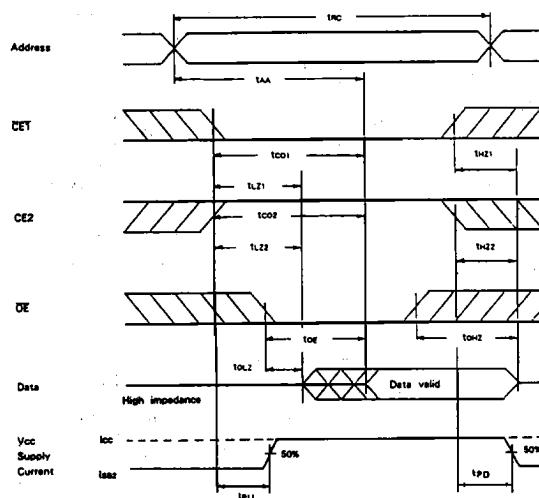
Timing Waveform

1) Read cycle

- Read cycle No. 1 : [$\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$]

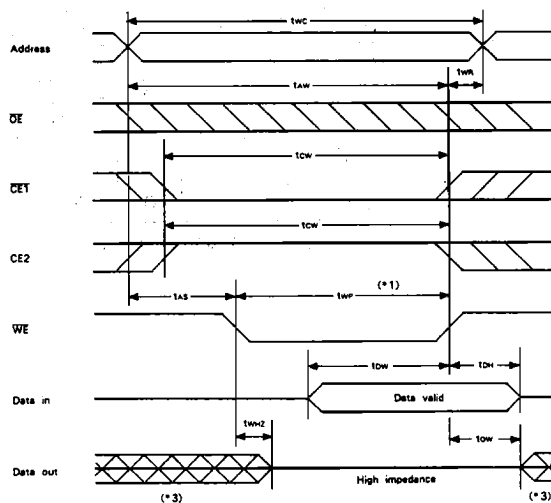


- Read cycle No. 2 : [$\overline{WE} = V_{IH}$]

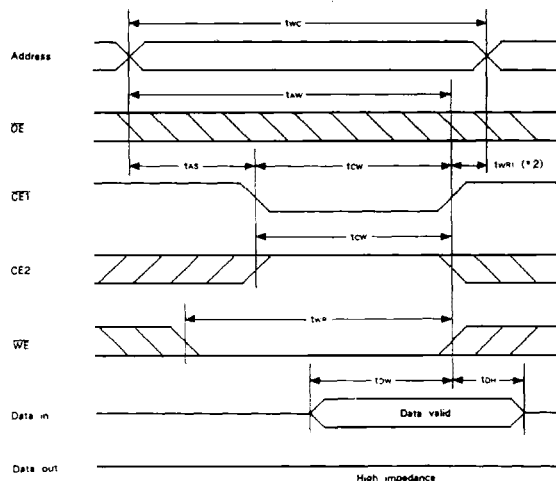


2) Write cycle

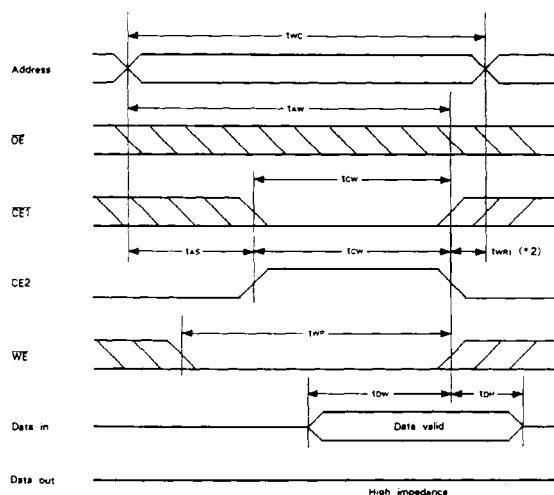
- Write cycle No. 1 : [$\overline{WE}$ control]



• Write cycle No. 2 : [$\overline{CE1}$ control]



• Write cycle No. 3 : [$\overline{CE2}$ control]



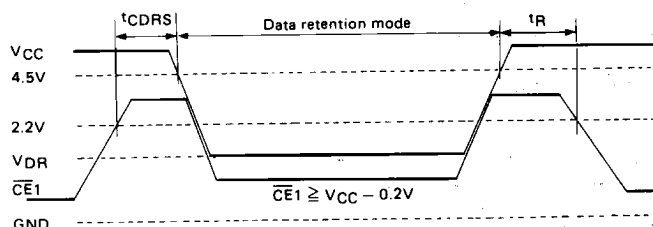
Note)

- *1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.
- *2. t_{wh1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.
- *3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

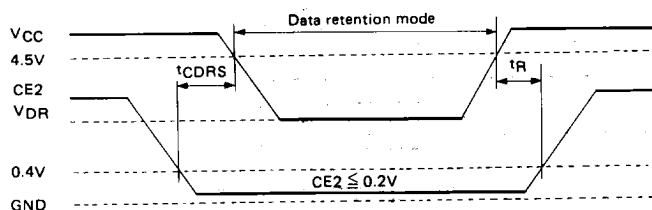
Data Retention Characteristics

Ta = 0 to +70°C

Item	Symbol	Test condition	- 25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1	2.0	5.0	5.5	V
Data retention current	I _{CCDR1}	V _{CC} = 3.0V *1	—	0.5	50	μA
	I _{CCDR2}	V _{CC} = 2.0 to 5.5V *1	—	1.0	100	μA
Data retention set up time	t _{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t _R		t _{RC} *2	—	—	ns

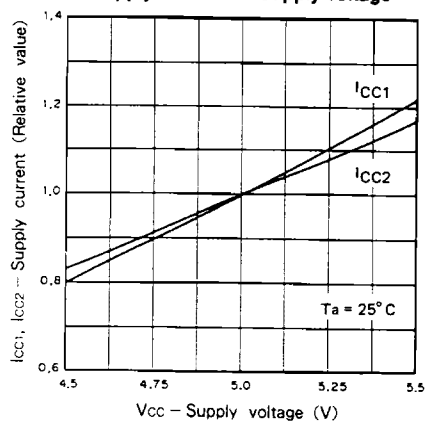
*1 $\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ *2 t_{RC}: Read cycle timeData Retention Waveform (1): [$\overline{CE1}$ control]

Data Retention Waveform (2): [CE2 control]

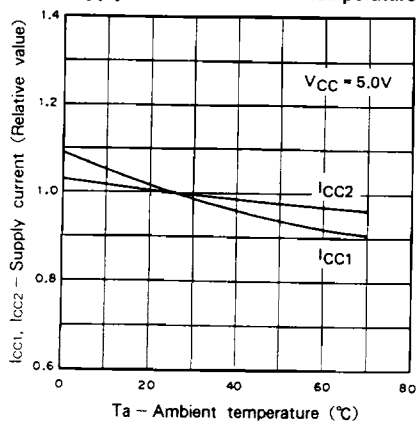


Example of Representative Characteristics

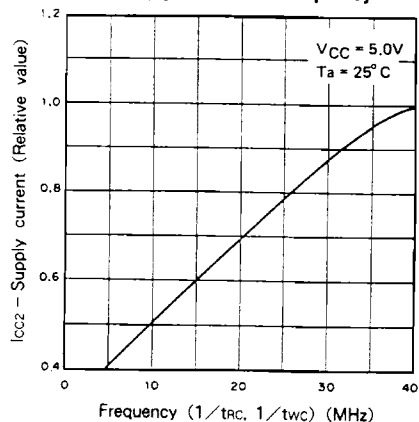
Supply current vs. Supply voltage



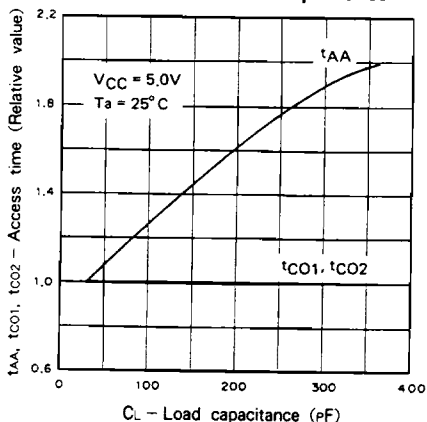
Supply current vs. Ambient temperature



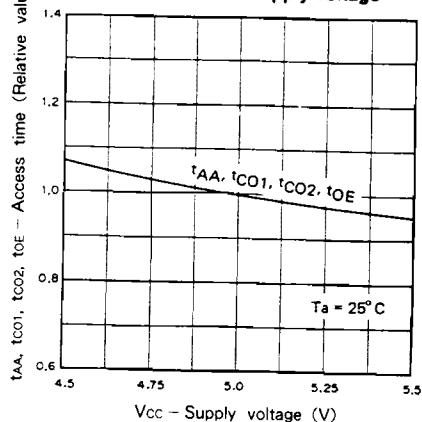
Supply current vs. Frequency



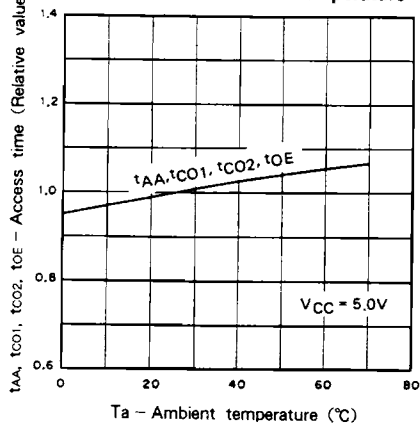
Access time vs. Load capacitance



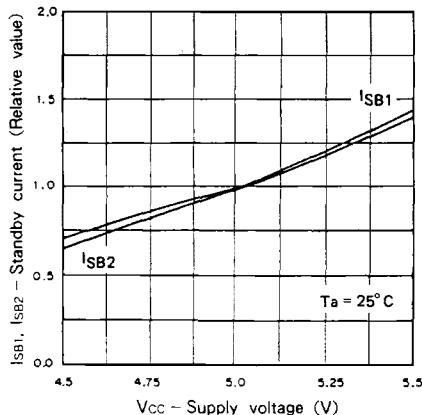
Access time vs. Supply voltage



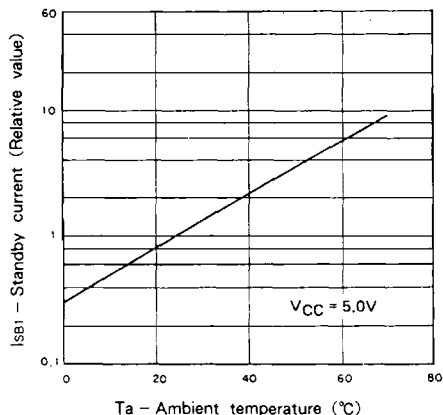
Access time vs. Ambient temperature



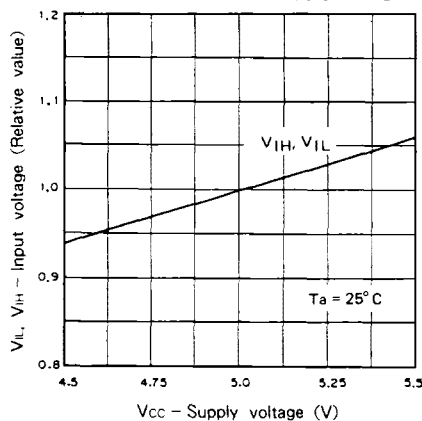
Standby current vs. Supply voltage



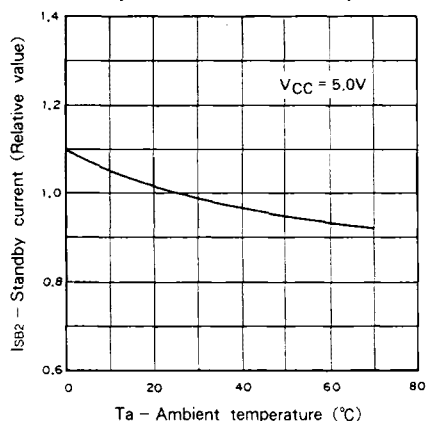
Standby current vs. Ambient temperature



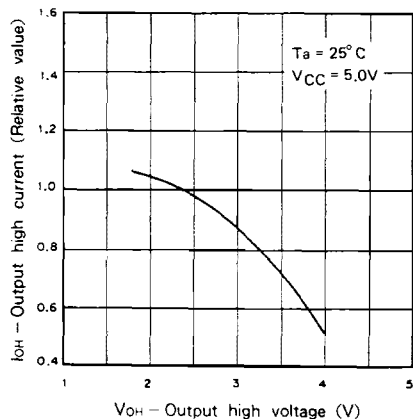
Input voltage level vs. Supply voltage



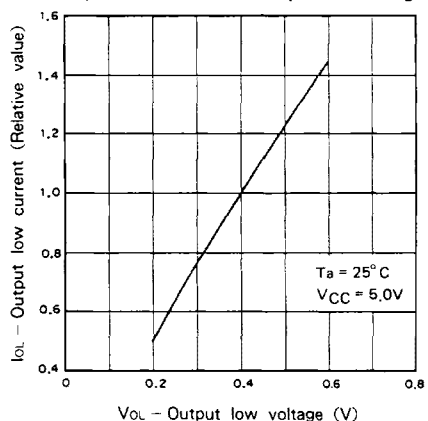
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

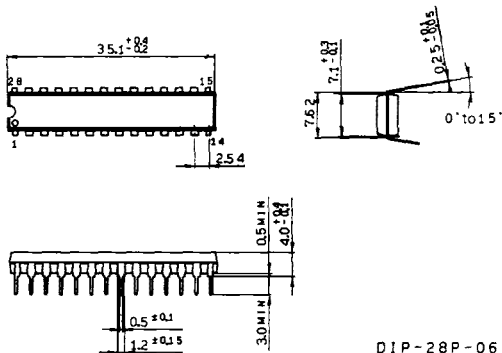


Output low current vs. Output low voltage

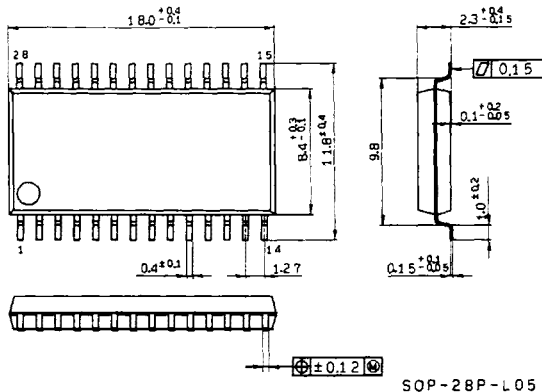


Package Outline Unit : mm

CXK5971P 28 pin DIP (Plastic) 300mil 2.0g



CXK5971M 28 pin SOP (Plastic) 450mil 0.7g



CXK5971J 28 pin SOJ (Plastic) 300mil 0.8g

