

NEC**MOS INTEGRATED CIRCUIT**
 μ PD780961, 780962, 780963, 780964**8-BIT SINGLE-CHIP MICROCONTROLLER**

The μ PD780961, 780962, 780963, and 780964, which are members of the μ PD780964 subseries of the 78K/0 series, are suited to control general-purpose inverters.

Compared to the conventional μ PD78014 subseries or μ PD78018F subseries products, EMI (Electro Magnetic Interface) noise is reduced for the μ PD780924 subseries products.

A flash memory version, the μ PD78F0964, that can operate within the same power supply voltage range as the mask ROM version, and various development tools are also provided.

The details of functions are described in the following user's manuals. Be sure to read them before designing.

μ PD780924, 780964 Subseries User's Manual : In preparation
78K/0 Series User's Manual Instructions : IEU-1372

FEATURES

- Internal ROM and RAM

Item Part Number	Program memory (ROM)	Data memory (internal high-capacity RAM)	Package
μ PD780961	8 Kbytes	512 bytes	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 x 14 mm)
μ PD780962	16 Kbytes		
μ PD780963	24 Kbytes	1024 bytes	
μ PD780964	32 Kbytes		

- External memory expansion space: 48 Kbytes
- Minimum instruction execution time: 0.24 μ s (@ $f_x = 8.38$ -MHz operation)
- I/O ports: 47
- 10-bit resolution A/D converter: eight channels
- Serial interface: two channels
- Timer: Five channels
- Power supply voltage: $V_{DD} = 2.7$ to 5.5 V

APPLICATIONS

Motor control for inverter-type air conditioners, washing machines, etc.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

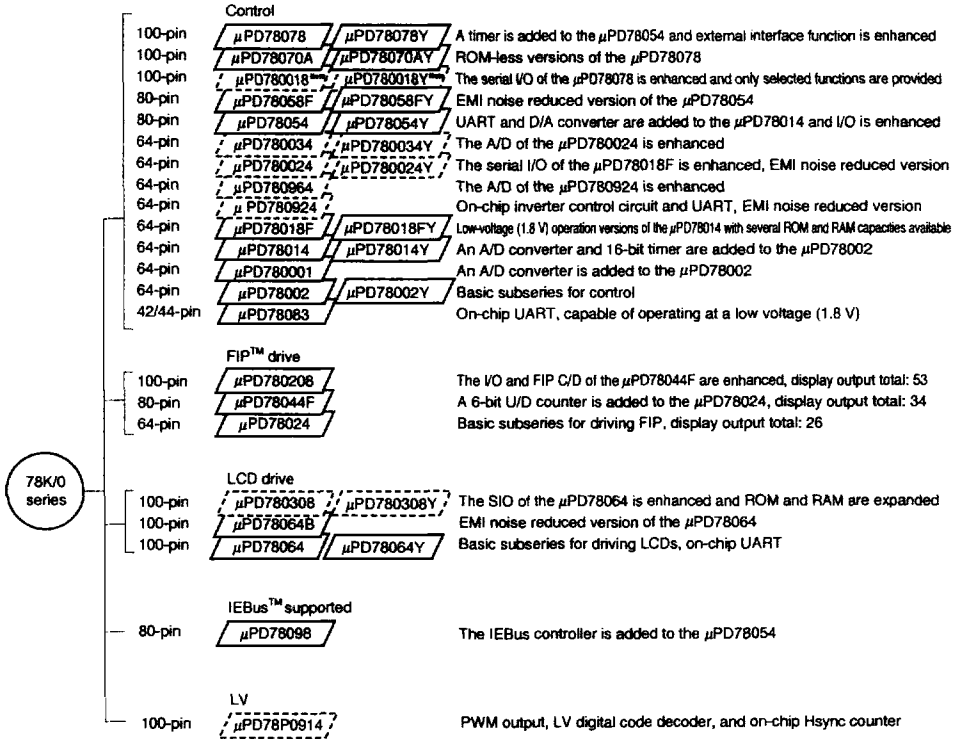
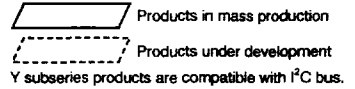
ORDERING INFORMATION

Part Number	Package
μ PD780961CW-xxx	64-pin plastic shrink DIP (750 mil)
μ PD780962CW-xxx	64-pin plastic shrink DIP (750 mil)
μ PD780963CW-xxx	64-pin plastic shrink DIP (750 mil)
μ PD780964CW-xxx	64-pin plastic shrink DIP (750 mil)
μ PD780961GC-xxx-AB8	64-pin plastic QFP (14 x 14 mm)
μ PD780962GC-xxx-AB8	64-pin plastic QFP (14 x 14 mm)
μ PD780963GC-xxx-AB8	64-pin plastic QFP (14 x 14 mm)
μ PD780964GC-xxx-AB8	64-pin plastic QFP (14 x 14 mm)

Remark xxx indicates the ROM code suffix.

78K/0 SERIES DEVELOPMENT

The 78K/0 series product line-up is shown below. Subseries names are shown inside frames.



Note Under planning

The table below shows the main differences between subseries.

Subseries		Functions	ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V _{DD} MIN. Value	External Expansion
				8-bit	16-bit	Watch	WDT							
For control	μPD78078	32 K to 60 K	4ch	1ch	1ch	1ch	8ch	—	2ch	3ch (UART: 1ch)	88	1.8 V	Available	
	μPD78070A	—								61	2.7 V			
	μPD780018	48 K to 60 K	2ch	—	2ch	3ch (UART : 1ch)	88	69	2.0 V					
	μPD78058F	16 K to 60 K												
	μPD78054	16 K to 60 K	—	8ch	—	51	1.8 V							
	μPD780034	8 K to 32 K												
	μPD780024	8 K to 32 K	8ch	—	8ch	47	2.7ch							
	μPD780964	8 K to 32 K												
	μPD780924	8 K to 32 K	3ch	Note	—	8ch	—	53	1.8 V					
	μPD78018F	8 K to 60 K	2ch	1ch	1ch	—	2.7 V							
	μPD78014	8 K to 32 K	—	—	—	39	—							
	μPD780001	8 K												
μPD78002	8 K to 16 K	—	1ch	—	53	—	Available							
μPD78083	8 K to 16 K	—	—	—	8ch	—	33	1.8 V	—					
For FIP drive	μPD780208	32 K to 60 K	2ch	1ch	1ch	1ch	8ch	—	—	2ch	74	2.7 V	—	
	μPD78044F	16 K to 40 K									68			
	μPD78024	24 K to 32 K									54			
For LCD drive	μPD780308	48 K to 60 K	2ch	1ch	1ch	1ch	8ch	—	—	3ch (UART: 1ch)	57	1.8 V	—	
	μPD78064B	32 K								2ch (UART : 1ch)	68	2.0 V		
	μPD78064	16 K to 32 K												
iEBus support	μPD78098	32 K to 60 K	2ch	1ch	1ch	1ch	8ch	—	2ch	3ch (UART: 1ch)	69	2.7 V	Available	
For LV	μPD78PC914	32K	6ch	—	—	1ch	8ch	—	—	2ch	54	4.5 V	Available	

Note 10-bit timer: one channel

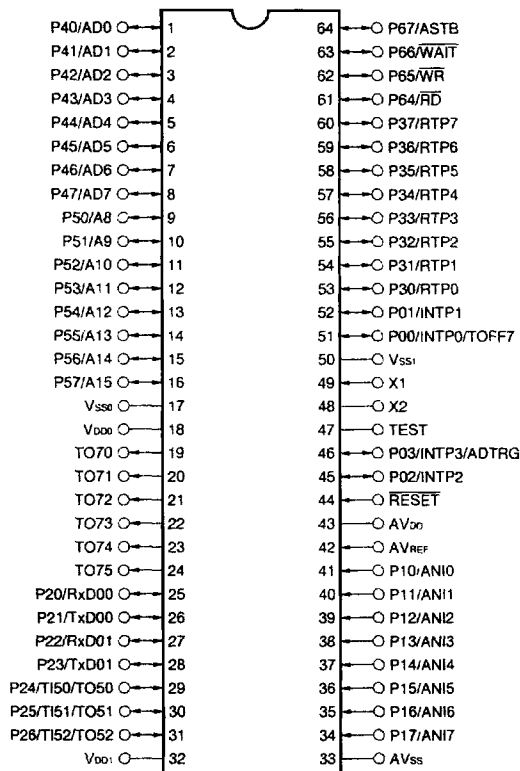
FUNCTION OVERVIEW

Product Name		μ PD780961	μ PD780962	μ PD780963	μ PD780964
Internal memory	ROM	8 Kbytes	16 Kbytes	24 Kbytes	32 Kbytes
	Internal high-speed RAM	512 bytes		1024 bytes	
Memory space		64 Kbytes			
General-purpose register		8 bits x 32 registers (8 bits x 8 registers x 4 banks)			
Instruction cycle		On-chip instruction execution time variable function 0.24 μ s/0.48 μ s/0.96 μ s/1.9 μ s/3.8 μ s (@ 8.38-MHz operation with system clock)			
Instruction set		<ul style="list-style-type: none"> • 16-bit operation • Multiply/divide (8 bits x 8 bits, 16 bits + 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc. 			
I/O ports		Total : 47 <ul style="list-style-type: none"> • CMOS inputs : 8 • CMOS I/Os : 39 			
Real-time output ports		8 bits x 1 or 4 bits x 2			
A/D converter		<ul style="list-style-type: none"> • 8-bit resolution x 8 channels • Power supply voltage: $V_{DD} = 2.7$ to 5.5 V 			
Serial interface		UART x 2 channels			
Timer		<ul style="list-style-type: none"> • 16-bit timer/event counter : 3 channels • 10-bit timer : 1 channel • Watchdog timer : 1 channel 			
Timer output:		9 (8-bit PWM output x 3, and inverter control output x 6)			
Vectored interrupt	Maskable interrupts	Internal: 12, external: 4			
	Non-maskable interrupt	Internal: 1			
	Software interrupt	1			
Power supply voltage		$V_{DD} = 2.7$ to 5.5 V			
Operating ambient temperature		$T_A = -40$ to +85 °C			
Package		<ul style="list-style-type: none"> • 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 x 14 mm) 			

1. PIN CONFIGURATION (Top View)

• 64-Pin Plastic Shrink DIP (750 mil)

μPD780961CW-xxx, 780962CW-xxx, 780963CW-xxx, 780964CW-xxx

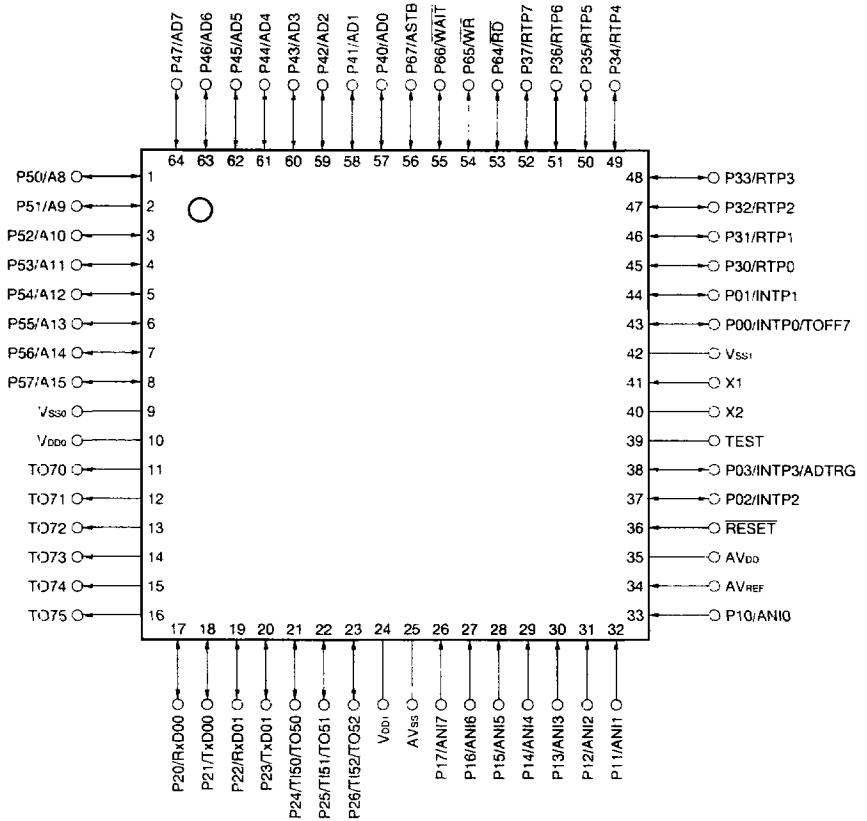


- Cautions**
1. Connect the TEST pin to VSS0 directly.
 2. Connect the AVDD pin to VDD0.
 3. Connect the AVSS pin to VSS0.

Remark When the μPD780961, 780962, 780963, or 780964 is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to VDD0 and VSS1 individually and connecting VSS0 and VSS1 to different ground lines, is recommended.

• 64-Pin Plastic QFP (14 x 14 mm)

μPD780961GC-xxx-AB8, 780962GC-xxx-AB8, 780963GC-xxx-AB8, 780964GC-xxx-AB8

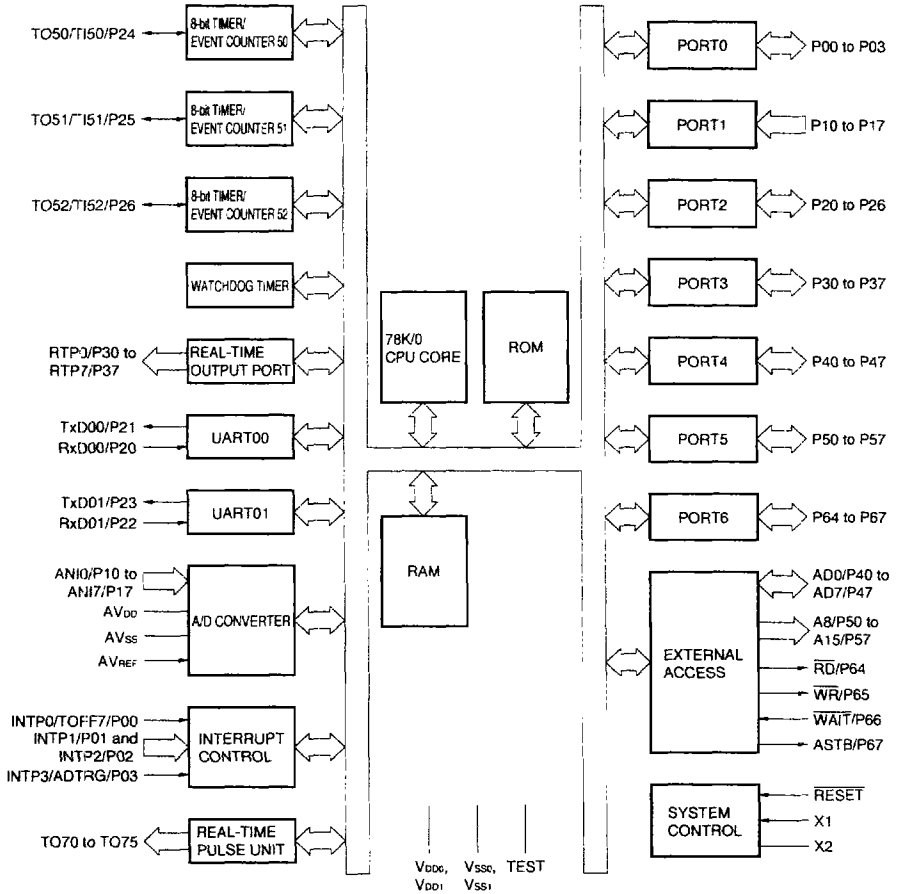


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1. Connect the TEST pin to VSS0 directly.
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 3. Connect the AVSS pin to VSS0.

Remark When the μPD780961, 780962, 780963, or 780964 is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to VDD0 and VSS1 individually and connecting VSS0 and VSS1 to different ground lines, is recommended.

A8 to A15	: Address Bus	\overline{RD}	: Read Strobe
AD0 to AD7	: Address/Data Bus	RESET	: Reset
ADTRG	: AD Trigger Input	RTP0 to RTP7	: Real-time Port
ANI0 to ANI7	: Analog Input	RxD00, RxD01	: Receive Data
ASTB	: Address Strobe	TEST	: Test
AV _{DD}	: Analog Power Supply	TI50 to TI52	: Timer Input
AV _{REF}	: Analog Reference Voltage	TO50 to TO52,	
AV _{SS}	: Analog Ground	TO70 to TO75	: Timer Output
INTP0 to INTP3	: Interrupt From Peripherals	TOFF7	: Timer Output Off
P00 to P03	: Port 0	TxD00, TxD01	: Transmit Data
P10 to P17	: Port 1	V _{DD0} , V _{DD1}	: Power Supply
P20 to P26	: Port 2	V _{SS0} , V _{SS1}	: Ground
P30 to P37	: Port 3	\overline{WAIT}	: Wait
P40 to P47	: Port 4	\overline{WR}	: Write Strobe
P50 to P57	: Port 5	X1, X2	: Crystal
P64 to P67	: Port 6		

2. BLOCK DIAGRAM



Remark Internal ROM and RAM capacity varies depending on the product.

3. PIN FUNCTION LIST

3.1 PORT PINS

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 4-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	INTP0/TOFF7
P01				INTP1
P02				INTP2
P03				INTP3/ADTRG
P10 to P17	Input	Port 1. 8-bit input only port.	Input	AN10 to AN17
P20	I/O	Port 2. 7-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	RxD00
P21				TxD00
P22				RxD01
P23				TxD01
P24				TI50/TO50
P25				TI51/TO51
P26				TI52/TO52
P30 to P37	I/O	Port 3. 8-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	RTP0 to RTP7
P40 to P47	I/O	Port 4. 8-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	AD0 to AD7
P50 to P57	I/O	Port 5. 8-bit I/O port. Input/output can be specified bit-wise. LEDs can be driven directly. When used as an input port, an on-chip pull-up resistor can be connected by software..	Input	A8 to A15
P64	I/O	Port 6. 4-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	RD
P65				WR
P66				WAIT
P67				ASTB

3.2 NON PORT PINS

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	input	External interrupt input that can specify the effective edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TOFF7
INTP1			Input	P01
INTP2			Input	P02
INTP3			Input	P03/ADTRG
TI50	Input	External count clock input to timer (TM50).	Input	P24/TO50
TI51		External count clock input to timer (TM51).	Input	P25/TO51
TI52		External count clock input to timer (TM52).	Input	P26/TO52
TO50	Output	Timer (TM50) output.	Input	P24/TI50
TO51		Timer (TM51) output.	Input	P25/TI51
TO52		Timer (TM52) output.	Input	P26/TI52
RTP0 to RTP7	Output	Real-time output port that outputs pulses in synchronization with trigger signals outputs from the real-time pulse unit.	Input	P30 to P37
TxD00	Output	Asynchronous serial interface serial data output.	Input	P21
TxD01			Input	P23
RxD00	Input	Asynchronous serial interface serial data input.	Input	P20
RxD01			Input	P22
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	External trigger signal input to the A/D converter.	Input	P03/INTP3
TO70 to TO75	Output	Timer output for the 3-phase PWM inverter control.	Hi-Z	-
TOFF7	Input	Timer output (TO70 to TO75) stop interrupt input.	Input	P00/INTP0
AD0 to AD7	I/O	Lower address/data bus when memory is expanded externally.	Input	P40 to P47
A8 to A15	Output	Upper address bus when memory is expanded externally.	Input	P50 to P57
RD	Output	Strobe signal output for external memory read operation.	Input	P64
WR		Strobe signal output for external memory write operation.	Input	P65
WAIT	Input	Wait insertion when accessing external memory.	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory.	Input	P67
AVREF	Input	A/D converter reference voltage input.	-	-
AVDC	-	A/D converter analog power supply. Connect to V _{DD} .	-	-
AVSS	-	A/D converter ground potential. Connect to V _{SS} .	-	-
RESET	Input	System reset input.	-	-
X1	Input	Crystal connection for system clock oscillation.	-	-
X2			-	-
V _{DD}	-	Positive power supply for ports.	-	-
V _{SS}	-	Ground potential for ports.	-	-
V _{DD1}	-	Positive power supply except for ports.	-	-
V _{SS1}	-	Ground potential except for ports.	-	-
TEST	-	Test mode set pin. Connect to V _{SS} directly.	-	-

3.3 RECOMMENDED CONNECTION OF UNUSED PINS

The recommended connections of unused pins are shown in Table 3-1.

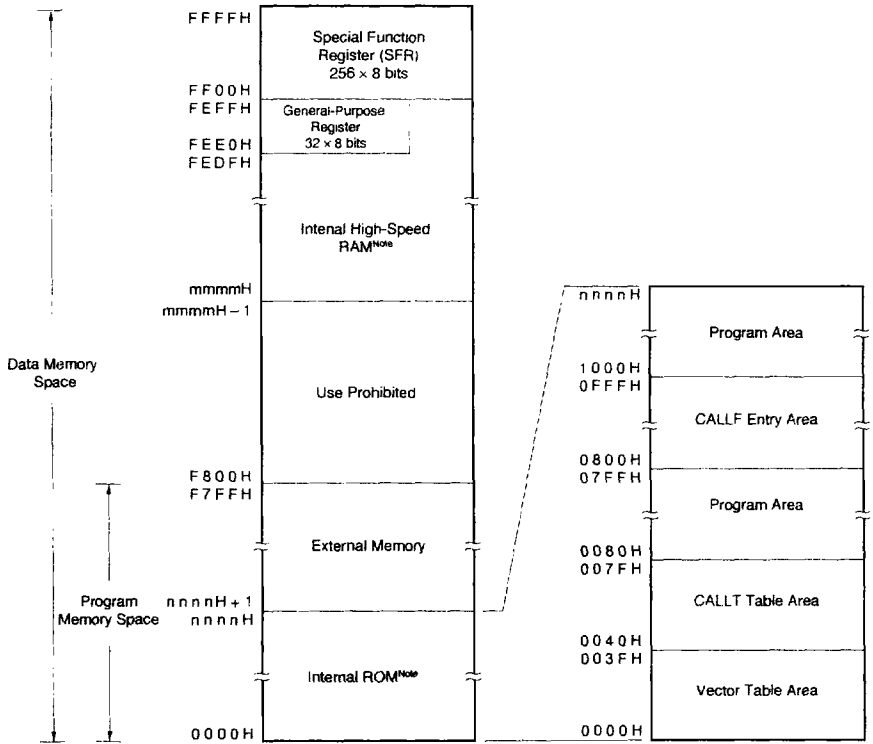
Table 3-1. Recommended Connection of Unused Pins

Pin Name	I/O	Recommended Connection of Unused Pins
P00:/NTP0/TOFF7	I/O	Individually connect to V _{SS0} via a resistor.
P01:/NTP1		
P02:/NTP2		
P03:/NTP3/ADTRG		
P10/ANI0 to P17/ANI7	Input	Individually connect to V _{DD0} or V _{SS0} via a resistor.
P20/RxD00	I/O	
P21/TxD00		
P22/RxD01		
P23/TxD01		
P24, TI50/TO50		
P25, TI51/TO51		
P26, TI52/TO52		
P30/RTP0 to P37/RTP7		
P40/AD0 to P47/AD7		
P50/A8 to P57/A15		
P64/RD		
P65/WR		
P66/WAIT		
P67/ASTB		
TO70 to TO75		
AV _{DD0}	-	Connect to V _{DD0} .
AV _{REF}		Connect to V _{SS0} .
AV _{SS}		
TEST		Connect to V _{SS0} directly.

4. MEMORY SPACE

The memory map of the μPD780961, 780962, 780963, and 780964 is shown in Figure 4-1.

Figure 4-1. Memory Map



Note The internal ROM and internal high-speed RAM capacity differ depending on the product (see the table below).

Product Name	Internal ROM End Address nnnnH	Internal High-Speed RAM Start Address mmmmH
μPD780961	1FFFH	FD00H
μPD780962	3FFFH	
μPD780963	5FFFH	FB00H
μPD780964	7FFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 PORTS

Two kinds of I/O ports are provided.

- CMOS input (Port 1) : 8
 - CMOS input/output (Port 0, ports 2 to 6) : 39
-
- Total : 47

Table 5-1. Functions of Ports

Port Name	Pin Name	Function
Port 0	P01 to P03	I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.
Port 1	P10 to P17	Input only port.
Port 2	P20 to P26	I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.
Port 3	P30 to P37	I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.
Port 4	P40 to P47	I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.
Port 5	P50 to P57	I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software. LEDs can be driven directly.
Port 6	P64 to P67	I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.

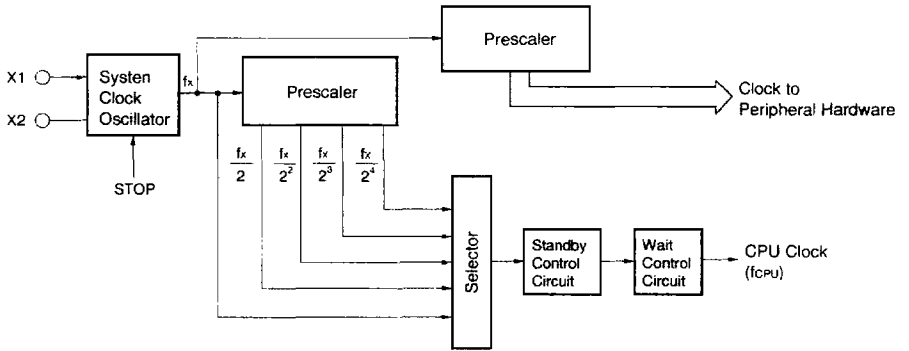
5.2 CLOCK GENERATOR

A system clock generator is incorporated.

The instruction execution time can be changed.

- 0.24 μ s/0.48 μ s/0.96 μ s/1.9 μ s/3.8 μ s (@ 8.38-MHz operation with system clock)

Figure 5-1. Clock Generator Block Diagram



5.3 TIMER/EVENT COUNTERS

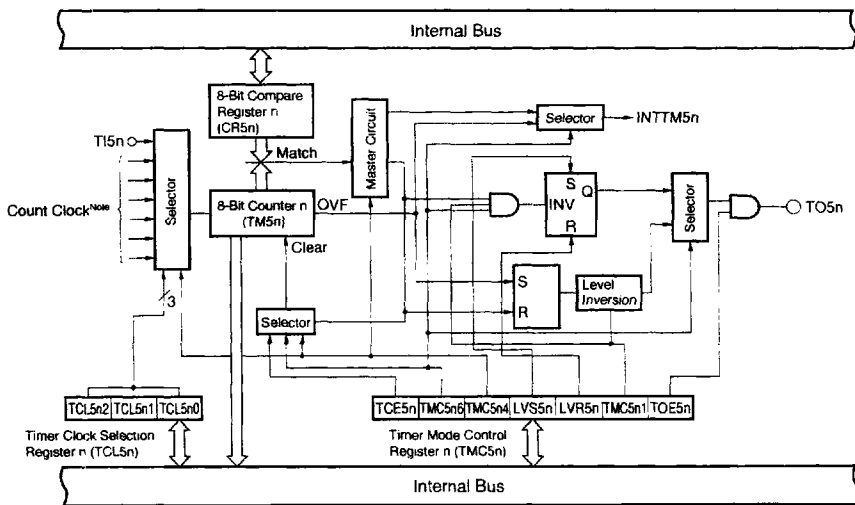
Five timer/event counter channels are incorporated.

- 8-bit timer/event counter : 3 channels
- 10-bit timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counters

		8-bit Timer/Event Counter	10-bit Timer	Watchdog Timer
Type	Interval timer	3 channels	1 channel	1 channel
	External event counter	3 channels	—	—
Functions	Timer output	3 outputs	6 outputs	—
	PWM output	3 outputs	—	—
	Square wave output	3 outputs	—	—
	Interrupt request	3	1	1

Figure 5-2. 8-Bit Timer/Event Counter Block Diagram



Note Count clock differs depending on the timer

TM50 : $fx/2, fx^2, fx^5, fx^7, fx^9, fx^{11}$

TM51 : $fx, fx/2, fx^2, fx^3, fx^4, fx^5$

TM52 : $fx^4, fx^5, fx^6, fx^7, fx^8, fx^9$

Remark n = 0 to 2

Figure 5-3. 10-bit Timer Block Diagram

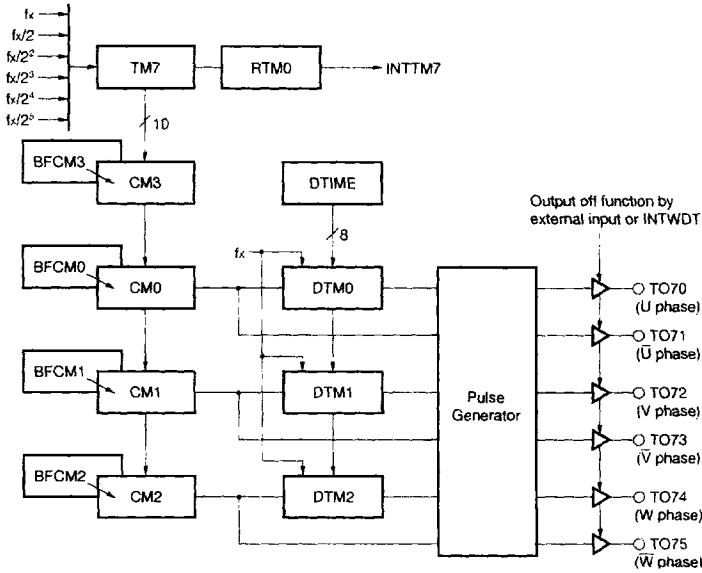
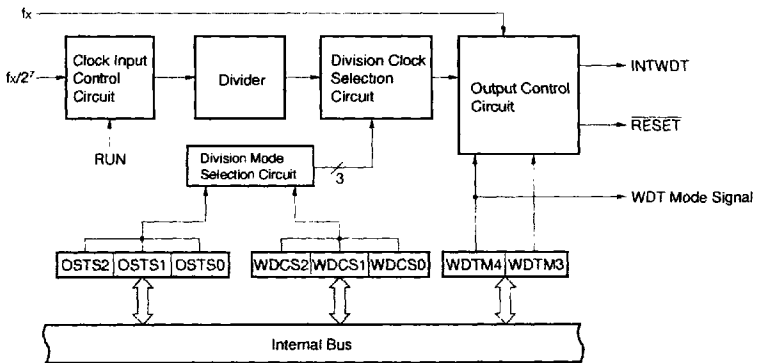


Figure 5-4. Watchdog Timer Block Diagram

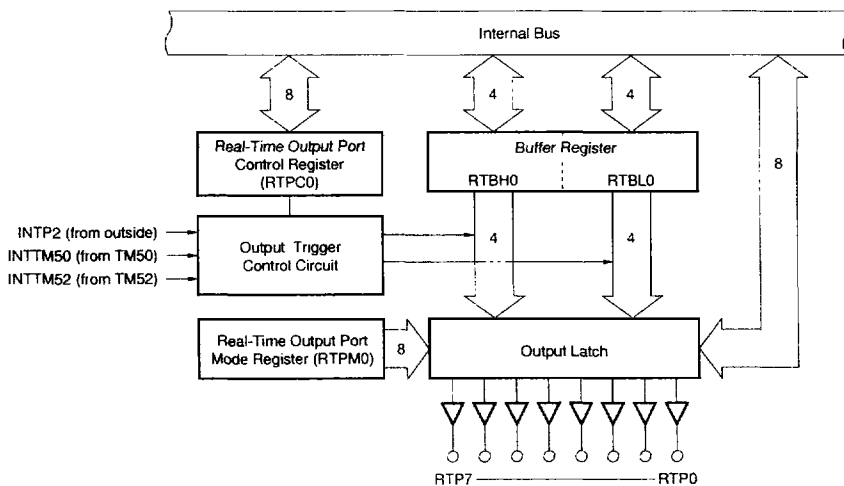


5.4 REAL-TIME OUTPUT PORT

The real-time output port outputs data stored in buffers in synchronization with match interrupts of 8-bit timer/event counters (TM50 and TM52) or external interrupts, enabling to output pulses without jitter.

Therefore, the real-time output method is suited for applications which output given patterns at set intervals.

Figure 5-5. Real-Time Output Port Block Diagram

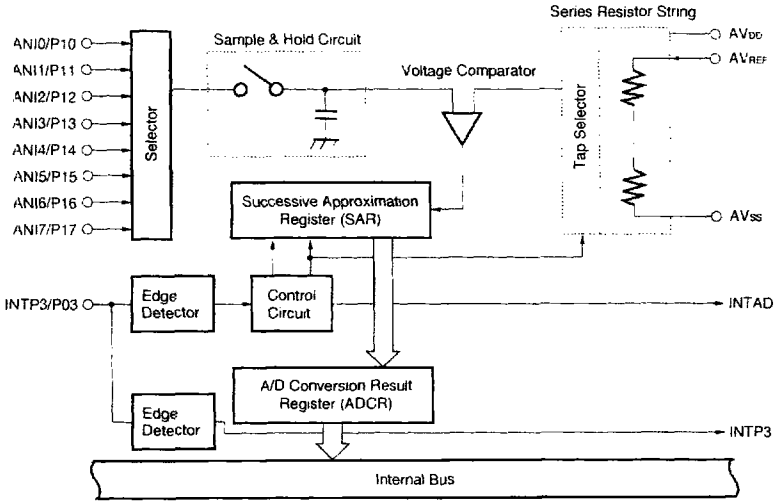


5.5 A/D CONVERTER

Eight 10-bit resolution A/D converter channels are incorporated.
A/D conversion by the following two methods.

- Hardware start
- Software start

Figure 5-6. A/D Converter Block Diagram



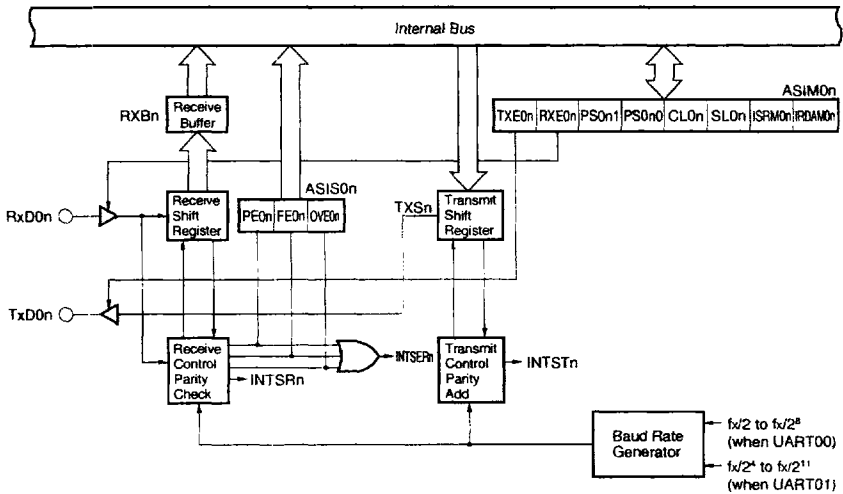
5.6 SERIAL INTERFACE

Two independent serial interface channels (UART00 and UART01) are incorporated.

Each serial interface incorporates a baud-rate generator. Therefore, it is possible to set a serial transfer rate that is independent of the operating clock frequency.

The serial transfer rate can be set from 75 to 76800 bps (@ $f_x = 8.38\text{-MHz}$ operation) by setting the mode register.

Table 5-7. Serial Interface Block Diagram



Remark $n = 0, 1$

6. INTERRUPT FUNCTIONS

There are 18 interrupt functions of three different kinds as shown below.

- Non-maskable interrupt : 1
- Maskable interrupts : 16
- Software interrupt : 1

Table 6-1. Interrupt Source List

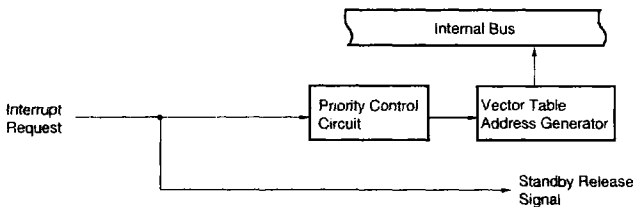
Interrupt Type	Default Priority <small>Note 1</small>	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type <small>Note 2</small>		
		Name	Trigger					
Non-maskable	—	INTWDT	Watchdog timer overflow (when non-maskable interrupt is selected)	Internal	0004H	(A)		
Maskable	0	INTWDT	Watchdog timer overflow (when interval timer is selected)			External	0006H 0008H 000AH 000CH	(B)
	1	INTP0	Pin input edge detection	Internal	000EH 0010H 0012H 0014H 0016H 0018H 001AH 001CH 001EH 0020H 0022H			(C)
	2	INTP1						
	3	INTP2						
	4	INTP3						
	5	INTTM7	TM7 under flow	Internal	000EH 0010H 0012H 0014H 0016H 0018H 001AH 001CH 001EH 0020H 0022H	(B)		
	6	INTSER0	UART00 receive error generation					
	7	INTSR0	UART00 receive termination					
	8	INTST0	UART00 transmit termination					
	9	INTSER1	UART01 receive error generation					
	10	INTSR1	UART01 receive termination					
	11	INTST1	UART01 transmit termination					
	12	INTTM50	TM50 and CR50 match signal generation					
	13	INTTM51	TM51 and CR51 match signal generation					
	14	INTTM52	TM52 and CR52 match signal generation					
15	INTAD0	A/D conversion termination						
Software	—	BRK	BRK instruction execution	—	003EH	(D)		

Notes 1. The default priority is the priority applicable when more than one maskable interrupt is generated. 0 is the highest priority and 15, the lowest.

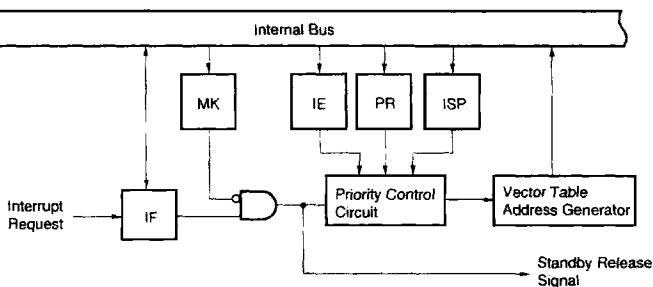
2. Basic configuration types (A) to (D) correspond to (A) to (D) on the next page.

Figure 6-1. Basic Interrupt Function Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External Maskable Interrupt

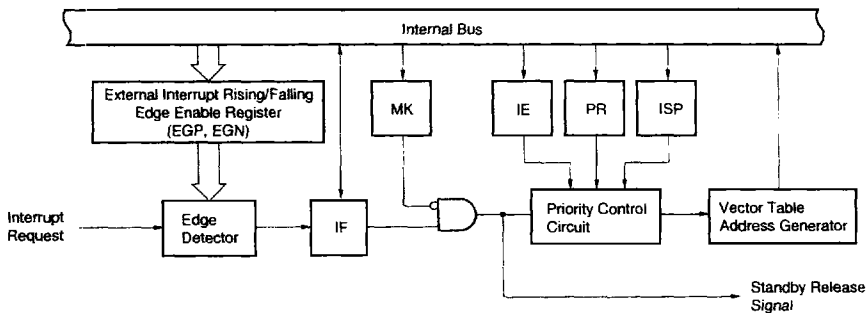
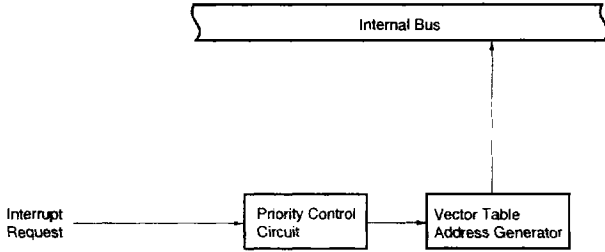


Figure 6-1. Basic Interrupt Function Configuration (2/2)

(D) Software Interrupt



- IF : Interrupt request flag
- IE : Interrupt enable flag
- ISP : In-service priority flag
- MK : Interrupt mask flag
- PR : Priority specification flag

7. EXTERNAL DEVICE EXPANSION FUNCTION

The external device expansion function is used to connect external devices to areas other than the internal ROM, RAM and SFR.

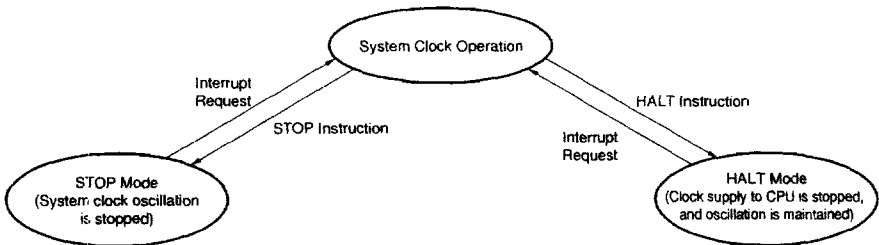
Ports 4 to 6 are used for connection with external devices.

8. STANDBY FUNCTIONS

There are the following two standby functions to reduce the current consumption.

- HALT mode : The CPU operating clock is stopped. The average current consumption can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The system clock oscillation is stopped. The whole operation by the system clock is stopped, so that the system operates with ultra-low power dissipation.

Figure 8-1. Standby Functions



9. RESET FUNCTIONS

There are the following two reset methods.

- External reset by RESET input.
- Internal reset by watchdog timer runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand 1st Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	\$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r=A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand 1st Operand	#word	AX	rp ^{Note}	sfrp	saddrp	laddr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW ^{Note}						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
laddr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL.

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand 1st Operand	A.bit	sfr.bit	saddr.bit	PWS.bit	[HL].bit	CY	Saddr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

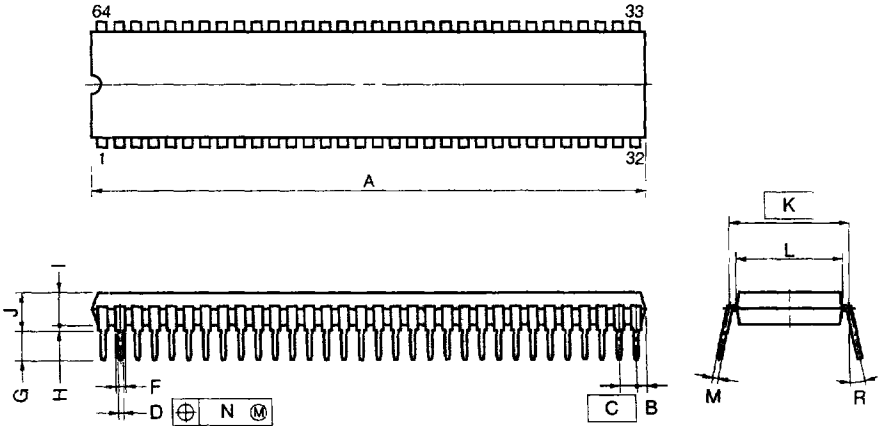
2nd Operand 1st Operand	AX	laddr16	laddr11	[addr5]	Saddr16
Basic instruction	BR	CALL, BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT, BF, BTCLR, DBNZ

(5) Other Instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



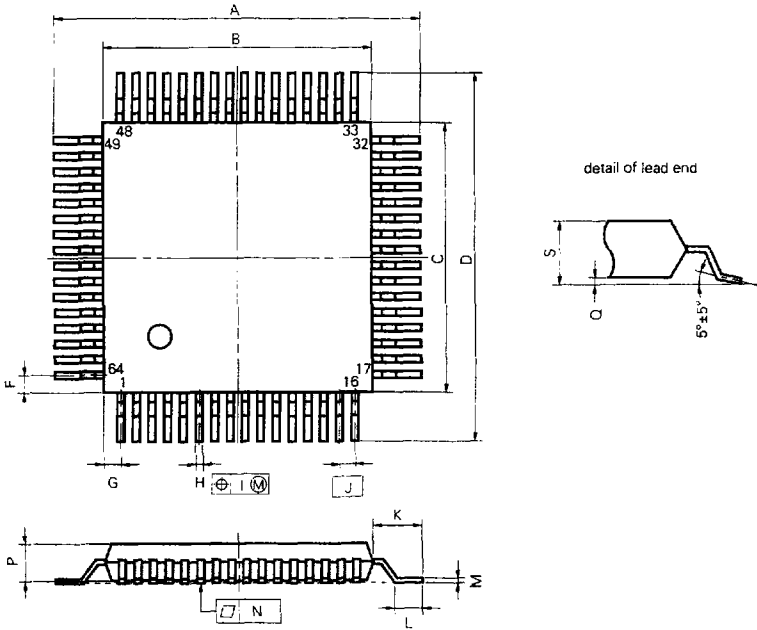
NOTE

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.128±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.689
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.17	0.007
R	0-15°	0-15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (□14)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P64GC-80-AB8-3

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	0.551 ^{+0.009} / _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} / _{-0.008}
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	0.014 ^{+0.004} / _{-0.005}
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	0.031 ^{+0.009} / _{-0.008}
M	0.15 ^{+0.10} / _{-0.05}	0.006 ^{+0.004} / _{-0.003}
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.