

M61311SP/M61316SP**I²C BUS CONTROLLED VIDEO PRE-AMP FOR HIGH RESOLUTION COLOR DISPLAY****DESCRIPTION**

M61311SP/M61316SP is Semiconductor Integrated Circuit for CRT Display Monitor. It includes OSD Blanking, OSD Mixing, Retrace Blanking, Video Detector, Sync Separator, Wide Band Amplifier, Brightness Control. Main/Sub Contrast, Video Response Adjust, Ret BLK Adjust, 4ch D/A OUT and OSD level Adjust Function can be controlled by IIC Bus.

FEATURES

Frequency Band Width

RGB: 200MHz (M61311SP)
150MHz (M61316SP)
(4Vp-p at -3dB)

OSD: 80MHz

Input

RGB: 0.7Vp-p (typical)
OSD: 3.5V --- 5.0V (positive)
OSD BLK: 3.5V --- 5.0V (positive)
Retrace BLK: 2.5V --- 5.0V (positive)
Clamp Pulse: 2.5V --- 5.0V (positive)

Output

RGB: 5Vp-p
(at Brightness less than 2VDC)
OSD: 4Vp-p
(at Brightness less than 2VDC)
Sync OUT: 5Vp-p
Video Det OUT: High = 4.2VDC , Low = 0.7VDC

STRUCTURE

Bipolar Silicon Monolithic IC

APPLICATION

CRT Display Monitor

RECOMMENDED OPERATING CONDITIONS

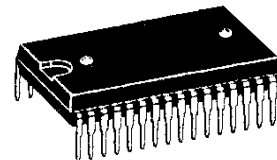
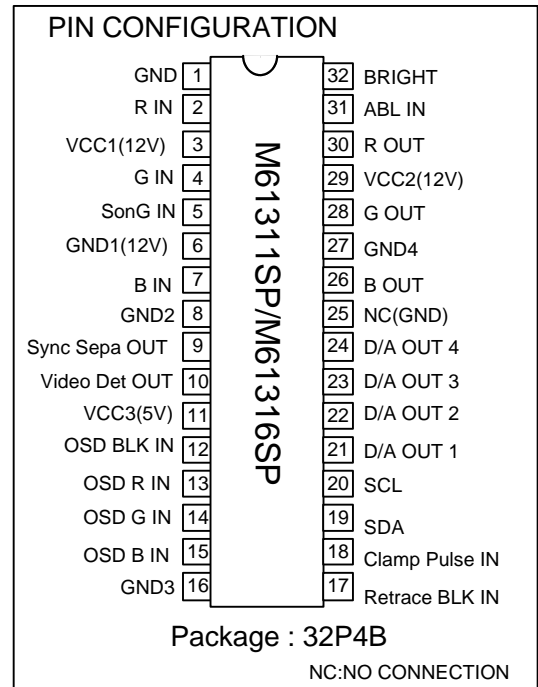
Supply Voltage Range 11.50V --- 12.50V (V3,V29)
4.75V --- 5.25V (V11)

Rated Supply Voltage 12.00V (V3,V29)
5.00V (V11)

MAJOR SPECIFICATION

IIC Bus Controlled 3ch Video Pre-Amp with OSD Mixing Function and Retrace Blanking Function.

The difference in the M61311SP/M61316SP is RGB Video Frequency Band Width. M61311SP is 200MHz, M61316SP is 150MHz in conditions RGB Output is 4Vp-p at -3dB.



32 pin plastic SDIP

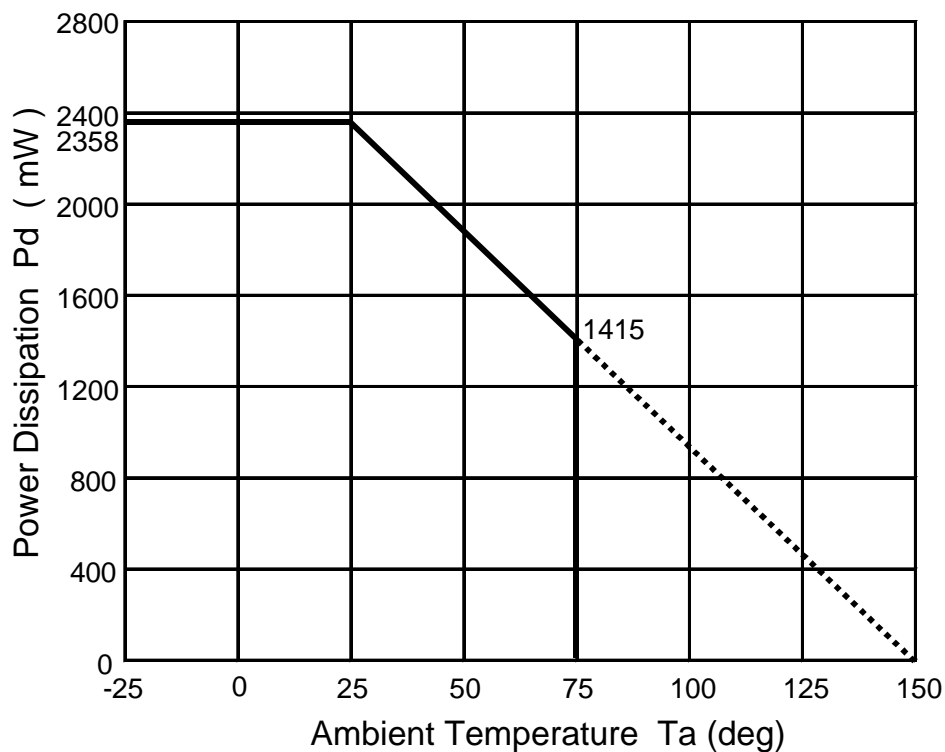
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ABSOLUTE MAXIMUM RATING (Ambient temperature:25deg)

Parameter	Symbol	Rating	Unit
Supply voltage (Pin3,29)	Vcc12	13.0	V
Supply voltage (Pin11)	Vcc5	6.0	V
Power dissipation	Pd	2358	mW
Ambient temperature	Topr	-20 --- +75	deg
Storage temperature	Tstg	-40 --- +150	deg
Recommend supply 12	Vopr12	12.0	V
Recommend supply 5	Vopr5	5.0	V
Voltage range 12	Vopr'12	11.5 --- 12.5	V
Voltage range 5	Vopr'5	4.75 --- 5.25	V

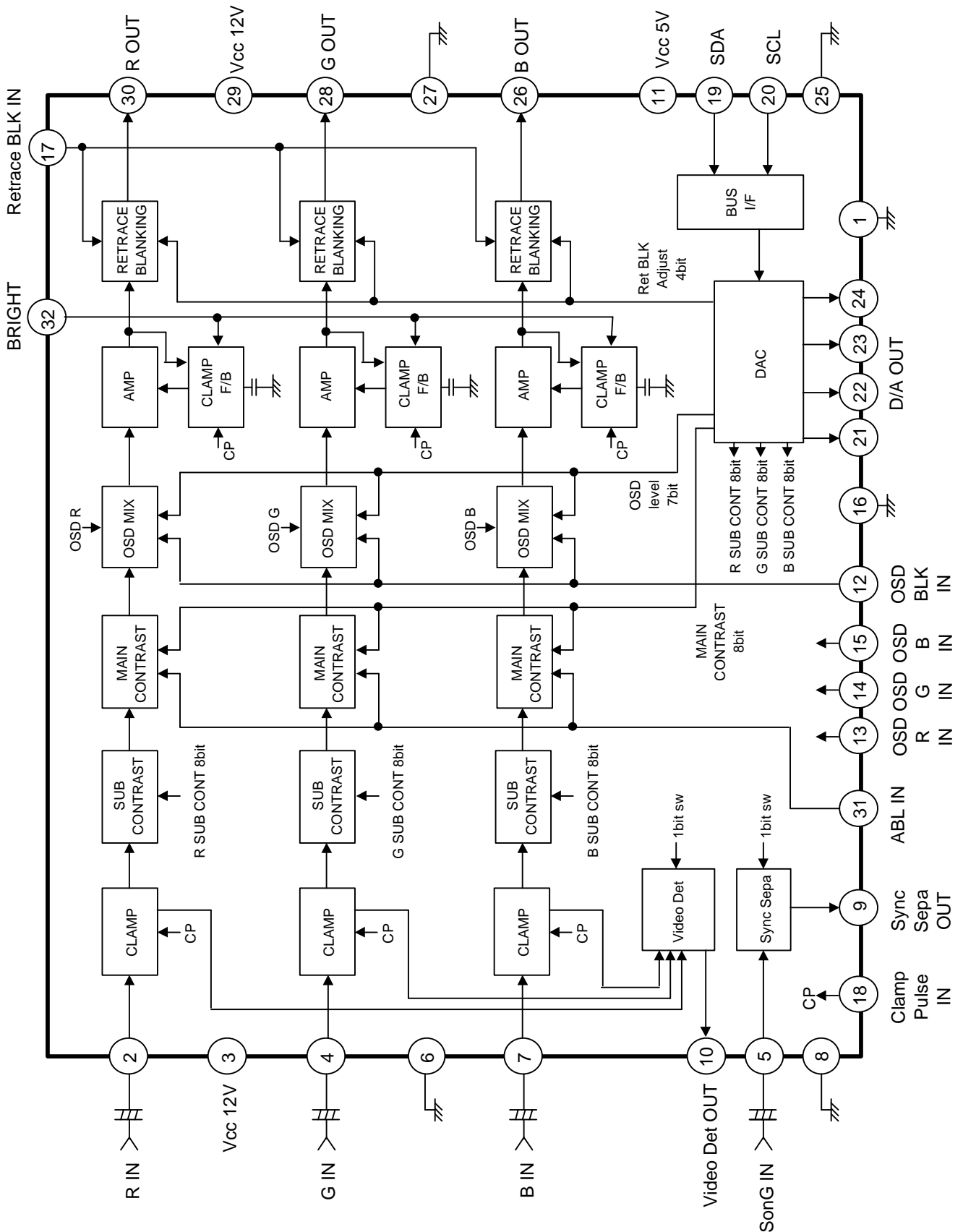
THERMAL DERATING (Maximum Rating)



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BLOCK DIAGRAM



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BUS CONTROL TABLE

(1) Slave address:

D7	D6	D5	D4	D3	D2	D1	R/W	
1	0	0	0	1	0	0	0	=88H

(2) Slave receiver format:

Normal mode

8bit			8bit			8bit		
S	SLAVE ADDRESS	A	SUB ADDRESS	A	DATA BYTE	A	P	

Auto increment mode

8bit			8bit			8bit		
S	SLAVE ADDRESS	A	SUB ADDRESS (0XH)+10H	A	DATA (SUB ADDRESS=0XH)	A		

8bit			8bit			8bit		
DATA (SUB ADDRESS=0(X+1)H)	A	DATA (SUB ADDRESS=0(X+2)H)	A	-----				

S:Start condition
A:Acknowledge
P:Stop condition

(3) Sub address byte and data byte format:

Function	Bit	Sub add	Data byte(top:byte format under:start condition)							
			D7	D6	D5	D4	D3	D2	D1	D0
Main contrast	8	00H	A07	A06	A05	A04	A03	A02	A01	A00
			0	0	0	0	0	0	0	1
Sub contrast R	8	01H	A17	A16	A15	A14	A13	A12	A11	A10
			0	0	0	0	0	0	0	1
Sub contrast G	8	02H	A27	A26	A25	A24	A23	A22	A21	A20
			0	0	0	0	0	0	0	1
Sub contrast B	8	03H	A37	A36	A35	A34	A33	A32	A31	A30
			0	0	0	0	0	0	0	1
OSD level	7	04H	-	A46	A45	A44	A43	A42	A41	A40
			-	0	0	0	0	0	0	1
RE-BLK Adjust	4	05H	-	-	-	-	A53	A52	A51	A50
			-	-	-	-	0	0	0	1
Sharpness control	4	06H	-	-	-	-	A63	A62	A61	A60
			-	-	-	-	0	0	0	1
Sync Sepa SW	1	06H	-	-	-	A64	-	-	-	-
			-	-	-	0	-	-	-	-
Video Det SW	1	06H	-	-	A65	-	-	-	-	-
			-	-	0	-	-	-	-	-
TEST MODE	2	06H	A67	A66	-	-	-	-	-	-
			0	0	-	-	-	-	-	-
D/A OUT1	8	07H	A77	A76	A75	A74	A73	A72	A71	A70
			0	0	0	0	0	0	0	1
D/A OUT2	8	08H	A87	A86	A85	A84	A83	A82	A81	A80
			0	0	0	0	0	0	0	1
D/A OUT3	8	09H	A97	A96	A95	A94	A93	A92	A91	A90
			0	0	0	0	0	0	0	1
D/A OUT4	8	0AH	AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
			0	0	0	0	0	0	0	1

*)pre-data

*)sub add. 06H

Sync Sepa SW A64 0:Sync Sepa ON 1:Sync Sepa OFF

Video Det SW A65 0:Video Det ON 1:Video Det OFF

Always set up as A66 and A67 in 0.

For IIC Data, please transfer in the period of Vertical.

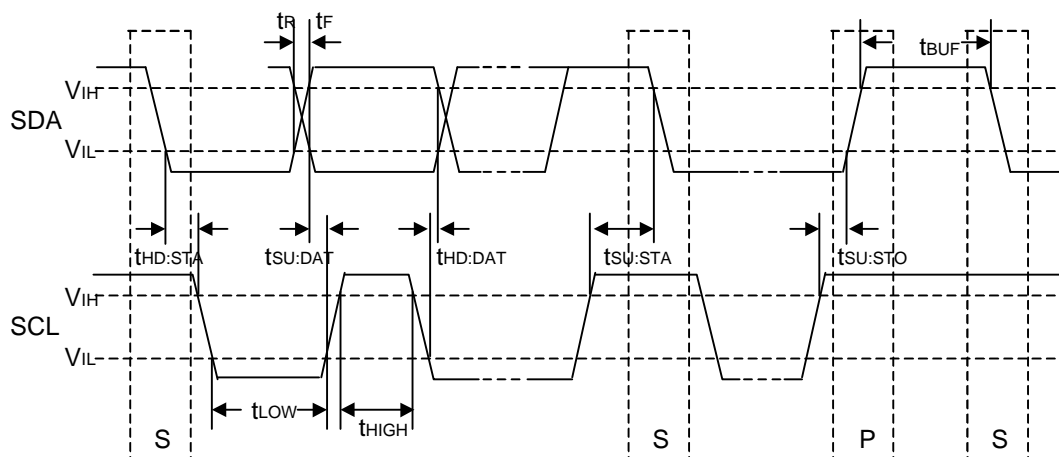
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IIC BUS CONTROL SECTION SDA,SCL CHARACTERISTICS

parameter	symbol	MIN	MAX	unit
min. input LOW voltage	V _{IL}	-0.5	1.5	V
max. input HIGH voltage	V _{IH}	3.0	5.5	V
SCL clock frequency	f _{SCL}	0	400	KHz
Time the bus must be free before a new transmission can start	t _{BUF}	1.3	-	uS
Hold time start condition After this period the first clock pulse is generated	t _{HD:STA}	0.6	-	uS
The LOW period of the clock	t _{LOW}	1.3	-	uS
The HIGH period of the clock	t _{HIGH}	0.6	-	uS
Set up time for start condition (Only relevant for a repeated start condition)	t _{SU:STA}	0.6	-	uS
Hold time DATA	t _{HD:DAT}	0	0.9	uS
Set-up time DATA	t _{SU:DAT}	100	-	nS
Rise time both SDA and SCL lines	t _R	20+0.1Cb	300	nS
Fall time both SDA and SCL lines	t _F	20+0.1Cb	300	nS
Set-up time for stop condition	t _{SU:STO}	0.6	-	uS

TIMING DIAGRAM



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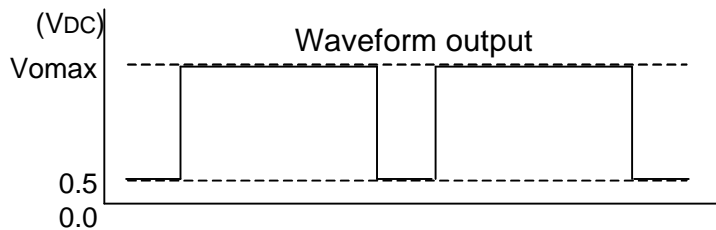
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No.	Symbol	parameter	Test point	Input														CTL Vol		Bus CTL (H)												Limits			Unit
				3 12V Vcc	2 R IN	4 G IN	5 S ON IN	7 B IN	12 OSD BLK	13 OSD R IN	14 OSD G IN	15 OSD B IN	17 RET BLK	18 CP IN	31 ABL (V)	32 BRT (V)	00H Main cont	01H Sub R cont	02H Sub G cont	03H Sub B cont	04H OSD Adj	05H ReBLK Adj	06H Sharp SW	06H S onG SW	06H VDET SW	07H D/A OUT1	08H D/A OUT2	09H D/A OUT3	0AH D/A OUT4	MIN	TYP	MAX			
38	OTr	OSD pulse characteristics 1	26,28,30	b	a	a	a	a	a	b	b	b	a	b	5	2	FF	FF	FF	FF	6F	00	08				FF	FF	FF	FF	-	2	5	nS	
39	OTf	OSD pulse characteristics 2	26,28,30	b	a	a	a	a	a	b	b	b	a	b	5	2	FF	FF	FF	FF	6F	00	08				FF	FF	FF	FF	-	4	7	nS	
40	Oadj1	OSD adjust control characteristics 1 (MAX)	26,28,30	b	a	a	a	a	b	b	b	b	a	b	5	2	FF	FF	FF	FF	7F	00	08				FF	FF	FF	FF	3.3	4.0	4.9	Vp-p	
41	ΔOadj1	OSD adjust control relative characteristics 1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FF	FF	FF	FF	7F	00	08				FF	FF	FF	FF	0.8	1.0	1.2	-	
42	Oadj2	OSD adjust control characteristics 2 (TYP)	26,28,30	b	a	a	a	a	b	b	b	b	a	b	5	2	FF	FF	FF	FF	64	00	08				FF	FF	FF	FF	1.2	1.8	2.4	Vp-p	
43	ΔOadj2	OSD adjust control relative characteristics 2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FF	FF	FF	FF	40	00	08				FF	FF	FF	FF	0.8	1.0	1.2	-	
44	Oadj3	OSD adjust control characteristics 3 (MIN)	26,28,30	b	a	a	a	a	b	b	b	b	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	-0.5	-0.1	0.3	Vp-p	
45	ΔOadj3	OSD adjust control relative characteristics 3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	-0.2	0	0.2	-	
46	VthOSD	OSD input threshold voltage	26,28,30	b	a	a	a	a	a	b	b	b	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	1.7	2.5	3.3	Vdc	
47	OBLK	Black level difference in OSD BLK on/off	26,28,30	b	a	a	a	a	b	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	-0.5	-0.1	0.3	Vdc	
48	ΔOBLK	Relative OBLK	26,28,30	b	a	a	a	a	b	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	-0.2	0	0.2	-	
50	VthBLK	OSD BLK input threshold voltage	26,28,30	b	b	b	a	b	b	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	1.7	2.5	3.3	Vdc	
51	HBLK1	Retrace BLK characteristics 1	26,28,30	b	a	a	a	a	a	a	a	a	b	b	5	2	FF	FF	FF	FF	00	0F	08				FF	FF	FF	FF	1.6	1.9	2.2	Vdc	
52	HBLK2	Retrace BLK characteristics 2	26,28,30	b	a	a	a	a	a	a	a	a	b	b	5	2	FF	FF	FF	FF	00	08	08				FF	FF	FF	FF	1.0	1.3	1.6	Vdc	
53	HBLK3	Retrace BLK characteristics 3	26,28,30	b	a	a	a	a	a	a	a	a	b	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	0.3	0.6	0.9	Vdc	
54	VthHBLK	Retrace BLK input threshold voltage	26,28,30	b	a	a	a	a	a	a	a	a	b	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	0.7	1.5	2.3	Vdc	
55	SS-NV	SOG input maximum noise voltage	9	b	a	a	b	a	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	-	-	0.02	Vp-p	
56	SS-SV	SOG minimum input voltage	9	b	a	a	b	a	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	0.2	-	-	Vp-p	
57	VSH	Sync output high level	9	b	a	a	b	a	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	4.5	4.9	5.0	Vdc	
58	VSL	Sync output low level	9	b	a	a	b	a	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	0	0.4	0.7	Vdc	
59	TDS-F	Sync output delay time 1	9	b	a	a	b	a	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	10	30	65	nS	
60	TDS-R	Sync output delay time 2	9	b	a	a	b	a	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	10	30	65	nS	
61	VD-NV	V-DET input maximum noise voltage	10	b	b	b	a	b	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	-	-	0.05	Vp-p	
62	VD-SV	V-DET minimum input voltage	10	b	b	b	a	b	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	0.2	-	-	Vp-p	
63	VVDH	V-DET output high level	10	b	b	b	a	b	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	3.8	4.2	5.0	Vdc	
64	VVDL	V-DET output low level	10	b	b	b	a	b	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	0	0.7	1.1	Vdc	
65	TDV-F	V-DET output delay time 1	10	b	b	b	a	b	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	10	23	50	nS	
66	TDV-R	V-DET output delay time 2	10	b	b	b	a	b	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	1	13	40	nS	
67	VDH	D/A output maximum voltage	21,22,23,24	b	a	a	a	a	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	4.7	5.2	5.7	Vdc	
68	VDL	D/A output minimum voltage	21,22,23,24	b	a	a	a	a	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				00	00	00	00	0	0	0.5	Vdc	
69	IA+1	D/A OUT input current 1	21,22,23,24	b	a	a	a	a	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				00	00	00	00	0.18	-	-	mA	
70	IA+2	D/A OUT input current 2	21,22,23,24	b	a	a	a	a	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				00	00	00	00	0.18	-	-	mA	
71	IA-	D/A OUT output current	21,22,23,24	b	a	a	a	a	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				FF	FF	FF	FF	-	-	0.4	mA	
72	DNL	D/A nonlinearity	21,22,23,24	b	a	a	a	a	a	a	a	a	a	b	5	2	FF	FF	FF	FF	00	00	08				Vari able	Vari able	Vari able	Vari able	-1.0	-	1.0	LSB	

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- Note1) Measuring conditions are as listed in supplementary Table. Measured with a current meter at test point IE
- Note2) Measuring conditions are as listed in supplementary Table. Measured with a current meter at test point I/
- Note3) Measuring conditions are as listed in supplementary Table. Measured with a current meter at test point IE
- Note4) It makes the amplitude of SG1 1.4p-p. Measure the DC voltage of the white level of the waveform output. The measured value is called Vomax.



- Note5) Increase the input signal(SG1) amplitude gradually, starting from 0.7Vp-p. Measure the amplitude of the input signal when the output signal starts becoming distorted.
- Note6) Input SG1, and measure the amplitude output at OUT(26,28,30). The amplitude is called VOUT(26,28,30) Maximum gain GV is calculated by the equation below:

$$GV = 20 \text{ LOG } (VOUT / 0.7) \text{ (dB)}$$
- Note7) Relative maximum gain ΔGV is calculated by the equation below:

$$\Delta GV = VOUT(26) / VOUT(28) , VOUT(28) / VOUT(30) , VOUT(30) / VOUT(26)$$
- Note8) Input SG1, and measure the amplitude output at OUT(26,28,30). The amplitude is called VOUT(26,28,30) The measured value is called VC1.
- Note9) Relative characteristics $\Delta VC1$ is calculated by the equation below:

$$\Delta VC1 = VOUT(26) / VOUT(28) , VOUT(28) / VOUT(30) , VOUT(30) / VOUT(26)$$
- Note10) Measuring condition and procedure are the same as described in Note8.
- Note11) Measuring condition and procedure are the same as described in Note9.
- Note12) Measuring condition and procedure are the same as described in Note8.
- Note13) Relative characteristics $\Delta VC3$ is calculated by the equation below:

$$\Delta VC3 = VOUT(26) - VOUT(28) , VOUT(28) - VOUT(30) , VOUT(30) - VOUT(26)$$
- Note14) Input SG1, and measure the amplitude output at OUT(26,28,30). The amplitude is called VOUT(26,28,30) The measured value is called VSC1.
- Note15) Relative characteristics $\Delta VSC1$ is calculated by the equation below:

$$\Delta VSC1 = VOUT(26) / VOUT(28) , VOUT(28) / VOUT(30) , VOUT(30) / VOUT(26)$$
- Note16) Measuring condition and procedure are the same as described in Note14.
- Note17) Measuring condition and procedure are the same as described in Note15.
- Note18) Measuring condition and procedure are the same as described in Note14.
- Note19) Relative characteristics $\Delta VSC3$ is calculated by the equation below:

$$\Delta VSC3 = VOUT(26) - VOUT(28) , VOUT(28) - VOUT(30) , VOUT(30) - VOUT(26)$$

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Note20) Measure the amplitude output at OUT(26,28,30). The amplitude is called VOUT(26,28,30). The measured value is ABL1.

Note21) Relative characteristics $\Delta ABL1$ is calculated by the equation below:

$$\Delta ABL1 = VOUT(26) / VOUT(28) , VOUT(28) / VOUT(30) , VOUT(30) / VOUT(26)$$

Note22) Measuring condition and procedure are the same as described in Note20.

Note23) Measuring condition and procedure are the same as described in Note21.

Note24) Measuring condition and procedure are the same as described in Note20.

Note25) Relative characteristics $\Delta ABL3$ is calculated by the equation below:

$$\Delta ABL3 = VOUT(26) - VOUT(28) , VOUT(28) - VOUT(30) , VOUT(30) - VOUT(26)$$

Note26) Measure the DC voltage at OUT(26,28,30). The amplitude is called VOUT(26,28,30). The measured value is called VB1.

Note27) Relative characteristics $\Delta VB1$ is calculated by the equation below:

$$\Delta VB1 = VOUT(26) - VOUT(28) , VOUT(28) - VOUT(30) , VOUT(30) - VOUT(26)$$

Note28) Measuring condition and procedure are the same as described in Note26.

Note29) Measuring condition and procedure are the same as described in Note27.

Note30) Measuring condition and procedure are the same as described in Note26.

Note31) Measuring condition and procedure are the same as described in Note27.

Note32) Measure the time needed for the input pulse to rise from 10% to 90% (Tr1) and for the output pulse to rise from 10% to 90% (Tr2) with an active probe.
 Pulse characteristics Tr is calculated by the equations below:

$$Tr = \sqrt{(Tr2)^2 - (Tr1)^2} \text{ (nS)}$$

Note33) Relative characteristics ΔTr is calculated by the equation below:

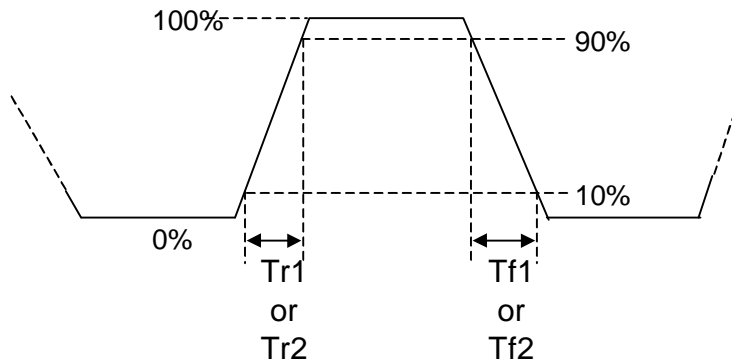
$$\Delta Tr = Tr(26) - Tr(28) , Tr(28) - Tr(30) , Tr(30) - Tr(26)$$

Note34) Measure the time needed for the input pulse to fall from 90% to 10% (Tf1) and for the output pulse to fall from 90% to 10% (Tf2) with an active probe.
 Pulse characteristics Tf is calculated by the equations below:

$$Tf = \sqrt{(Tf2)^2 - (Tf1)^2} \text{ (nS)}$$

Note35) Relative characteristics ΔTf is calculated by the equation below:

$$\Delta Tf = Tf(26) - Tf(28) , Tf(28) - Tf(30) , Tf(30) - Tf(26)$$



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- Note36) Decrease the SG5 input level gradually from 5.0Vp-p, monitoring the waveform output. Measure the top level of input pulse when the output pedestal voltage turn decrease with unstable. And increase the SG5 input level gradually from 0Vp-p. Measure the top level of input pulse when the output pedestal voltage turn increase with stable (a point of 2.0V). The measured value is called VthCP.
- Note37) Decrease the SG5 pulse width gradually from 0.5uS, monitoring the output. Measure the SG5 pulse width when the output pedestal voltage turn decrease with unstable. And increase the SG5 pulse width gradually from 0uS. Measure the SG5 pulse width when the output pedestal voltage turn increase with stable (a point of 2.0V). The measured value is called WCP.
- Note38) Measure the time needed for the output pulse to rise from 10% to 90% (OTr) with an active probe.
- Note39) Measure the time needed for the output pulse to fall from 90% to 10% (OTf) with an active probe.
- Note40) Measure the amplitude output at OUT(26,28,30). The amplitude is called VOUT(26,28,30). The measured value is called Oadj1.
- Note41) Relative characteristics $\Delta Oadj1$ is calculated by the equation below:

$$\Delta Oadj1 = VOUT(26) / VOUT(28) , VOUT(28) / VOUT(30) , VOUT(30) / VOUT(26)$$
- Note42) Measuring condition and procedure are the same as described in Note40.
- Note43) Measuring condition and procedure are the same as described in Note41.
- Note44) Measuring condition and procedure are the same as described in Note40.
- Note45) Relative characteristics $\Delta Oadj3$ is calculated by the equation below:

$$\Delta Oadj3 = VOUT(26) - VOUT(28) , VOUT(28) - VOUT(30) , VOUT(30) - VOUT(26)$$
- Note46) Decrease the SG6 input level gradually from 5.0Vp-p, monitoring the output. Measure the top level of SG6 when the output is disappeared. And increase the SG6 input level gradually from 0Vp-p. Measure the top level of SG6 when the output is appeared. The measured value is called VthOSD.
- Note47) Calculating the black level voltage minus the output voltage of high section of SG6 it makes VOUT(26,28,30). The calculated value is called OBLK.
- Note48) Relative characteristics $\Delta OBLK$ is calculated by the equation below:

$$\Delta OBLK = VOUT(26) - VOUT(28) , VOUT(28) - VOUT(30) , VOUT(30) - VOUT(26)$$
- Note50) Confirm that output signal is being blanked by the SG6 at the time.
 Decrease the SG6 input level gradually from 5.0Vp-p, monitoring the output. Measure the top level of SG6 when the blanking period is disappeared. And increase the SG6 input level gradually from 0Vp-p. Measure the top level of SG6 when the blanking period is appeared. The measured value is called VthBLK.
- Note51) Measure the bottom voltage at amplitude of OUT(26,28,30). The measured value is called HBLK1.
- Note52) Measuring condition and procedure are the same as described in Note51.
- Note53) Measuring condition and procedure are the same as described in Note51.
- Note54) Decrease the SG7 input level gradually from 5.0Vp-p, monitoring the output. Measure the top level of SG7 when the output is disappeared. And increase the SG7 input level gradually from 0Vp-p. Measure the top level of SG7 when the output is appeared. The measured value is called VthHBLK.

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Note55) When SG4 is all black (no video), the sync's amplitude of SG4 gradually from 0Vp-p to 0.02Vp-p. No pulse output permitted.

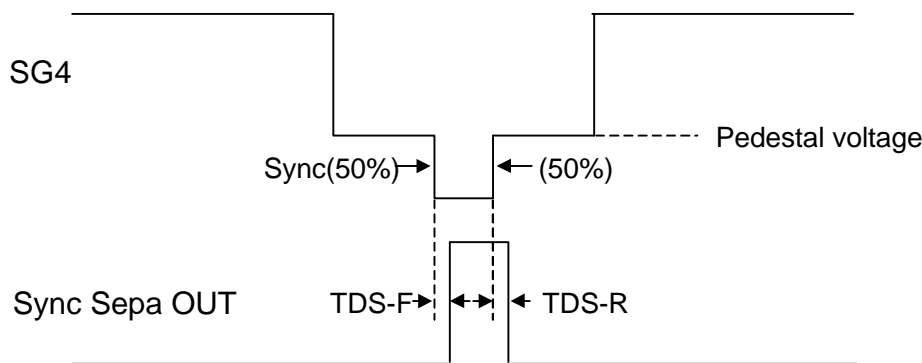
Note56) When SG4 is all white or all black, the sync's amplitude of SG4 gradually from 0.2Vp-p to 0.3Vp-p. Positive pulse has occurred to Sync Sepa OUT.

Note57) Measure the high voltage at Sync Sepa OUT. The measured value is treated as VSH.

Note58) Measure the low voltage at Sync Sepa OUT. The measured value is treated as VSL.

Note59) Sync Sepa OUT becomes high with sink part of SG4.
Measure the time needed for the front edge of SG4 Sync to fall from 50% and for SyncOUT to rise from 50% with an active probe. The measured value is called TDS-F.

Note60) Sync Sepa OUT becomes high with sink part of SG4.
Measure the time needed for the rear edge of SG4 Sync to rise from 50% and for SyncOUT to fall from 50% with an active probe. The measured value is called TDS-R.



Note61) Increase the SG1 input level gradually from 0Vp-p to 0.05Vp-p. No pulse Video Det OUT permitted.

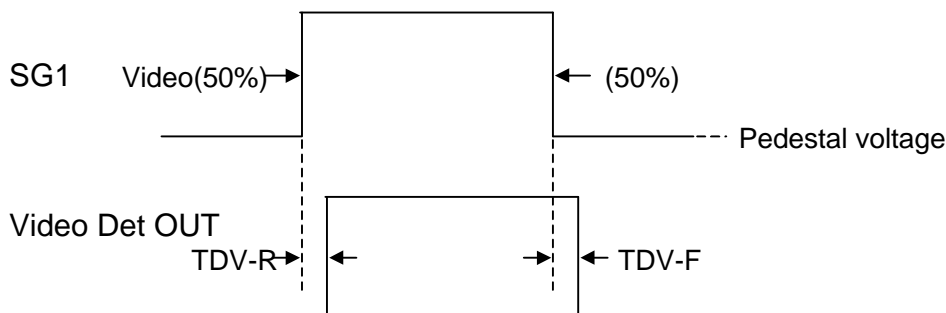
Note62) Decrease the SG1 input level gradually from 0.2p-p to 0.3Vp-p. Positive pulse has occurred to Video Det OUT

Note63) Measure the high voltage at Video Det OUT. The measured value is treated as VVDH.

Note64) Measure the low voltage at Video Det OUT. The measured value is treated as VVDL.

Note65) Video Det OUT becomes high with signal part of SG1.
Measure the time needed for the SG1 to fall from 50% and for Video Det OUT to fall from 50% with an active probe. The measured value is called TDV-F.

Note66) Video Det OUT becomes high with signal part of SG1.
Measure the time needed for the SG1 to rise from 50% and for Video Det OUT to rise from 50% with an active probe. The measured value is called TDV-R.



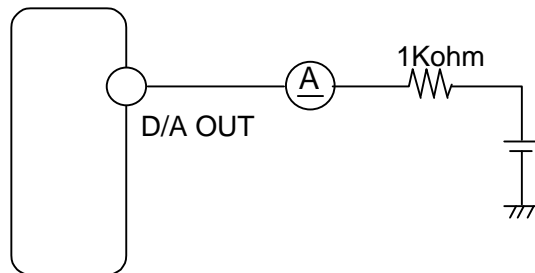
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Note68) Measure the DC voltage at D/A OUT. The measured value is called VDL.

Note69) Measure the input current that flows into D/A OUT through 1Kohm by 2VDC.

Note70) Measure the input current that flows into D/A OUT through 1Kohm by 0.5VDC.

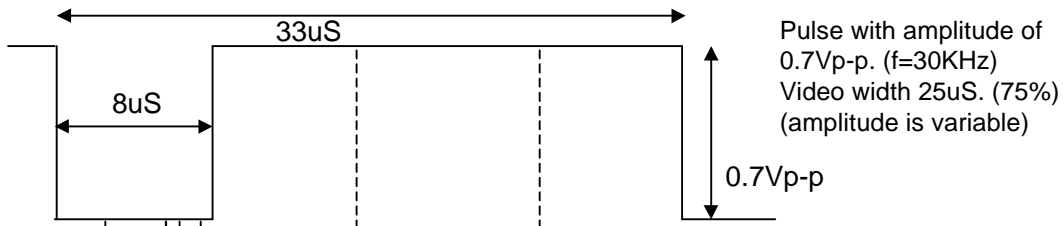
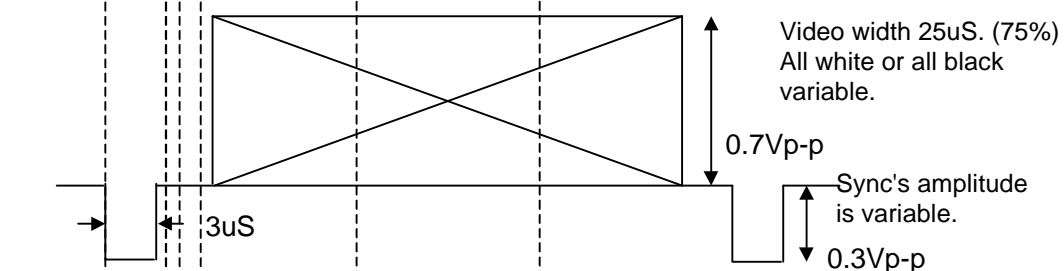

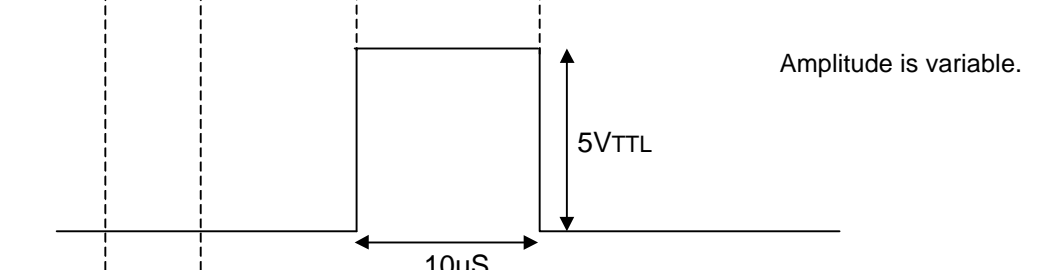

Note71) Measure the output current that flows out of D/A OUT through 1Kohm by 4.2VDC.



Note72) The difference of differential non-linearity of D/A OUT must be less than ± 1.0 LSB.

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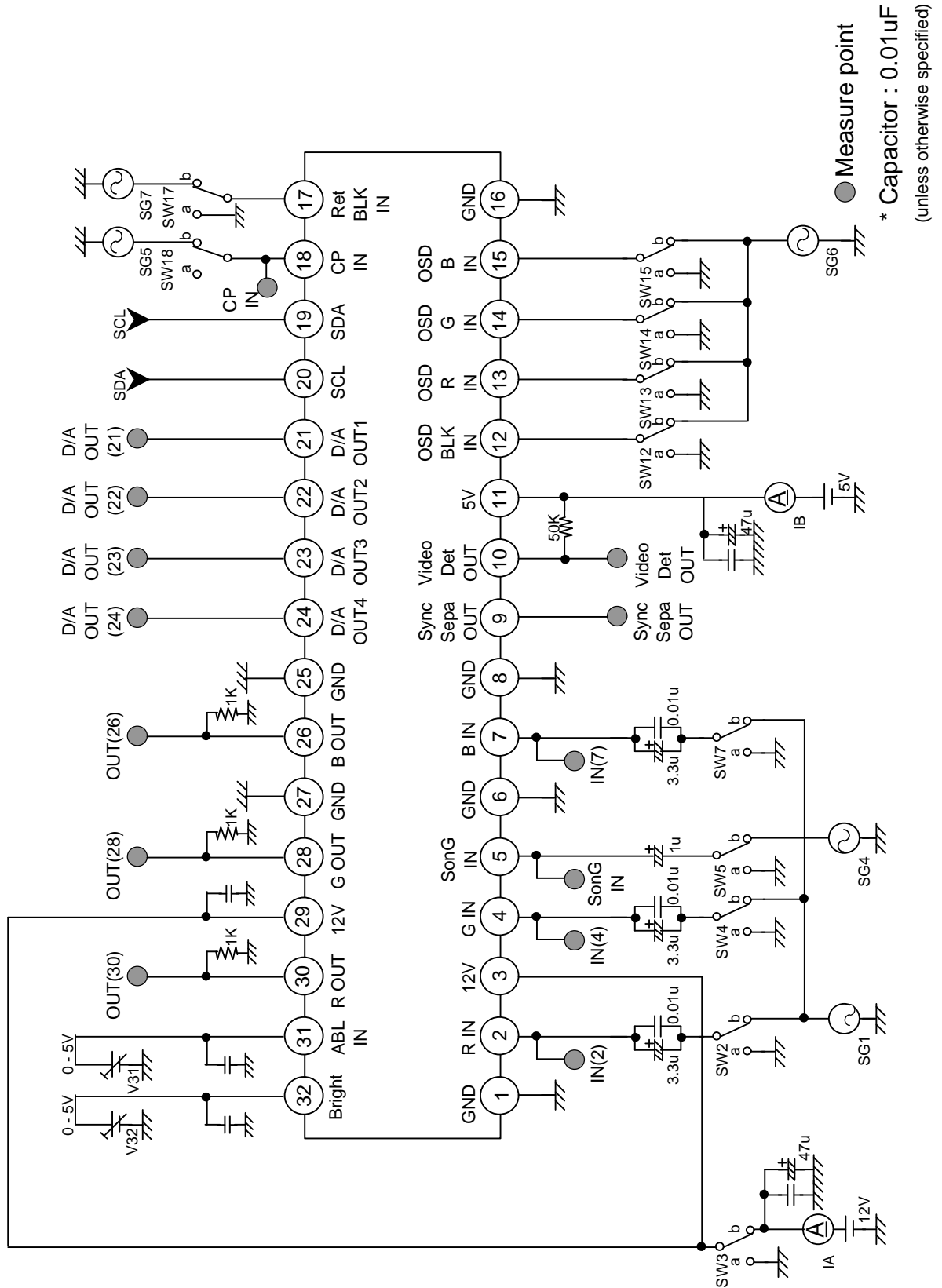
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SG No.	Input signal
<p>SG1 Video signal (all white)</p>	 <p>Pulse with amplitude of 0.7Vp-p. (f=30KHz) Video width 25µs. (75%) (amplitude is variable)</p>
<p>SG4 Video Signal (all white, all black)</p>	 <p>Video width 25µs. (75%) All white or all black variable.</p> <p>0.7Vp-p</p> <p>3µs</p> <p>0.3Vp-p</p> <p>Sync's amplitude is variable.</p>
<p>SG5 Clamp pulse</p>	 <p>0.5µs</p> <p>5VTTL</p> <p>Pulse width and amplitude are variable.</p>
<p>SG6 OSD pulse</p>	 <p>10µs</p> <p>5VTTL</p> <p>Amplitude is variable.</p>
<p>SG7 BLK pulse</p>	 <p>5µs</p> <p>5VTTL</p> <p>Amplitude is variable.</p>

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TEST CIRCUIT



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I²C BUS CONTROLLED VIDEO PRE-AMP FOR HIGH RESOLUTION COLOR DISPLAY

TERMINAL DESCRIPTION

No.	Name	DC Voltage(V)	Peripheral Circuit of pins	Remark
2 4 7	R IN G IN B IN	3.5		Clamp to about 3.5V due to clamp pulse from Pin18. Input at low impedance.
3	VCC 1 (12V)	12		Connect to the power supply that stabilized.
5	SonG IN	When open 2.3		SYNC ON VIDEO input pin. Sync is negative. Input signal at Pin5, compare with the reference voltage of internal circuit in order to separate Sync signal from Sync on Green signal. Input at low impedance. Do not input the signal without the Sync. When it does not use this function, connect to capacitor between GND, turn on Sync Sepa SW by IIC BUS.
1 6 8 16 27	GND GND 1 GND 2 GND 3 GND 4	GND		Connect to GND.
9	Sync Sepa OUT	-		Sync Sepa output pin. When the rise time of the signal is sped up, connect about 2.3 Kohm between 5V power supply. When it does not use, do openly. So as not to flow into Pin9 8mA over, resistance value does not make to 2.3Kohm or under. Output is a positive.
10	Video Det OUT	-		Pin10 needs to connect the 50Kohm between 5V power supply. When it does not use this function, turn off Video Det SW by IIC BUS.
11	VCC (5V)	5		Connect to the power supply that stabilized.

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No.	Name	DC Voltage(V)	Peripheral Circuit of pins	Remark
12 13 14 15	OSD BLK IN OSD R IN OSD G IN OSD B IN			<p>Input the positive pulse.</p> <p>3.5 --- 5V 1.5V --- GND</p> <p>When it does not use this function, connect to GND. When input OSD RGB pulse, input OSD BLK pulse without fail.</p>
17	Retrace BLK IN	-		<p>Input the positive pulse.</p> <p>2.5 --- 5V 0.5V --- GND</p> <p>When it does not use this function, connect to GND.</p>
18	Clamp Pulse IN	-		<p>Input the positive pulse which width 200nS over. Input at low impedance.</p> <p>2.5 --- 5V 0.5V --- GND</p>
19	SDA	-		<p>SDA of IIC BUS. (Serial data line)</p> <p>Tth = 2.3V</p>

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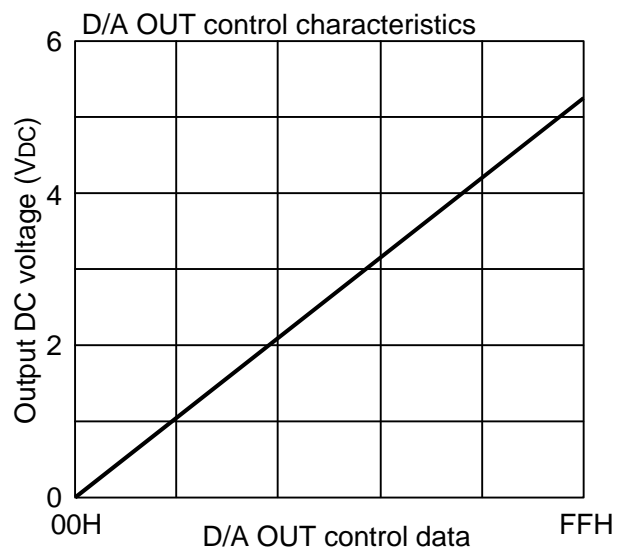
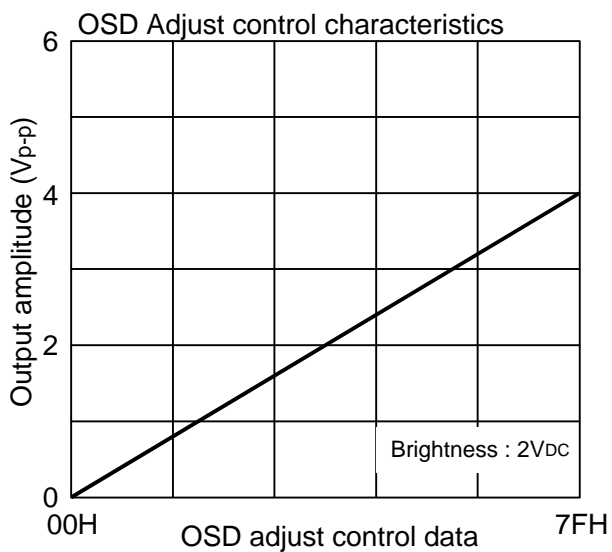
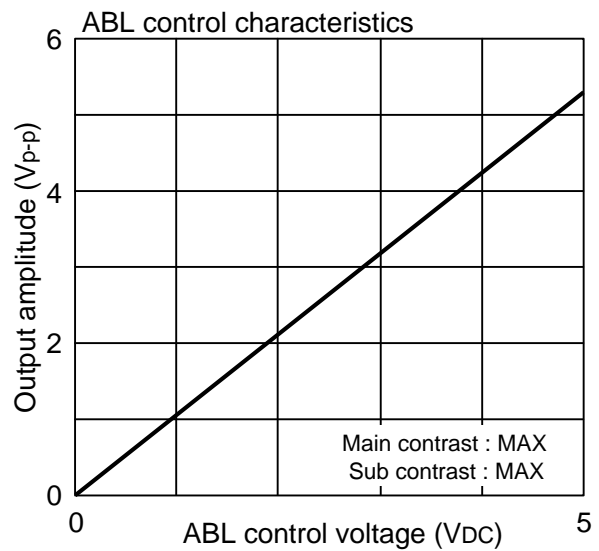
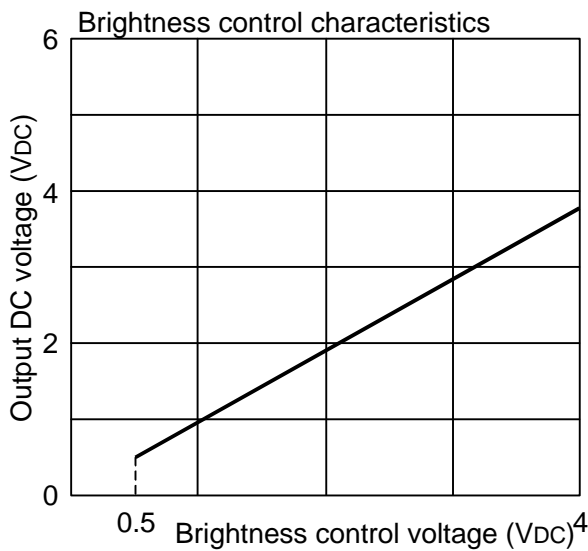
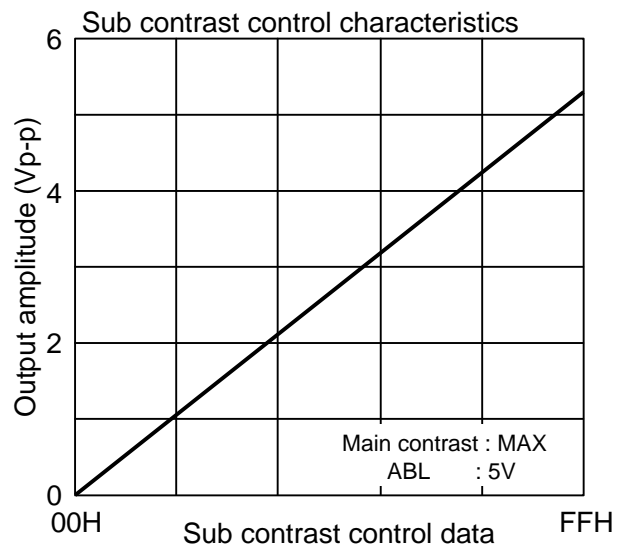
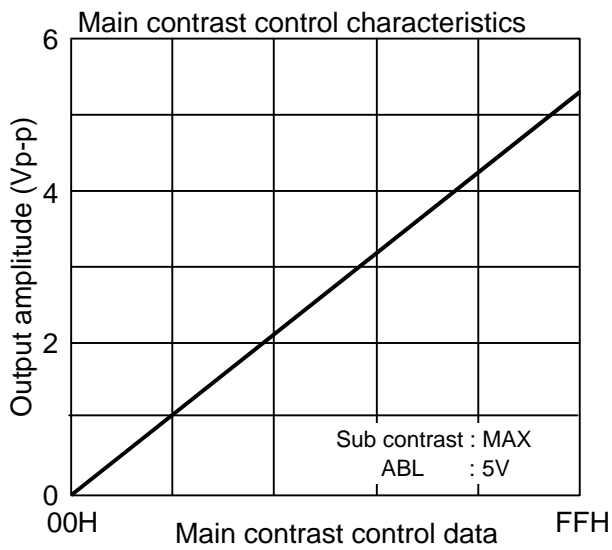
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No.	Name	DC Voltage(V)	Peripheral Circuit of pins	Remark
20	SCL	-		<p>SCL of IIC BUS. (Serial clock line)</p> <p>Tth = 2.3V</p>
21	D/A OUT 1			<p>D/A output pin. Output voltage ranges is 0V to 5V. Input current is below 0.18mA. Output current is below 0.4mA.</p>
22	D/A OUT 2			
23	D/A OUT 3			
24	D/A OUT 4			
26	B OUT	Variable		<p>This terminal needs to connect the 1 to 3Kohm resistor between GND. This resistance value may be changed, to improve the video output characteristics.</p>
28	G OUT			
30	R OUT			
27	GND 4			Connect to GND.
29	VCC 2 (12V)	12		It is the power supply of emitter follower of RGB output exclusive use.
31	ABL IN	When open 2.5V		<p>ABL (Automatic beam limiter) input pin. Input voltage in the ranges of 0V to 5V. Output amplitude MAX with 5V. Output amplitude MIN with 0V. When it does not use this function, connect to 5V.</p>
32	BRIGHT	-		It is recommended that the IC is used between pedestal voltage 2V to 3V.
25	NC	-		Connect to GND.

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ELECTRICAL CHARACTERISTICS (Reference data)



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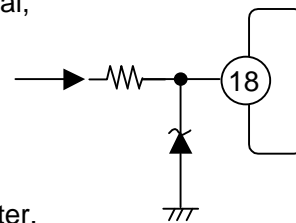
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APPLICATION METHOD FOR M61311SP/M61316SP

ABOUT CLAMP PULSE INPUT

Clamp pulse needs to be always inputted.
 Clamp pulse width is recommended :
 15KHz at 1.0 uS over
 30KHz at 0.5 uS over
 64KHz at 0.3 uS over

The clamp pulse circuit in ordinary set is a long round about way, and beside high voltage, sometimes connect to external terminal, it is very easy affected by large surge. Therefore, the fig. shown right is recommended.



NOTICE OF APPLICATION

Make the nearest distance between output and pull down resistor.
 Recommend this resistor is 1to 3 Kohm.
 Power dissipation in 3Kohm is smaller than 1Kohm.

Recommend pedestal voltage of IC output signal is 2V.

As for the low level of the pulse input of OSD BLK, OSD, Clamp Pulse, Retrace BLK etc., avoid cons the GND level or under.

PIN31 connect to the voltage that stabilized, and pay attention as surge etc. does not flow into.

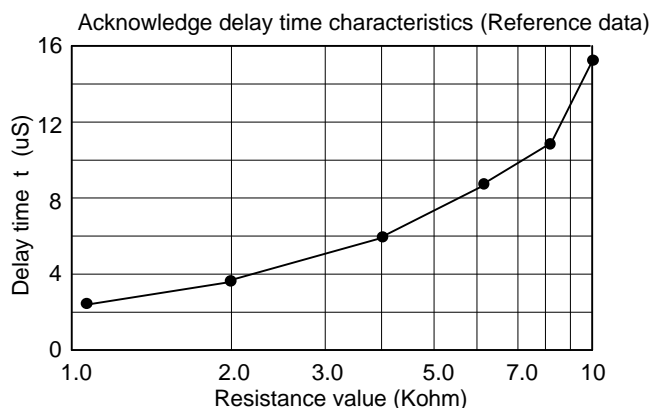
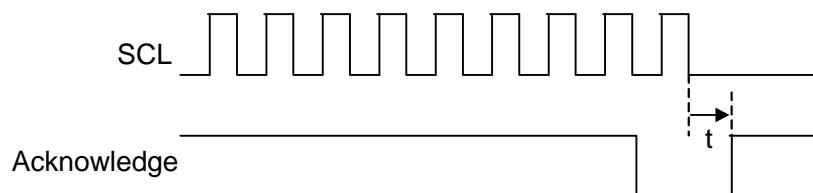
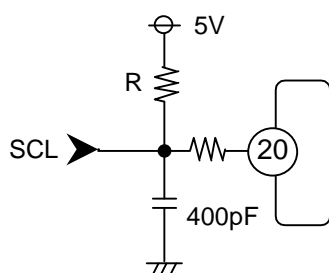
VCC(12V,5V) connects to the power supply that stabilized, and bypass-capacitor connects near the term When capacitor is connected to Pin29, it sometimes oscillates. Do not connect capacitor to Pin29.

Connect to bypass-capacitance of the DC line near the terminal.

Connect to the NC Pin to GND.

The time(t) is from fall of 9bit of SCL to rise of Acknowledge.

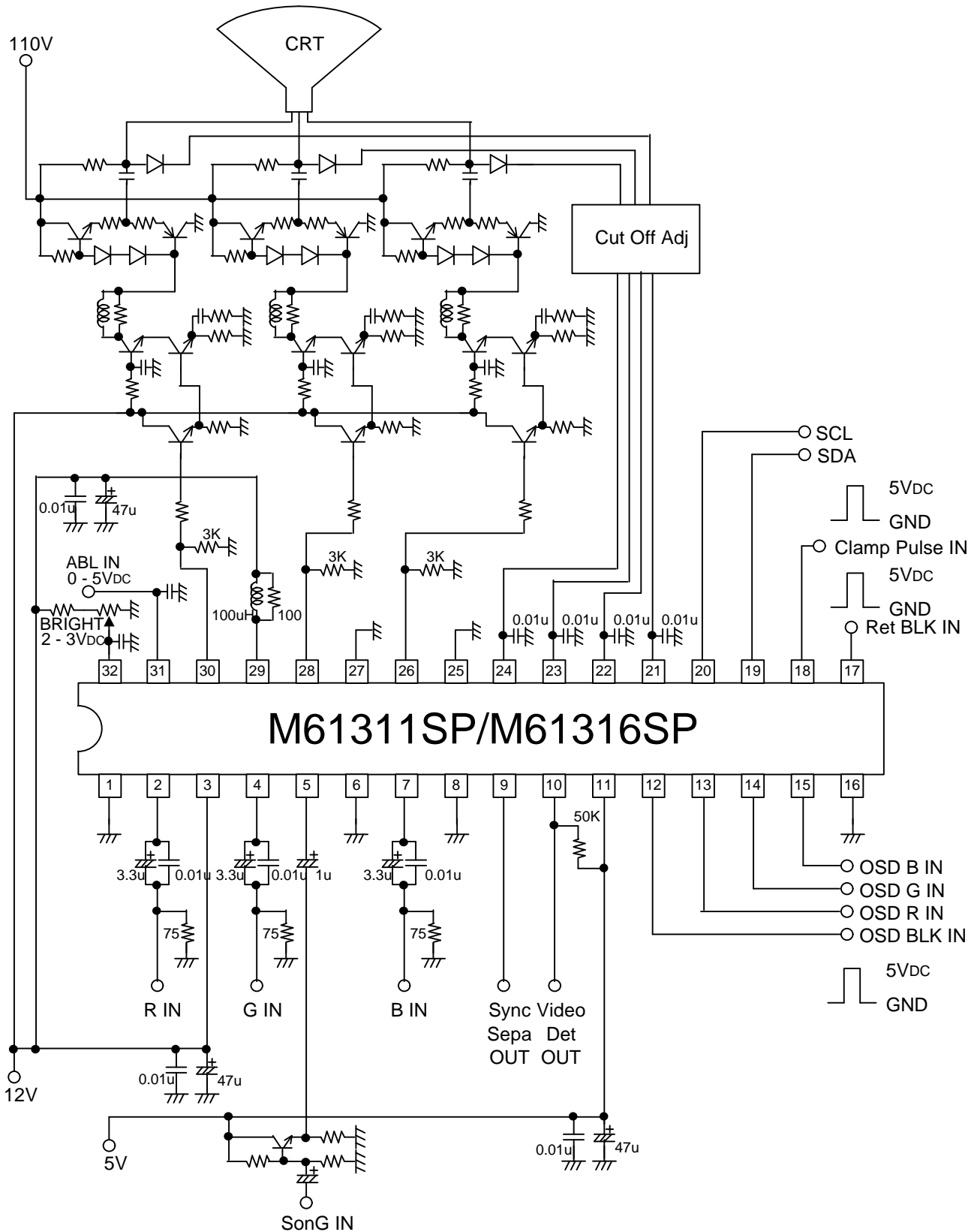
About the forwarding of IIC BUS, the time(t) changes with the resistance that connected outside. The next SCL does not overlap into this time(t).



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APPLICATION EXAMPLE



"Purchase of Mitsubishi electric corporation's IIC components conveys a license under the Philips IIC Patent Rights to use these components in an IIC system, provided that the system conforms the IIC Standard Specification as defined by PI

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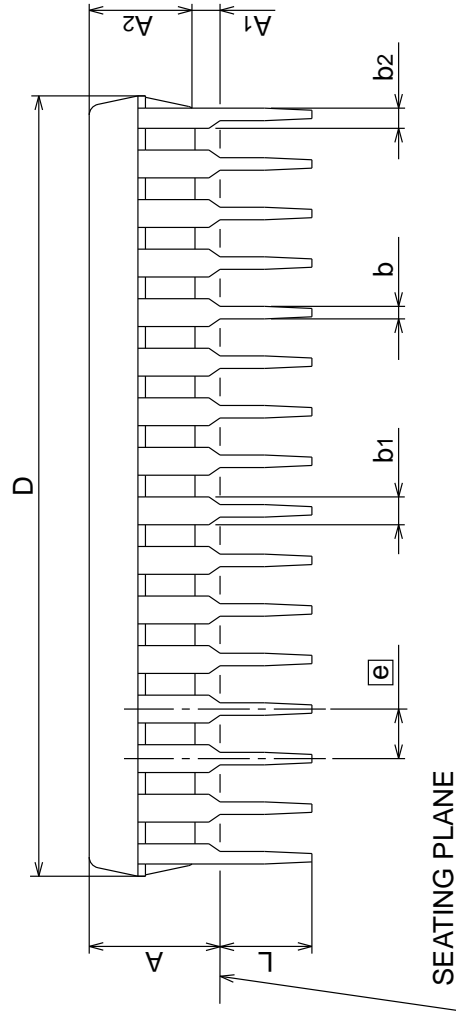
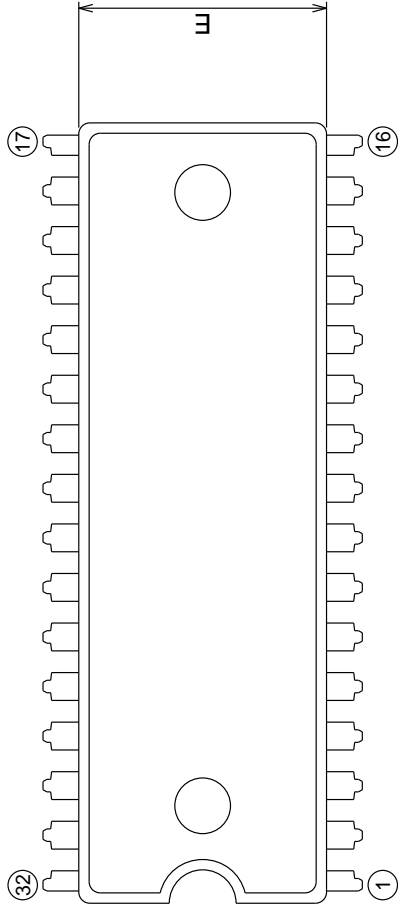
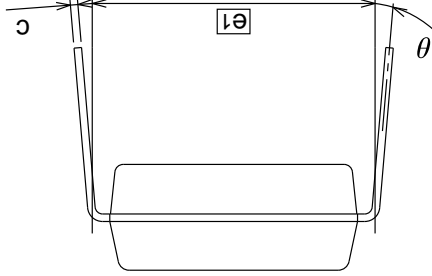
I²C BUS CONTROLLED VIDEO PRE-AMP FOR HIGH RESOLUTION COLOR DISPLAY

DETAILED DIAGRAM OF PACKAGE OUTLINE

Plastic 32pin 400mil SDIP

32P4B

EIAJ Package Code SDIP32-P-400-1.78	JEDEC Code -	Weight(g) 2.2	Lead Material Alloy 42/Cu Alloy
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Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	5.08
A1	0.51	-	-
A2	-	3.8	-
b	0.35	0.45	0.55
b1	0.9	1.0	1.3
b2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	-	1.778	-
e1	-	10.16	-
L	3.0	-	-
θ	0°	-	15°

I²C BUS CONTROLLED VIDEO PRE-AMP FOR HIGH RESOLUTION COLOR DISPLAY

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