FAIRCHILD SEMICONDUCTOR®

October 2013

FAH4840
Haptic Driver for Linear Resonant Actuators (LRAs)

Features

- Direct Drive of LRA (Linear Resonant Actuator)
- External PWM Input (10 kHz to 250 kHz) with Divider
- Internal Motor Enable / Disable Input
- Auto Resonant Tracking
- LDO Provides Stable Haptic Effect with Battery Depletion
- Low Shutdown Current: < 5 nA
- Fast Wake-Up Time
- Nearly Rail-to-Rail Output Swing
- Thermal Shutdown, Over-Current Shutdown
- Register-Based Control by I^2C
- Immersion TouchSense® 3000 Certified
- Package: 8- Lead MicroPak™ MLP

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Description

The FAH4840 is a high-performance amplifier for mobile phones and other hand-held devices. The haptic driver takes a single-ended PWM input signal to control a Linear Resonant Actuator (LRA). The device utilizes an external 10 kHz to 250 kHz PWM signal capable of meeting the wide range of resonant frequencies needed for an LRA haptics applications. The FAH4840 register map is accessible through an I^2C serial communication port.

Applications

- Mobile Phones
- Handheld Devices
- Any Key pad interface

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package	Packing Method	Quantity
FAH4840L8X	YB	-40°C to +85°C	MicroPak™ MLP	Reel	5000

Block Diagram

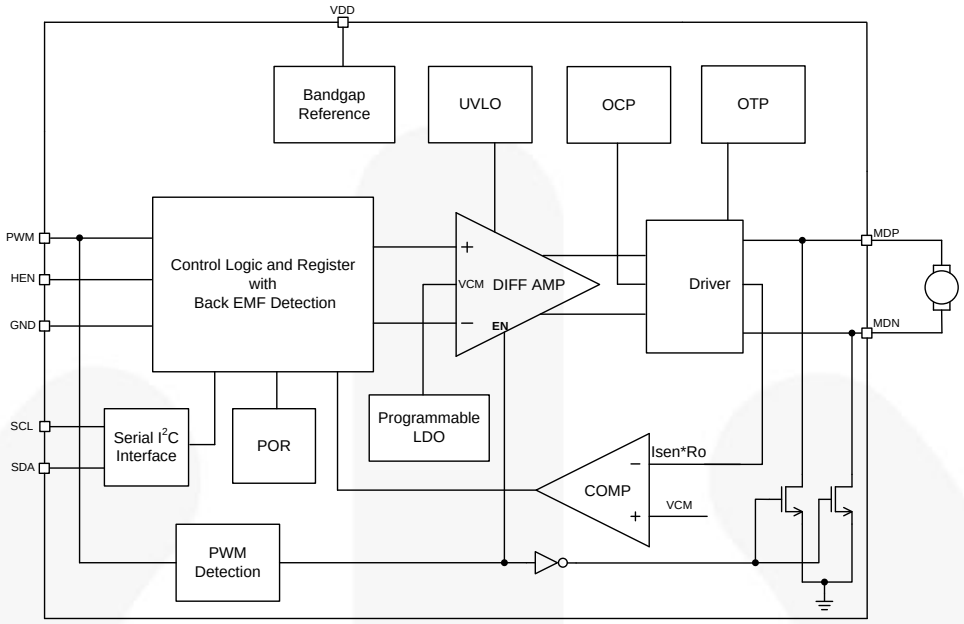


Figure 1. Block Diagram

Pin Configuration

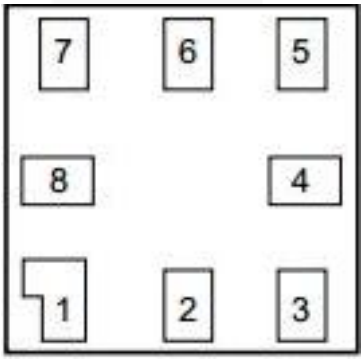


Figure 2. Pin Assignments (MicroPak MLP)

Pin Definitions

Name	Pin #	Type	Description
SDA	1	Input	I^2C data input
VDD	2	Power	Power
MDN	3	Output	Negative motor driver output
MDP	4	Output	Positive motor driver output
GND	5	Power	Ground
PWM	6	Input	PWM input
SCL	7	Input	I^2C clock input
HEN	8	Input	Haptic motor enable/disable (HIGH: enable, LOW: disable)

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O (All Input and Output Pins)	-0.3	V_{CC}+0.3	V

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C

Electrostatic Discharge Information

Symbol	Parameter	Max.	Unit
ESD	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	4	kV
	Charged Device Model, JESD22-C101	1	
Latch-Up	Test Condition for Latch-Up Current	±150	mA

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		+85	°C
V_{DD}	Supply Voltage Range	2.5	3.3	4.3	V
Z_{LOAD}	Load impedance	15	25	50	Ω

Dissipation Ratings

This thermal data is measured with a high-K board (four-layer board, according to the JESD51-7 JEDEC standard.)

Package	Θ_{JA}	Unit
8-Lead MicroPak MLP	280	°C/W

DC Electrical Characteristics

T_A = 25°C, V_{DD} = 3.3 V, V_{REG}=2.0 V, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{IPWM}	PWM Input Frequency	Square Wave Input	10		250	kHz
IIH_{PWM}	Input Current	PWM = 1.8 V		1	3	µA
IIH_{HEN}	Input Current	HEN = 1.8 V		1	3	µA
IIL_{PWM}	Input Current	PWM = 0 V		1	3	µA
IIL_{HEN}	Input Current	HEN = 0 V		1	3	µA
V_{IH}	Input Logic HIGH (HEN, PWM)		1.15			V
V_{IL}	Input Logic LOW (HEN, PWM)				0.5	V
C_{IN}	Input Capacitance	PWM Capacitance to GND or 1.8 V		6	10	pF
V_{OL}	Output Voltage	V_{DD}=3.3 V, R_L=15 Ω, V_{OL}=$V_{OL(measure)}$-(V_{CM}-V_{REG}/2), *See Waveforms Below*		0.02		mV
V_{OH}	Output Voltage	V_{DD}=3.3 V, R_L=15 Ω, V_{OH}=$V_{OH(measure)}$-(V_{CM}-V_{REG}/2), *See Waveforms Below*		1.95		V
I_{OUT}	Output Drive Current	V_{DD}=3.3 V, V_{REG}=3.0 V, R_L = 15 Ω		200		mA
I_{OUTSCP}	Short-Circuit Protection	V_{DD}=3.3 V, V_{REG}=3.0 V, MDP and MDN Shorted Together and Each Shorted to Ground		350	400	mA
I_{DD1}	Supply Current	PWM=22.4 kHz 50% Duty, HEN = HIGH, R_L= No Load		2	5	mA
I_{DD2}	Supply Current	PWM=22.4 kHz 90/10% Duty, HEN = HIGH, R_L= 25 Ω		77		mA
I_{DD3}	Supply Current	PWM,HEN = 0 V, R_L= 25 Ω		15		µA
I_{DD4}	Supply Current	PWM, HEN=0 V, V_{DD}=2.5 V, Address 0 Bit 7 Set to Zero		2.0		nA
V_{REG}	Output Voltage Range	Measure V_{REG} , V_{DD} per Table	1.4	2.0	3.2	V
V_{REGA}	Output Voltage Accuracy	Measure V_{REG}	-2.5		2.5	%

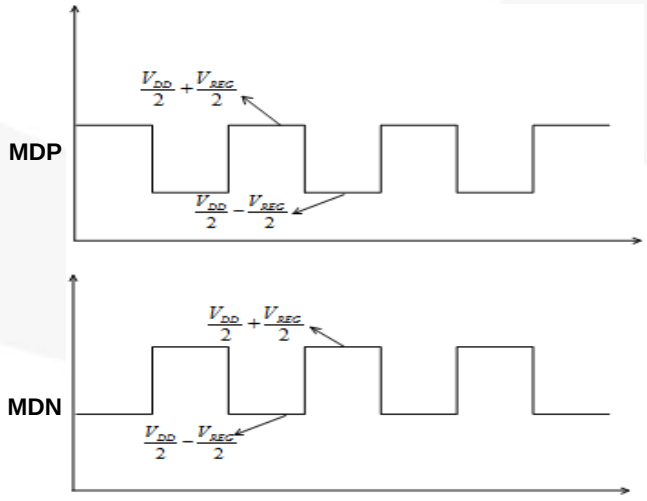


Figure 3. Output Waveforms

AC Electrical Characteristics

T_A = 25°C, V_{DD} = 3.3 V, V_{REG}=2.0 V, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{WU}	Wake-Up Time	PWM=80/20% Duty Cycle, HEN/PWM LOW to HIGH, Measurement Point PWM = 50%, Output Point = 90%		1	150	µs
t_{SD}	Shutdown Time	PWM=80/20% Duty Cycle, HEN HIGH to LOW, Measurement Point HEN = 50%, Output Point = 90%		0.2	150.0	µs
Restrk	Auto Resonance Tracking	PWM=22.4 kHz 80/20% Duty, R_L= 25 Ω	-2.5		2.5	Hz

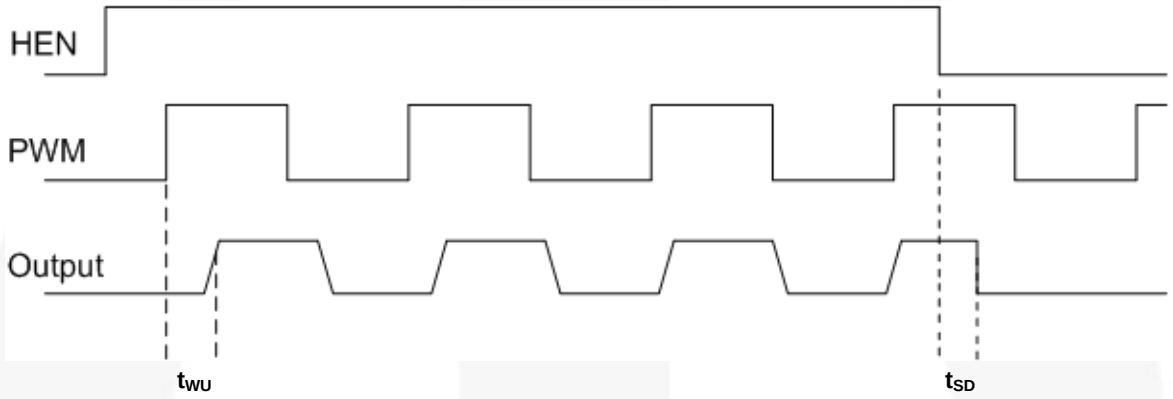


Figure 4. Haptic Enable / Disable Functional Timing

Table 1. V_{DD} vs. V_{REG} Supply Values

V_{REG_OUT} (Programmed Voltage)	V_{DD} (V)			
	2.5	2.7	3.0	3.3
	1.4	1.4	1.4	1.4
	1.6	1.6	1.6	1.6
	1.8	1.8	1.8	1.8
	2.0	2.0	2.0	2.0
	2.2	2.2	2.2	2.2
	2.4	2.4	2.4	2.4
		2.6	2.6	2.6
			2.8	2.8
				3.0
				3.2

I²C DC Electrical Characteristics

T_A = 25°C, V_{DD} = 3.3 V, V_{REG}=2.0 V, unless otherwise noted.

Symbol	Parameter	Fast Mode (400 kHz)		
		Min.	Max.	Unit
V_{IL}	Low-Level Input Voltage	-0.3	0.6	V
V_{IH}	High-Level Input Voltage	1.3		V
V_{OL}	Low-Level Output Voltage at 3 mA Sink Current (Open-Drain or Open-Collector)	0	0.4	V
I_{IH}	High-Level Input Current of Each I/O Pin, Input Voltage=V_{SVDD}	-1	1	µA
I_{IL}	Low-Level Input Current of Each I/O Pin, Input Voltage=0 V	-1	1	µA

I²C AC Electrical Characteristics

T_A = 25°C, V_{DD} = 3.3 V, V_{REG}=2.0 V, unless otherwise noted.

Symbol	Parameter	Fast Mode (400 kHz)		
		Min.	Max.	Unit
f_{SCL}	SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		µs
t_{LOW}	Low Period of SCL Clock	1.3		µs
t_{HIGH}	High Period of SCL Clock	0.6		µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		µs
$t_{HD;DAT}$	Data Hold Time	0	0.9	µs
$t_{SU;DAT}$	Data Set-up Time(1)	100		ns
t_r	Rise Time of SDA and SCL Signals(2)	20+0.1C_b	300	ns
t_f	Fall Time of SDA and SCL Signals(2)	20+0.1C_b	300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	0.6		µs
t_{BUF}	BUS-Free Time between STOP and START Conditions	1.3		µs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Notes:

1. A Fast-Mode I²C Bus® device can be used in a Standard-Mode I²C bus system, but the requirement $t_{SU;DAT}$ ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the Serial Data (SDA) line t_{r_max} + $t_{SU;DAT}$=1000 + 250=1250 ns (according to the Standard-Mode I²C Bus specification) before the SCL line is released.
2. C_b equals the total capacitance of one bus line in pf. If mixed with High-Speed Mode devices, faster fall times are allowed according to the I²C specification.

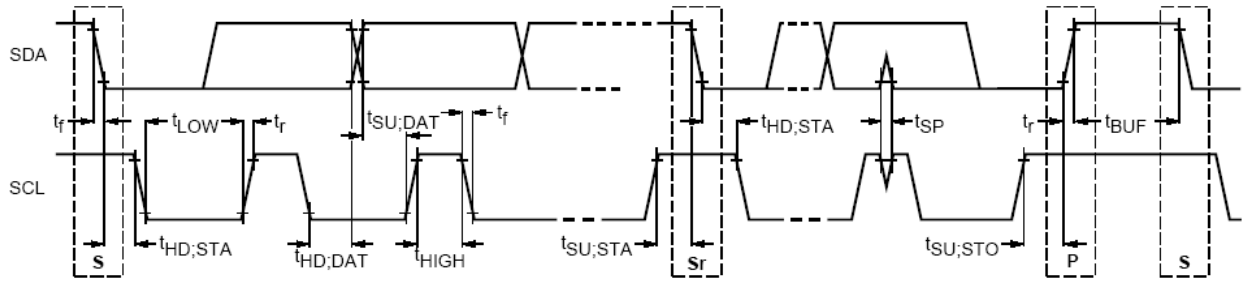


Figure 5. Definition of Timing for Full-Speed Mode Devices on the I²C Bus

Functional Description

I²C Control

Writing to and reading from registers is accomplished via the I²C interface. The I²C protocol requires that one device on the bus initiates and controls all read and write operations. This device is called the "master" device. The master device generates the SCL signal, which is the clock signal for all other devices on the bus. All other devices on the bus are called "slave" devices. The FAH4840 is a slave device. Both the master and slave devices can send and receive data on the bus.

During I²C operations, one data bit is transmitted per clock cycle. All I²C operations follow a repeating nine-clock-cycle pattern that consists of eight bits (one byte) of transmitted data followed by an acknowledge (ACK) or not acknowledge (NACK) from the receiving device. There are no unused clock cycles during any operation; therefore, there must be no breaks in the stream of data and ACKs/NACKs during data transfers.

For most operations, I²C protocol requires the SDA line to remain stable (unmoving) whenever SCL is HIGH; i.e. transitions on the SDA line can only occur when SCL is LOW. The exceptions to this rule are when the master device issues a START or STOP condition. The slave device cannot issue a START or STOP condition.

START Condition: This condition occurs when the SDA line transitions from HIGH to LOW while SCL is HIGH. The master device uses this condition to indicate that a data transfer is about to begin.

STOP Condition: This condition occurs when the SDA line transitions from LOW to HIGH while SCL is HIGH. The master device uses this condition to signal the end of a data transfer.

Acknowledge and Not Acknowledge: When data is transferred to the slave device, the slave device sends acknowledge (ACK) after receiving every byte of data. The receiving device sends an ACK by pulling SDA LOW for one clock cycle.

When the master device is reading data from the slave device, the master sends an ACK after receiving every byte of data. Following the last byte, a master device sends a "not acknowledge" (NACK) instead of an ACK, followed by a STOP condition. A NACK is indicated by leaving SDA HIGH during the clock after the last byte.

Slave Address

Each slave device on the bus must have a unique address so the master can identify the device sending or receiving data. The FAH4840 slave address is 0000110X binary or 06 HEX where "X" is the read/write bit. Master write operations are indicated when X=0. Master read operations are indicated when X=1.

Writing to and Reading from the FAH4840

All read and write operations must begin with a START condition generated by the master. After the START condition, the master must immediately send a slave address (7 bits), followed by a read/write bit. If the slave address matches the address of the FAH4840, the FAH4840 sends an ACK after receiving the read/write bit by pulling the SDA line LOW for one clock cycle.

Setting the Pointer

For all operations, the pointer stored in the command register must be pointing to the register that is going to be written or read. To change the pointer value in the command register, the read/write bit following the address must be 0. This indicates that the master writes new information into the command register.

After the FAH4840 sends an ACK in response to receiving the address and read/write bit, the master must transmit an appropriate 8-bit pointer value, as explained in the I²C Registers section. The FAH4840 sends an ACK after receiving the new pointer data.

The pointer set operation is illustrated in Figure 8 and Figure 9. Any time a pointer set is performed, it must be immediately followed by a read or write operation. The command register retains the current pointer value between operations; therefore, once a register is indicated, subsequent read operations do not require a pointer set cycle. Write operations always require the pointer be reset.

Reading

If the pointer is already pointing to the desired register, the master can read from that register by setting the read/write bit (following the slave address) to 1. After sending an ACK, the FAH4840 begins transmitting data during the following clock cycle. The master should respond with a NACK, followed by a STOP condition *(see Figure 6)*.

The master can read multiple bytes by responding to the data with an ACK instead of a NACK and continuing to send SCL pulses, as shown in Figure 7, then the FAH4840 increments the pointer by one and sends the data from the next register. The master indicates the last data byte by responding with a NACK, followed by a STOP condition.

To read from a register other than the one currently indicated by the command register, a pointer to the desired register must be set. Immediately following the pointer set, the master must perform a repeated START condition *(see Figure 9)*, which indicates to the FAH4840 that a new operation is about to occur. If the repeated START condition does not occur, the FAH4840 assumes that a write is taking place and the selected register is overwritten by the upcoming data on the data bus. After the START condition, the master must again send the device address and read/write bit. This time, the read/write bit must be set to 1 to indicate a read. The rest of the read cycle is the same as described in the previous paragraphs for reading from a preset pointer location.

Writing

All writes must be preceded by a pointer set, even if the pointer is already pointing to the desired register.

Immediately following the pointer set, the master must begin transmitting the data to be written. After transmitting each byte of data, the master must release the Serial Data (SDA) line for one clock cycle to allow the FAH4840 to acknowledge receiving the byte. The write operation should be terminated by a STOP condition from the master *(see Figure 8)*.

As with reading, the master can write multiple bytes by continuing to send data. The FAH4840 increments the pointer by one and accepts data for the next register. The master indicates the last data byte by issuing a STOP condition.

Read / Write Diagrams

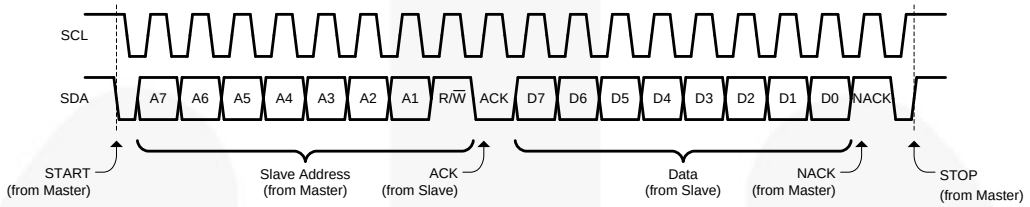


Figure 6. I²C Read

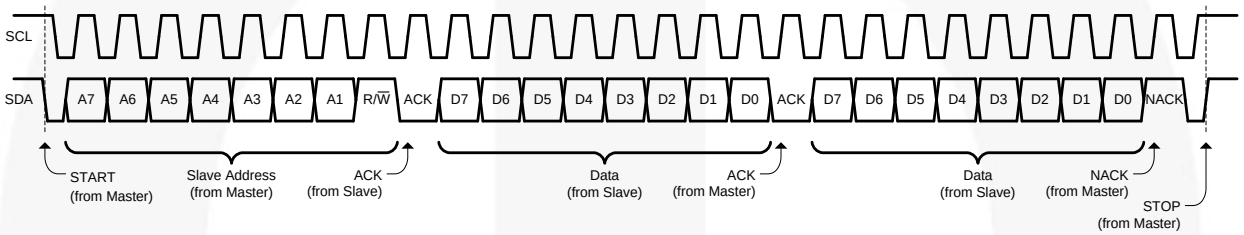


Figure 7. I²C Multiple Byte Read

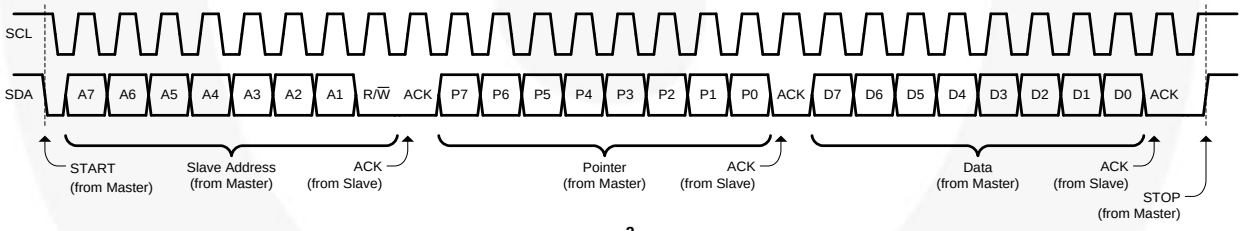


Figure 8. I²C Write

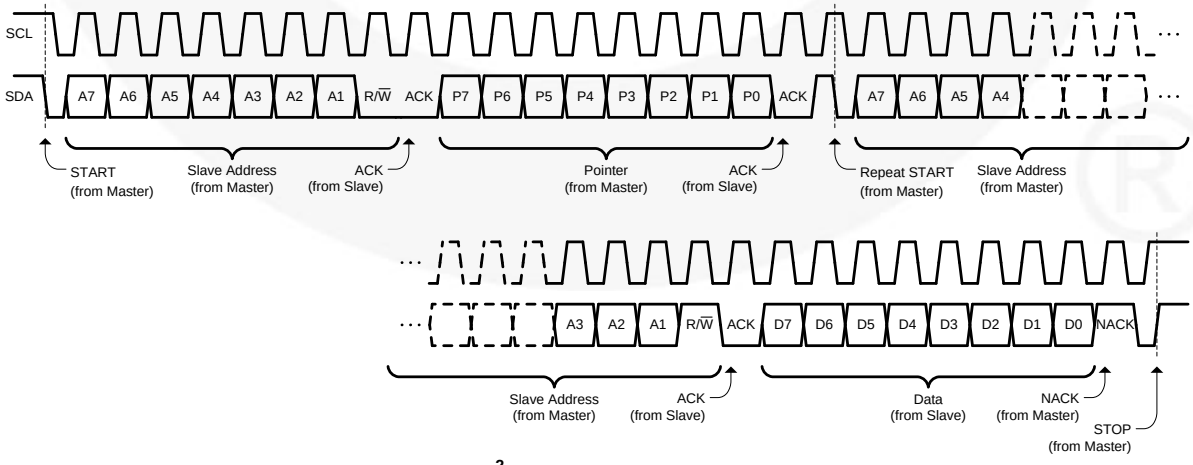


Figure 9. I²C Write Followed by Read

Table 2. Register Map Table

Adrs	Register	Type	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	CTRL1	R/W	10000000	HAPTIC_EN	Reserved	Reserved	Reserved		EN_LPF	SE	VREG_VCM
01H	CTRL2	R/W	00110011	IN_RES[2:0]			EN_PWM_DET	VREG_OUT[3:0]			
02H	STATUS1	R	Xxxx111x	Reserved	Reserved	Reserved	Reserved	VDD_G	VREG_OUT_G	VOT	Reserved
03H	CTRL_DIV1	R/W	01010011	PWM_DIV[7:0]							
04H	CTRL_DIV2	R/W	00000000	PWM_DIV[15:8]							
05H	CTRL_CALIB1	R/W	00000011	RESONANCE_MARGIN[3:0]				MEAS_DELAY[1:0]		EN_TEMP_REG	CALIB_EN
06H	CTRL_CALIB2	R/W	xxxx0011	Reserved	Reserved	Reserved	Reserved	PULSE_NUM[2:0]			SEL_AVRG
07H	CTRL_THR	R/W	00000100	Z_X_NUM[7:0]							
08H	CALIB_STATUS1	R	X001000	Reserved	CALIB_FAIL	LAST_LEVEL	CALIB_FIRST	CALIB_STATE[3:0]			
09H	CALIB_STATUS2	R	00000000	FIRST_TAG[7:0]							
0AH	CALIB_STATUS3	R	00000000	FIRST_TAG[15:8]							
0BH	CALIB_STATUS4	R	00000000	PWM_DIVISOR_A[7:0]							
0CH	CALIB_STATUS5	R	00000000	PWM_DIVISOR_A[15:8]							
0DH	CALIB_STATUS6	R	00000000	PWM_DIVISOR_B[7:0]							
0EH	CALIB_STATUS7	R	00000000	PWM_DIVISOR_B[15:8]							
0FH	CALIB_STATUS8	R	00000000	PWM_DIVISOR[7:0]							
10H	CALIB_STATUS9	R	00000000	PWM_DIVISOR[15:8]							
11H	CALIB_STATUS10	R	00000000	CNT_H[7:0]							
12H	CALIB_STATUS11	R	00000000	CNT_L[7:0]							
13H	CALIB_STATUS12	R	00000000	CNT_ZX[7:0]							
14H	CTRL3	W/R	Xxxxxxx0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SW_RST

Table 3. CTRL1

Address: 0x00

Reset Value: 1xxxx000

Bit #	Name	Type	Function
7	HAPTIC_EN	R/W	**1: Haptic Drive Enable Mode** 0: Power-Down Mode
6:3	Reserved		
2	EN_LPF	R/W	1: Enable internal 20 kHz LPF **0: Disable internal LPF**
1	SE	R/W	1: Single-Ended Mode **0: Differential Mode**
0	VREG_VCM	R/W	1: Outputs use V_{REG}/2 as VCMO **0: Outputs use V_{DD}/2 as VCMO**

Table 4. CTRL2

Address: 0x01

Reset Value: 00110011

Bit #	Name	Type	Function
7:5	IN_RES[2:0]	R/W	Input Resistance. 000: 8 kΩ **001: 10 kΩ** 010: 12 kΩ 011: 14 kΩ 100: 16 kΩ 101: 18 kΩ 110: 20 kΩ 111: 22 kΩ
4	EN_PWM_DET	R/W	**1: Enable PWM detection circuit** 0: Disable PWM detection circuit
3:0	VREG_OUT[3:0]	R/W	0000 1.4 V 0001 1.6 V 0010 1.8 V **0011 2.0 V** 0100 2.2 V 0101 2.4 V 0110 2.6 V 0111 2.8 V 1000 3.0 V 1001 3.2 V During LRA calibration stage 1, V_{REG_OUT} is always 2.0 V.

Table 5. STATUS1

Address: 0x02

Reset Value: xxxx111x

Bit #	Name	Type	Function
7:4	Reserved		
3	VDD_G	R	0: Input voltage is not good (less UVLO), Input voltage is less than 2.3 V (rising), 2.1 V (falling) **1: Input voltage is good (over UVLO)**
2	VREG_OUT_G	R	0: Regulator output is not good (V_{REG_OUT} is less than 70% of VREG_OUT programmed) **1: Regulator output is good**[3]
1	VOT	R	0: Over temperature protection is tripped **1: Over temperature protection is not tripped**
0	Reserved		

Note:

3. HEN must be HIGH for VREG_OUT to be enabled.

Table 6. CTRL_DIV1

Address: 0x03

Reset Value: 01010011

Bit #	Name	Type	Function
7:0	PWM_DIV[7:0]	R/W	LSB of the PWM divisor. For example, if the intended resonance frequency is 175 Hz and the PWM input clock frequency is 40 kHz, program the PWM[15:0] register as: PWM_DIV[15:0] = (1/175)/(1/40 kHz) = 228(decimal) = E4(HEX) PWM_DIV[15:8] = 00 PWM_DIV[7:0] = E4 Counter range is from 01 to E4. Default is 83

Table 7. CTRL_DIV2

Address: 0x04

Reset Value: 00000000

Bit #	Name	Type	Function
7:0	PWM_DIV[15:8]	R/W	MSB of the PWM divisor. Default is 0

Table 8. CTRL_CALIB1

Address: 0x05

Reset Value: 00000011

Bit #	Name	Type	Function
7:4	RESONANCE_MARGIN [3:0]	R/W	This is the % (of programmed PWM_DIV[15:0]) margin that is acceptable. The measured resonance frequency is ± compared against this margin. If within ± margins, the measured resonance frequency is accepted, else it is discarded. **0000 No limit** 0001 1/256 * 100 = %0.39 0010 1/128 * 100 = %0.78 0011 1/64 * 100 = %1.56 0100 1/32 * 100 = %3.12 0101 1/16 * 100 = %6.25 0110 1/8 * 100 = %12.5 0111 1/4 * 100 = %25.0
3:2	MEAS_DELAY[1:0]	R/W	Delay the zero crossing detection by a number of PWM clock cycles, which is calculated by below ratio multiple PWM_DIV. For example, if set to 00, the delay number is (PWM_DIV*1/8). **00: 1/8** 01: 1/16 10: 1/32 11: 1/64
1	EN_TEMP_REG	R/W	If set to 1, the detected PWM divisor value is stored in a Temp register and used at the starting of the next haptic event. If set to 0, haptic cycles always use the initial set PWM_DIV.
0	CALIB_EN	R/W	If set to 1, the part performs calibration, else no calibration.

Table 9. CTRL_CALIB2

Address: 0x06

Reset Value: xxxx0011

Bit #	Name	Type	Function
7:4	Reserved		
3:1	PULSE_NUM [2:0]	R/W	Determines the pulse number in stage 1 when calibration at beginning. The pulse number is #(PULSE_NUM+1). 000: pulse number 1 **001: pulse number 2** 010: pulse number **3** 011: pulse number 4 100: pulse number 5 101: pulse number 6 110: pulse number 7 111: pulse number 8
0	SEL_AVRG	R/W	**1: select average value of two periods as final LRA period result.** 0: select the detected first period as final LRA period result.

Table 10. CTRL_THR

Address: 0x07

Reset Value: 00000100

Bit #	Name	Type	Function
7:0	Z_X_NUM[7:0]	R/W	Threshold for transition region around zero-crossing point. It represents the jitter width around the zero-crossing point. When accumulative comparator result for one level (HIGH or LOW) around the transition edge reaches the threshold, zero-crossing point is thought to be found. The threshold is programmed referring to PWM_DIV. To be safe, set the threshold a bit larger than the real transition region.

Table 11. CALIB_STATUS1

Address: 0x08

Reset Value: x0010000

Bit #	Name	Type	Function
7	Reserved		
6	CALIB_FAIL	R	After the measurement delay period passes, count period of 3*PWM_DIV. During this time, if the four zero-crossing points are not found, calibration fails.
5	LAST_LEVEL	R	Indicate the last level (HIGH or LOW) for detecting next zero-crossing point.
4	CALIB_FIRST	R	Indicate whether current resonant detection is the first after power on reset or not.
3:0	CALIB_STATE	R	Resonant detection state machine.

Table 12. CALIB_STATUS2

Address: 0x09

Reset Value: 00000000

Bit #	Name	Type	Function
7:0	FIRST_TAG[7:0]	R	LSB bits of the tag for the first found zero-crossing edge.

Table 13. CALIB_STATUS3

Address: 0x0A

Reset Value: 00000000

Bit #	Name	Type	Function
7:0	FIRST_TAG[15:8]	R	MSB bits of the tag for the first found zero-crossing edge.

Table 14. CALIB_STATUS4

Address: 0x0B

Reset Value: 00000000

Bit #	Name	Type	Function
7:0	PWM_DIVISOR_A[7:0]	R	LSB bits of the resonant period calculated by the first zero-crossing point and third point.

Table 15. CALIB_STATUS5

Address: 0x0C

Reset Value: 00000000

Bit #	Name	Type	Function
7:0	PWM_DIVISOR_A[15:8]	R	MSB bits of the resonant period calculated by the first zero-crossing point and third point.

Table 16. CALIB_STATUS6

Address: 0x0D

Reset Value: 00000000

Bit #	Name	Type	Function
7:0	PWM_DIVISOR_B[7:0]	R	LSB bits of the resonant period calculated by the second zero-crossing point and the fourth point.

Table 17. CALIB_STATUS7

Address: 0x0E

Reset Value: 00000000

Bit #	Name	Type	Function
7:0	PWM_DIVISOR_B[15:8]	R	MSB bits of the resonant period calculated by the second zero-crossing point and the fourth point.

Table 18. CALIB_STATUS8

Address: 0x0F

Reset Value: 00000000

Bit #	Name	Type	Function
7:0	PWM_DIVISOR[7:0]	R	LSB bits of the final resonant period. PWM_DIVISOR may comes from initial PWM_DIV, or PWM_DIVISOR_A, or the average value of PWM_DIVISOR_A and PWM_DIVISOR_B.

Table 19. CALIB_STATUS9

Address: 0x10

Reset Value: 00000000

Bit #	Name	Type	Function
7:0	PWM_DIVISOR[15:8]	R	MSB bits of the final resonant period.

Table 20. CNT_H

Address: 0x11

Reset Value: 00000000

Bit #	Name	Type	Function
7:0	CNT_H[7:0]	R	High level counter during first edge detection.

Table 21. CNT_L

Address: 0x12

Reset Value: 00000000

Bit #	Name	Type	Function
7:0	CNT_L[7:0]	R	Low level counter during first edge detection.

Table 22. CNT_H

Address: 0x13

Reset Value: 00000000

Bit #	Name	Type	Function
7:0	CNT_ZX[7:0]	R	Level counter used for zero-crossing points detection.

Table 23. CTRL3

Address: 0x14

Reset Value: xxxxxxx0

Bit #	Name	Type	Function
7:1	Reserved		
0	SW_RST	W/R	Software reset bit, default is zero. When this bit is set 1, a negative pulse is generated and all the ongoing operation is stopped and all registers reset to default values. This bit is self-clearing and changes back to HIGH after the negative pulse.

Applications Information

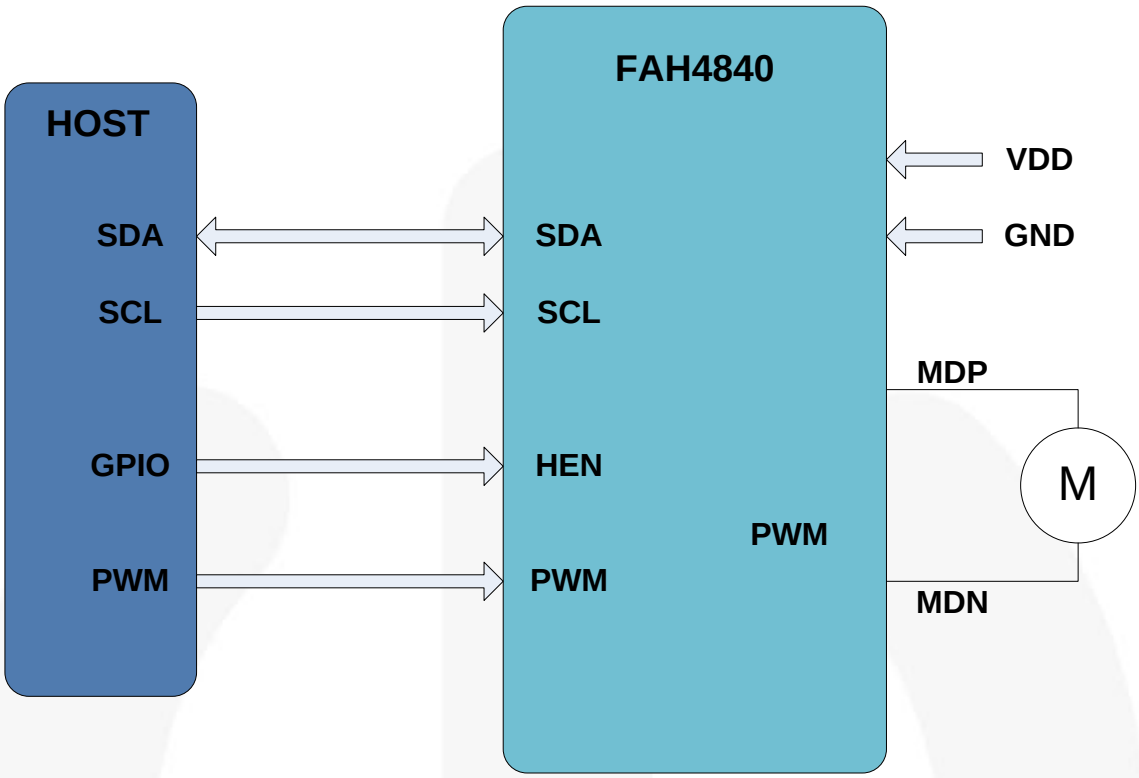


Figure 10. System Block Diagram

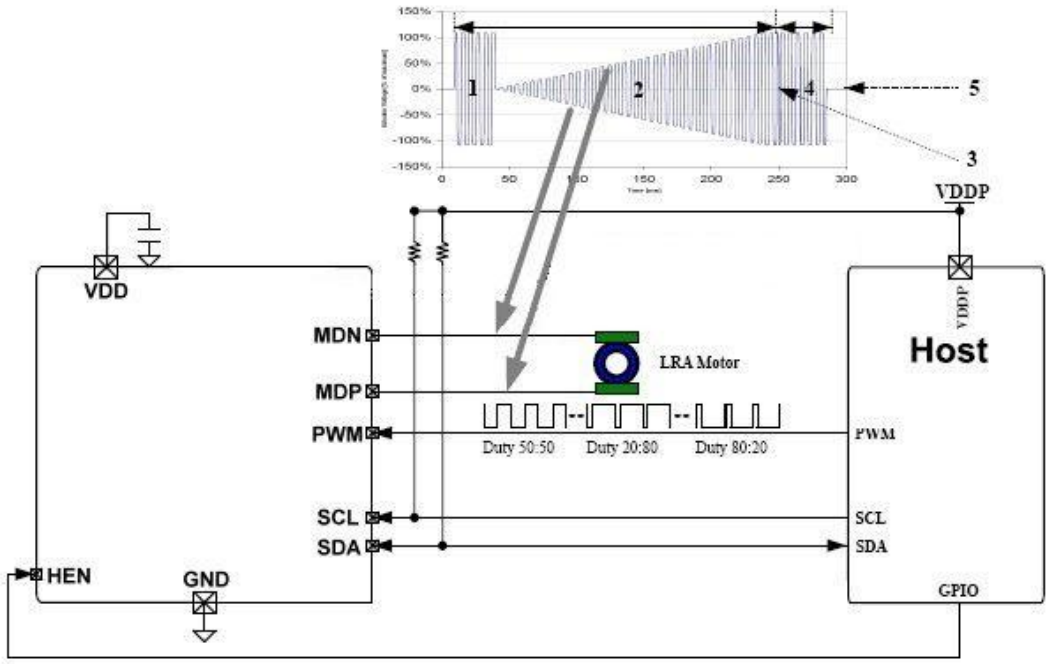


Figure 11. LRA System Block Diagram

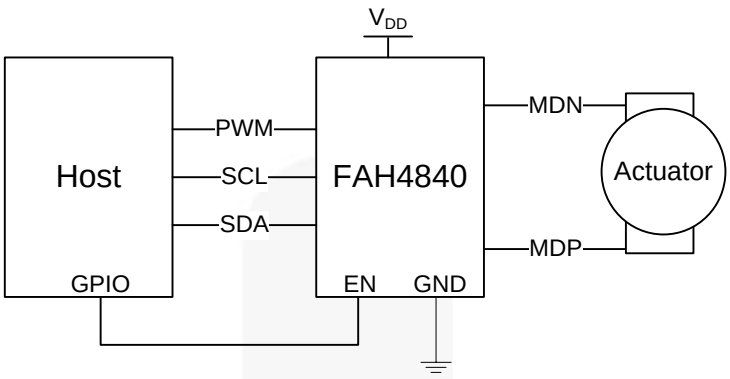
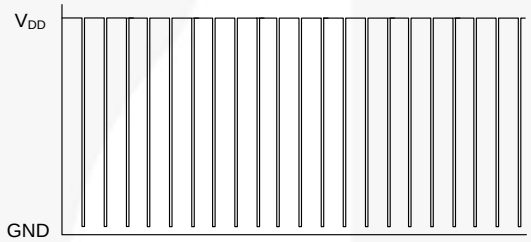
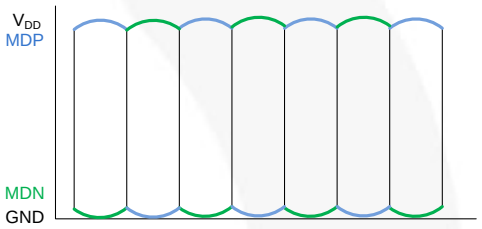
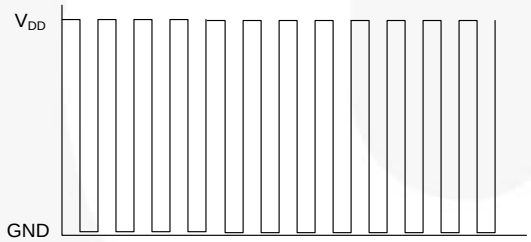
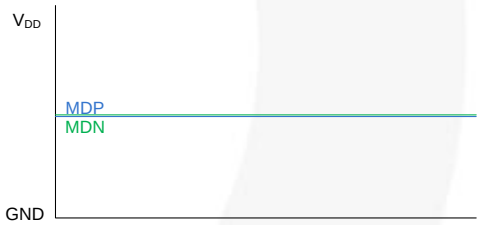
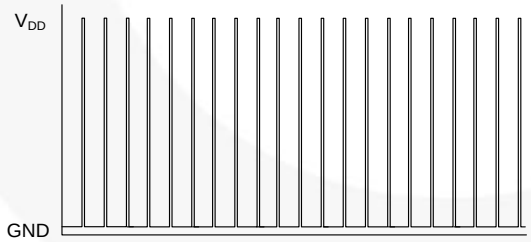
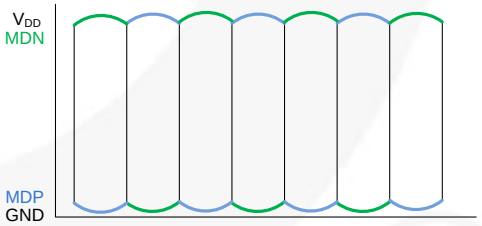


Figure 12. LRA System Block Diagram

Table 24. LRA Resonant Actuator Function

	PWM Duty Cycle[4]	LRA Drive Voltage at Resonant Frequency
90/10% PWM Duty Cycle		
50/50% PWM Duty Cycle		
10/90% PWM Duty Cycle		

Note:

4. PWM frequency is a multiple of the LRA resonant frequency. This is controlled by I^2C registers CTRL_DIV1 and CTRL_DIV2. For example, if the LRA resonant frequency is 175 Hz, the PWM frequency would be 14.5 kHz and the I^2C CTRL_DIV1 and CTRL_DIV2 registers would be programmed to 1/83.

Internal LDO

The internal LDO is designed for adjustable output voltage (V_{REG_OUT}), controlled by a 16-step I^2C register. This provides flexibility, convenience, and configuration for low-power consumption. The LDO includes an internal circuit for short-circuit current protection.

Serial Interface

The I^2C registers allow the user to program the motor type, PWM dividing ratio, power-down, and other functions. The device needs to function without any I^2C input signals connected.

Thermal Shutdown

The device has thermal shutdown capability. If the junction temperature is above 150°C, the temperature control block shuts down and remains off until the temperature goes below 134°C. The register values are kept, so re-initialization is not required.

Over-Current Limitation

The driver includes a current-limitation block to protect against an over-current condition. This is mainly a protection against a stuck spring condition. Over-current shutdown is at 350 mA typically.

Status Registers

The status register set monitors LDO input voltage, regulator output voltage, and over-temperature status.

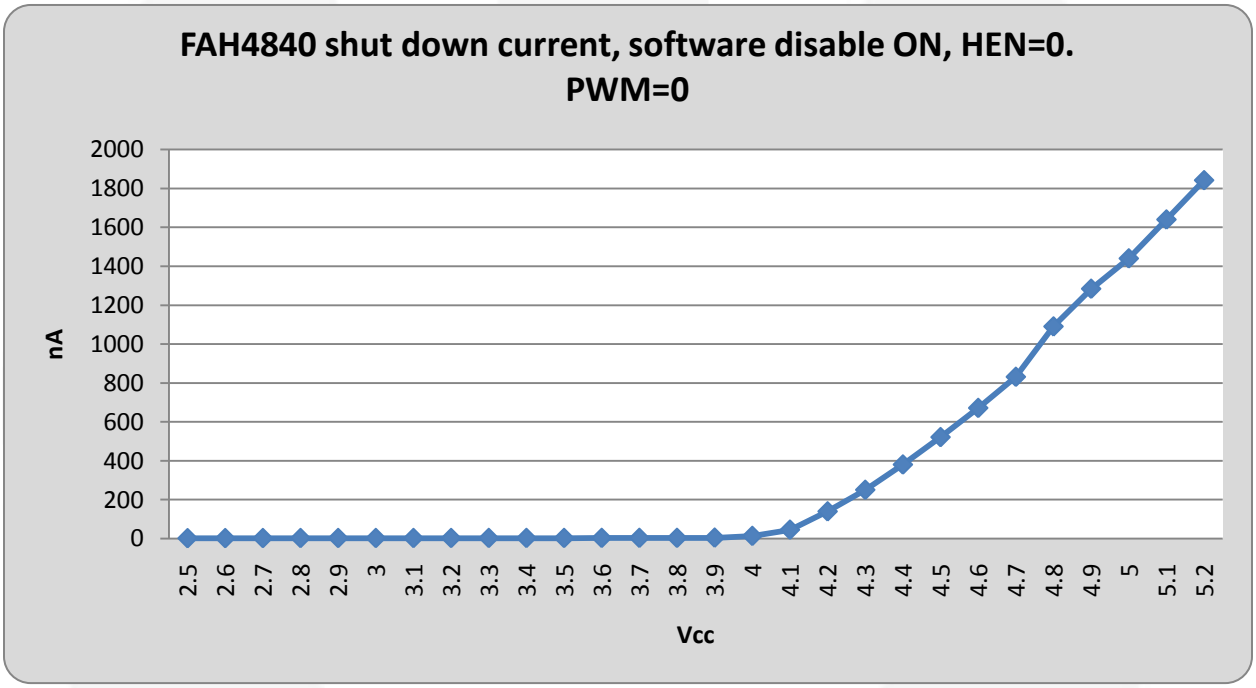
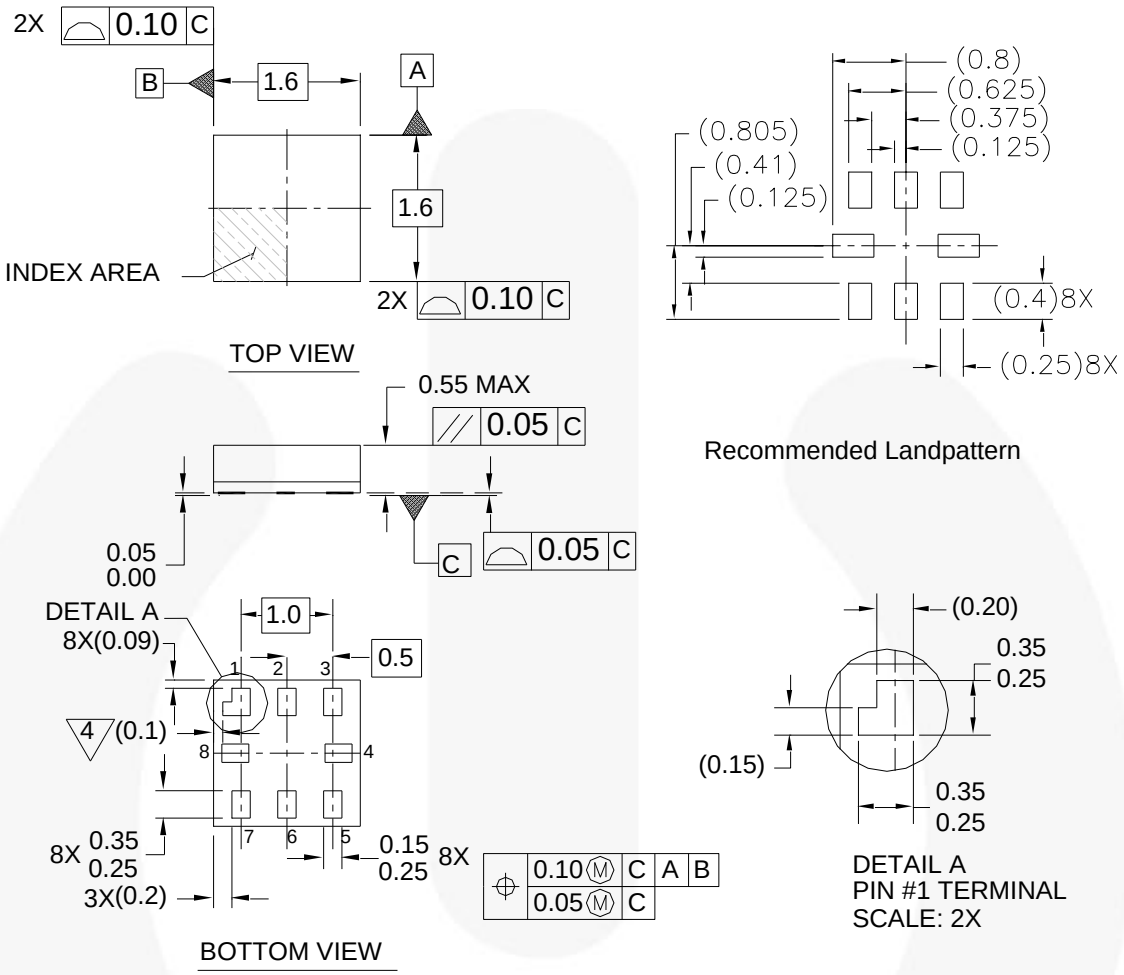


Figure 13. Typical Performance Characteristics

Physical Dimensions



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET
5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

Figure 14. 8-Lead, MicroPak MLP

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