μPD424400, 424400A/L, 42S4400A/L
1,048,576 x 4-Bit Dynamic CMOS RAM

Description

The devices listed below are fast-page dynamic RAMs organized as 1,048,576 words by 4 bits and designed to operate from a single power supply.

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
Second-generation products	
424400-xx	+5 V
424400-xxL	+5 V; low-power
Third-generation products	
424400A-xx	+5 V
42S4400A-xx	+5 V; self-refresh, low-power
424400L-Axx	+3.3 V
42S4400L-Axx	+3.3 V; self-refresh, low-power

-xx indicates speed grade (RAS access time).

Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1024 address combinations of A_0 - A_9 during a 16-ms refresh period.

The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

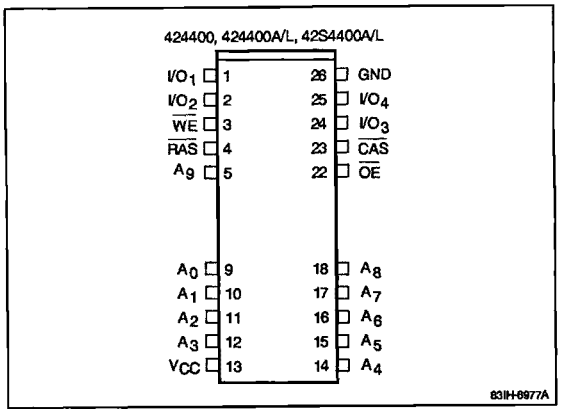
- 1,048,576 by 4-bit organization
- Single +5-volt power supply
- Fast-page option
- Self-refresh option (slow internal automatic refresh)
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- 26/20-pin SOJ, 20-pin ZIP, and 26/20-pin TSOP plastic packaging

Pin Identification

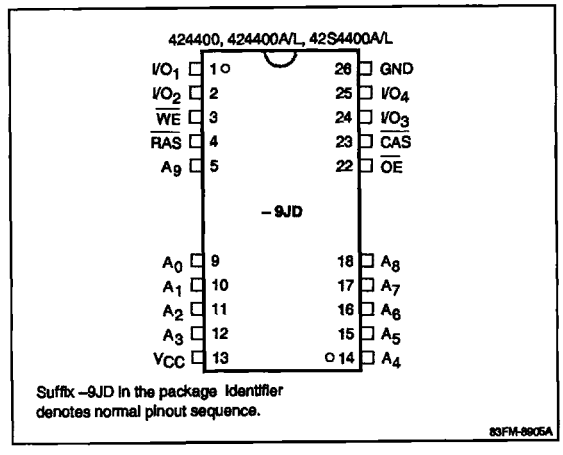
Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Pin Configurations

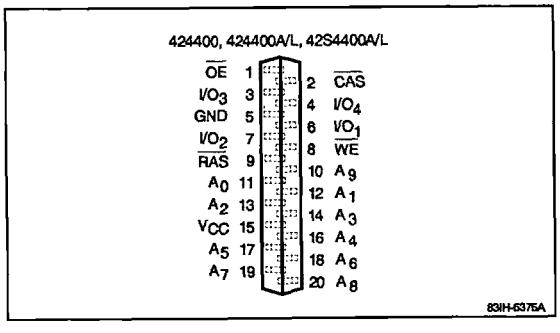
26/20-Pin Plastic SOJ



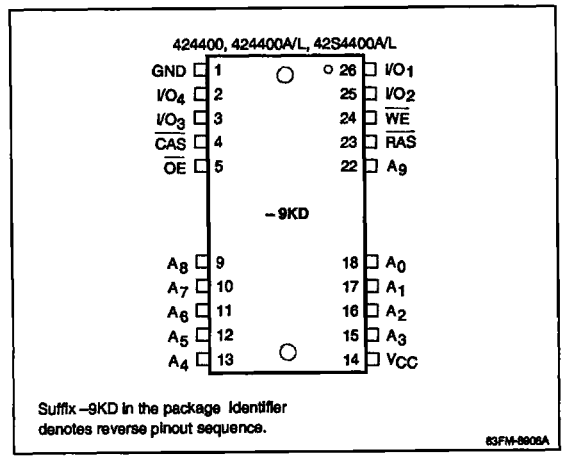
26/20-Pin Plastic TSOP (Normal Pinouts)



20-Pin Plastic ZIP



26/20-Pin Plastic TSOP (Reverse Pinouts)



Ordering Information, μPD424400 (+ 5 V; standard version; 2nd-generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Power Option	Package
μPD424400LA-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic SOJ (300-mil)
LA-70	70 ns	140 ns	45 ns		
LA-80	80 ns	160 ns	50 ns		
μPD424400LA-60L	60 ns	120 ns	40 ns	Low-power	
LA-70L	70 ns	140 ns	45 ns		
LA-80L	80 ns	160 ns	50 ns		
μPD424400V-60	60 ns	120 ns	40 ns	Standard	20-pin plastic ZIP
V-70	70 ns	140 ns	45 ns		
V-80	80 ns	160 ns	50 ns		
μPD424400V-60L	60 ns	120 ns	40 ns	Low-power	
V-70L	70 ns	140 ns	45 ns		
V-80L	80 ns	160 ns	50 ns		
μPD424400GS-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic TSOP (normal pinouts)
GS-70	70 ns	140 ns	45 ns		
GS-80	80 ns	160 ns	50 ns		
μPD424400GS-60L	60 ns	120 ns	40 ns	Low-power	
GS-70L	70 ns	140 ns	45 ns		
GS-80L	80 ns	160 ns	50 ns		
μPD424400GSM-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic TSOP (reverse pinouts))
GSM-70	70 ns	140 ns	45 ns		
GSM-80	80 ns	160 ns	50 ns		
μPD424400GSM-60L	60 ns	120 ns	40 ns	Low-power	
GSM-70L	70 ns	140 ns	45 ns		
GSM-80L	80 ns	160 ns	50 ns		

Ordering Information, μPD424400A (+ 5 V; standard version; 3rd-generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD424400ALA-50	50 ns	100 ns	35 ns	26/20-pin plastic SOJ (300-mil)
LA-60	60 ns	120 ns	40 ns	
LA-70	70 ns	140 ns	45 ns	
LA-80	80 ns	160 ns	50 ns	
μPD424400AV-50	50 ns	100 ns	35 ns	20-pin plastic ZIP
V-60	60 ns	120 ns	40 ns	
V-70	70 ns	140 ns	45 ns	
V-80	80 ns	160 ns	50 ns	
μPD424400AGS-50	50 ns	100 ns	35 ns	26/20-pin plastic TSOP (normal pinouts)
GS-60	60 ns	120 ns	40 ns	
GS-70	70 ns	140 ns	45 ns	
GS-80	80 ns	160 ns	50 ns	
μPD424400AGSM-50	50 ns	100 ns	35 ns	26/20-pin plastic TSOP (reverse pinouts)
GSM-60	60 ns	120 ns	40 ns	
GSM-70	70 ns	140 ns	45 ns	
GSM-80	80 ns	160 ns	50 ns	

Ordering Information, μPD42S4400A (+ 5 V; self-refresh, low-power version; 3rd-generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Self-Refresh Current (max)	Package
μPD42S4400ALA-50	50 ns	100 ns	35 ns	200 μA	26/20-pin plastic SOJ (300-mil)
LA-60	60 ns	120 ns	40 ns		
LA-70	70 ns	140 ns	45 ns		
LA-80	80 ns	160 ns	50 ns		
μPD42S4400AV-50	50 ns	100 ns	35 ns	200 μA	20-pin plastic ZIP
V-60	60 ns	120 ns	40 ns		
V-70	70 ns	140 ns	45 ns		
V-80	80 ns	160 ns	50 ns		
μPD42S4400AGS-50	50 ns	100 ns	35 ns	200 μA	26/20-pin plastic TSOP (normal pinouts)
GS-60	60 ns	120 ns	40 ns		
GS-70	70 ns	140 ns	45 ns		
GS-80	80 ns	160 ns	50 ns		
μPD42S4400AGSM-50	50 ns	100 ns	35 ns	200 μA	26/20-pin plastic TSOP (reverse pinouts)
GSM-60	60 ns	120 ns	40 ns		
GSM-70	70 ns	140 ns	45 ns		
GSM-80	80 ns	160 ns	50 ns		

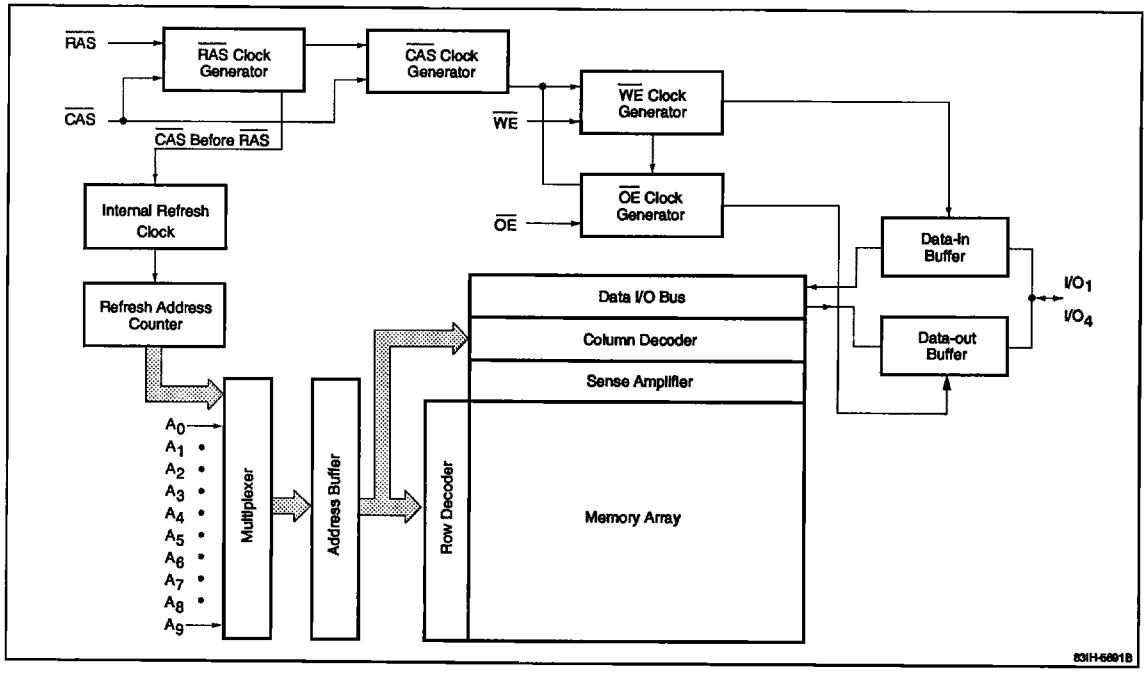
Ordering Information, μPD424400L (+ 3.3 V; standard version; 3rd-generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD424400LLA-A70	70 ns	140 ns	45 ns	26/20-pin plastic SOJ (300-mil)
LA-A80	80 ns	160 ns	50 ns	
μPD424400LV-A70	70 ns	140 ns	45 ns	20-pin plastic ZIP
V-A80	80 ns	160 ns	50 ns	
μPD424400LGS-A70	70 ns	140 ns	45 ns	26/20-pin plastic TSOP (normal pinouts)
GS-A80	80 ns	160 ns	50 ns	
μPD424400LGSM-A70	70 ns	140 ns	45 ns	26/20-pin plastic TSOP (reverse pinouts)
GSM-A80	80 ns	160 ns	50 ns	

Ordering Information, μPD42S4400L (+ 3.3 V; self-refresh, low-power version; 3rd-generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Self-Refresh Current (max)	Package
μPD42S4400LLA-A70	70 ns	140 ns	45 ns	100 μA	26/20-pin plastic SOJ (300-mil)
LA-A80	80 ns	160 ns	50 ns		
μPD42S4400LV-A70	70 ns	140 ns	45 ns	100 μA	20-pin plastic ZIP
V-A80	80 ns	160 ns	50 ns		
μPD42S4400LGS-A70	70 ns	140 ns	45 ns	100 μA	26/20-pin plastic TSOP (normal pinouts)
GS-A80	80 ns	160 ns	50 ns		
μPD42S4400LGSM-A70	70 ns	140 ns	45 ns	100 μA	26/20-pin plastic TSOP (reverse pinouts)
GSM-A80	80 ns	160 ns	50 ns		

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
5-volt devices	50 mA
3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_4

DC Characteristics; 5-Volt Devices

Recommended operating conditions unless otherwise noted.

		424400, 424400A		42S4400A			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0		2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
			1.0		0.2	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10	10	−10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	−10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		2.4		V	I_{OH} = −5 mA
Self-refresh current	I_{CC7}	Not applicable			200	μA	I_O = 0 mA; all I/O and input pins ≥ V_{CC} −0.2 V or ≤ 0.2 V or open; t_{RAS} ≥ 100 μs; 1024 refresh cycles must be performed within 16 ms before entering self-refresh and after exiting self-refresh

5d

DC Characteristics; 3.3-Volt Devices

Recommended operating conditions unless otherwise noted.

		424400L		42S4400L			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0		0.5	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
			0.5		0.1	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−5	5	−5	5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−5	5	−5	5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4		0.4	V	I_{OL} = 2 mA
Output voltage, high	V_{OH}	2.4		2.4		V	I_{OH} = −2 mA
Self-refresh current	I_{CC7}	Not applicable			100	μA	I_O = 0 mA; all I/O and input pins ≥ V_{CC} −0.2 V or ≤ 0.2 V or open; t_{RAS} ≥ 100 μs; 1024 refresh cycles must be performed within 16 ms before entering self-refresh and after exiting self-refresh

Low-Power Battery Backup (Low-Power and Self-Refresh Versions Only)

Symbol	424400-xxL	42S4400A	42S4400L	Unit	t_{RAS}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6} (max)	500	300	150	μA	≤ 1 μs	1024 refresh cycles (min) every 128 ms; $\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V or ≤ 0.2 V, as appropriate; I/O open; all other inputs ≥ V_{CC} − 0.2 V or ≤ 0.2 V	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; D_{IN}, $\overline{WE}$, $\overline{OE}$, Addresses ≥ V_{CC} − 0.2 V or ≤ 0.2 V; I/O open
	300	200	100	μA	≤ 200 ns		

Recommended Operating Conditions

Parameter	Symbol	5-Volt Devices Min	Typ	Max	3.3-Volt Devices Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

AC Characteristics

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	-50 Min	-50 Max	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5 V)		100		120		100		90	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC1} (+3.3 V)						70		60	mA	
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5 V)		100		120		100		90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC3} (+3.3 V)						70		60	mA	
Operating current, fast-page cycle, average	I_{CC4} (+5 V)		90		90		80		70	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
	I_{CC4} (+3.3 V)						60		50	mA	
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5 V)		100		120		100		90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC5} (+3.3 V)						70		60	mA	
Access time from column address	t_{AA}		25		30		35		40	ns	(Notes 3, 4, 7, 8, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		30		35		40		45	ns	(Notes 3, 4, 7, 11)
Column address setup time	t_{ASC}	0	5	0	5	0	10	0	15	ns	(Note 9)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		50		55		65		ns	(Note 16)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		15		15		20		20	ns	(Notes 3, 4, 7, 8, 11)
Column address hold time	t_{CAH}	15		15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	10		15		15		15		ns	

AC Characteristics (cont)

Parameter	Symbol	-50		-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ hold (CBR self-refresh)	t_{CHS}	−50		−50		−50		−50		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		0		ns	(Note 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10	10	10	10	10	15	10	20	ns	(Note 9)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		40		45		ns	(Note 16)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		15		ns	
Data-in hold time	t_{DH}	10		15		15		15		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 15)
Access time from $\overline{OE}$	t_{OEA}		15		15		20		20	ns	(Notes 3, 4, 7, 8, 11)
$\overline{OE}$ delay data time	t_{OED}	15		15		15		20		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	0	20	ns	(Note 10)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	15	0	20	ns	(Note 10)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		0		ns	(Notes 6, 7)
Fast-page cycle time	t_{PC}	35		40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	80		85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	17	40	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	25		30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ width (CBR self-refresh)	t_{RASS}	100		100		100		100		μs	

5d

AC Characteristics (cont)

Parameter	Symbol	-50		-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	100		120		140		160		ns	(Note 6)
						130		150		ns	(Notes 6, 18)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	35	20	40	20	50	25	60	ns	(Notes 8, 9)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9 (Note 19)
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		40		60		70		ns	
						50		60		ns	(Note 18)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ precharge (CBR self-refresh)	t_{RPS}	90		110		130		150		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	15		15		20		20		ns	
Read-write cycle time	t_{RWC}	145		165		185		210		ns	(Note 6)
						175		200		ns	(Notes 6, 18)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	75		80		90		105		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	10		10		15		15		ns	(Note 14)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		15		ns	
Write command pulse width	t_{WP}	10		10		15		15		ns	(Note 14)
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

AC Characteristics

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) For random read cycles, access time is defined as follows.

Input Conditions	Access Time
$t_{RAD} \leq t_{RAD}$ (max), $t_{RCD} \leq t_{RCD}$ (max)	t_{RAC}
$t_{RAD} \geq t_{RAD}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{RAD} \geq t_{RAD}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

The above access times assume that $\overline{OE}$ has been active t_{OEA} (max) prior to when data is expected on the output.

(9) t_{RCD} (max), t_{RAD} (max), t_{ASC} (max) and t_{CP} (max) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA}, t_{CAC}, or t_{ACP}) is to be used for determining when output data will be available.

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(11) For fast-page read operation, access time is defined follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

The above access times assume that $\overline{OE}$ has been active t_{OEA} (max) prior to when data is expected on the output.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

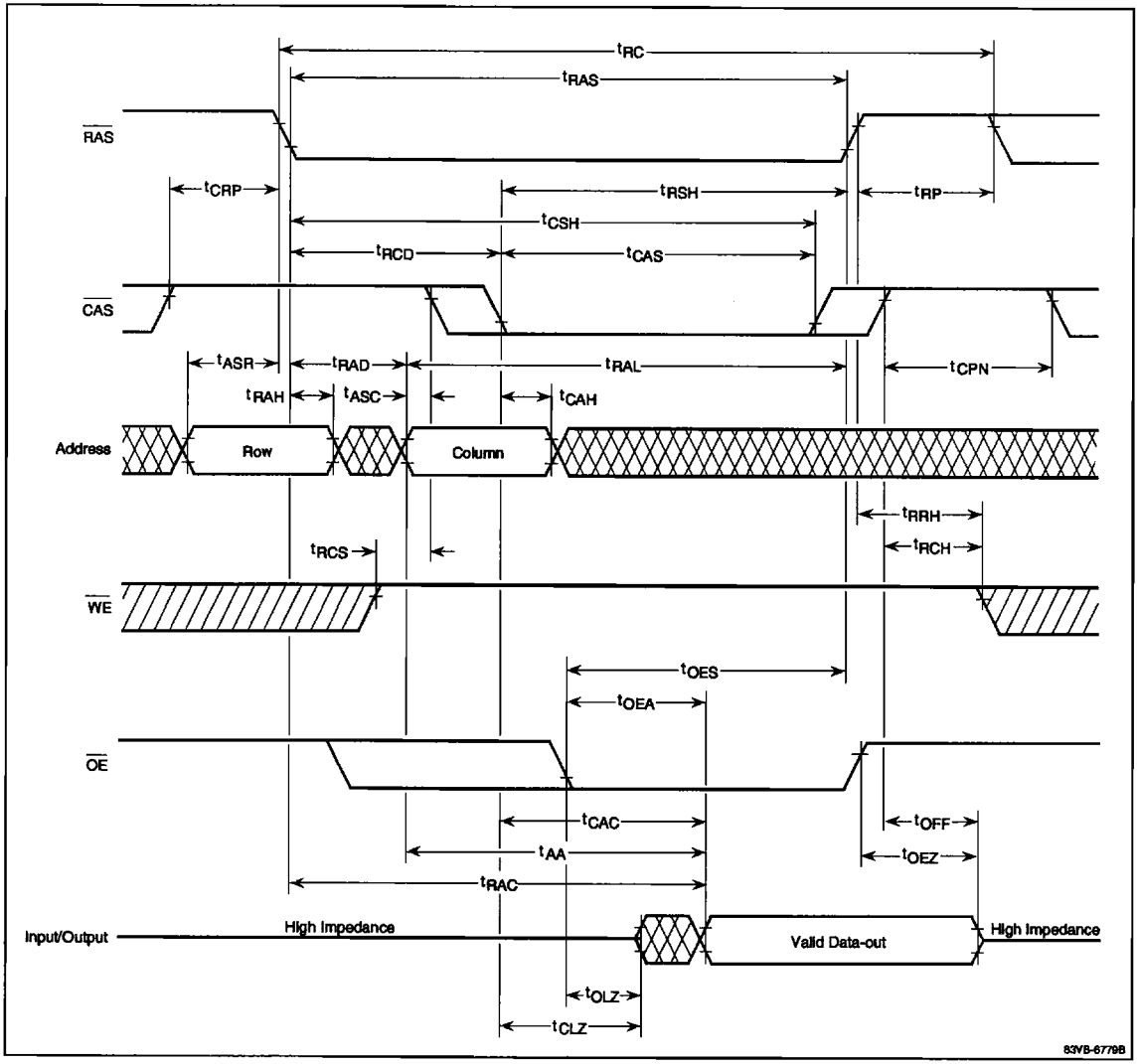
(18) Applies to μPD424400L and μPD42S4400L.

(19) 1024 refresh cycles must be performed within 16 ms before entering self-refresh and after exiting self-refresh.

5d

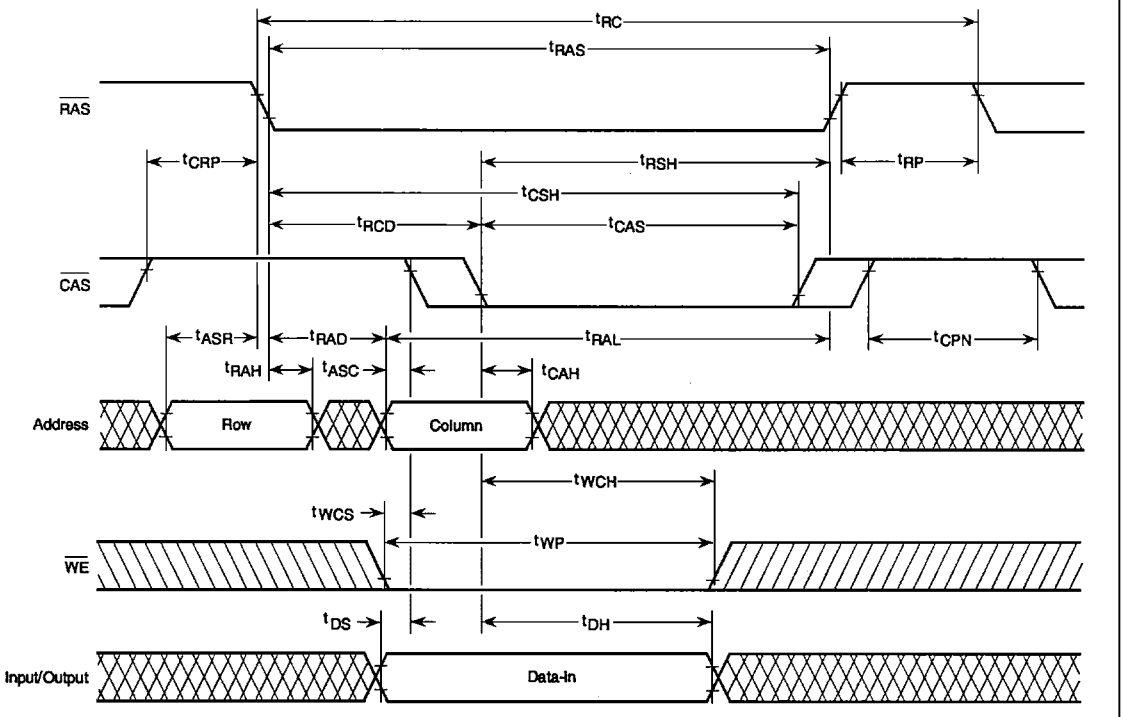
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



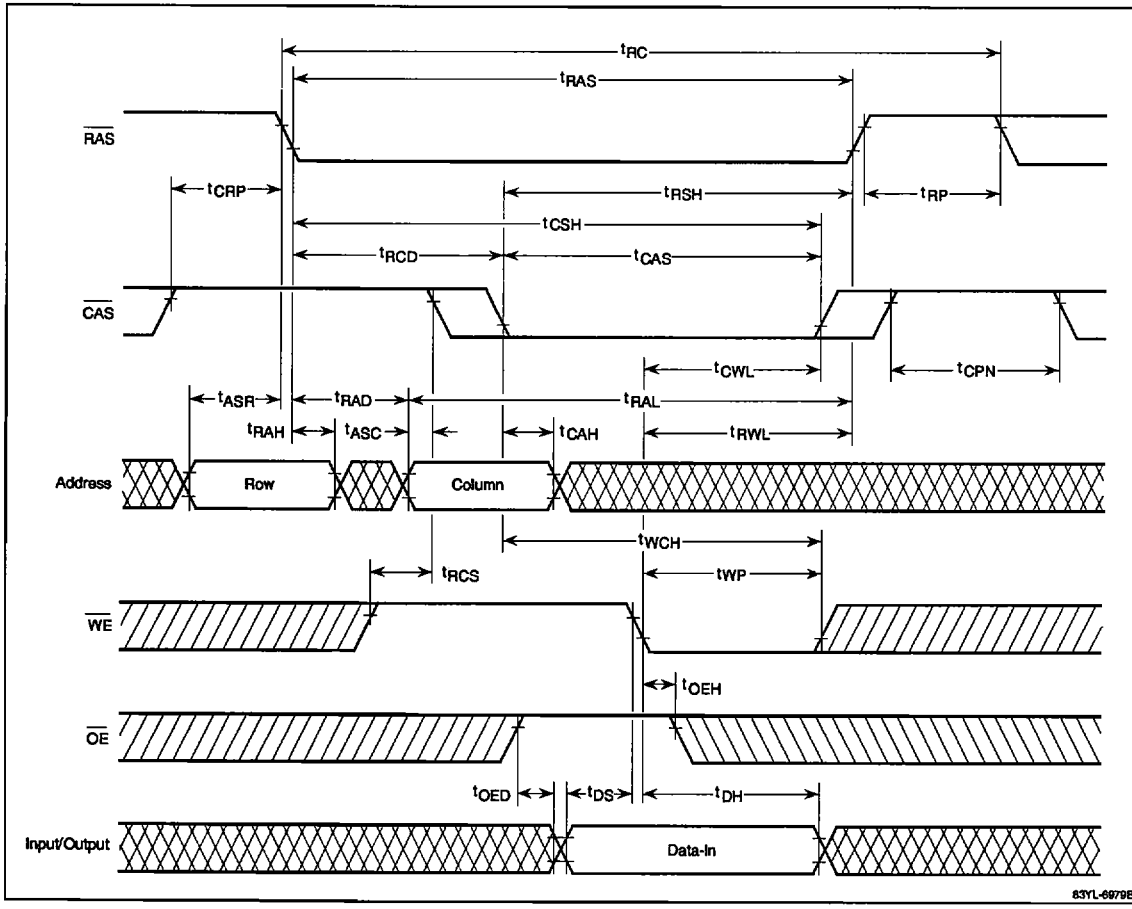
Note:
[1] $\overline{OE}$ = don't care.

83YL-6978B

5d

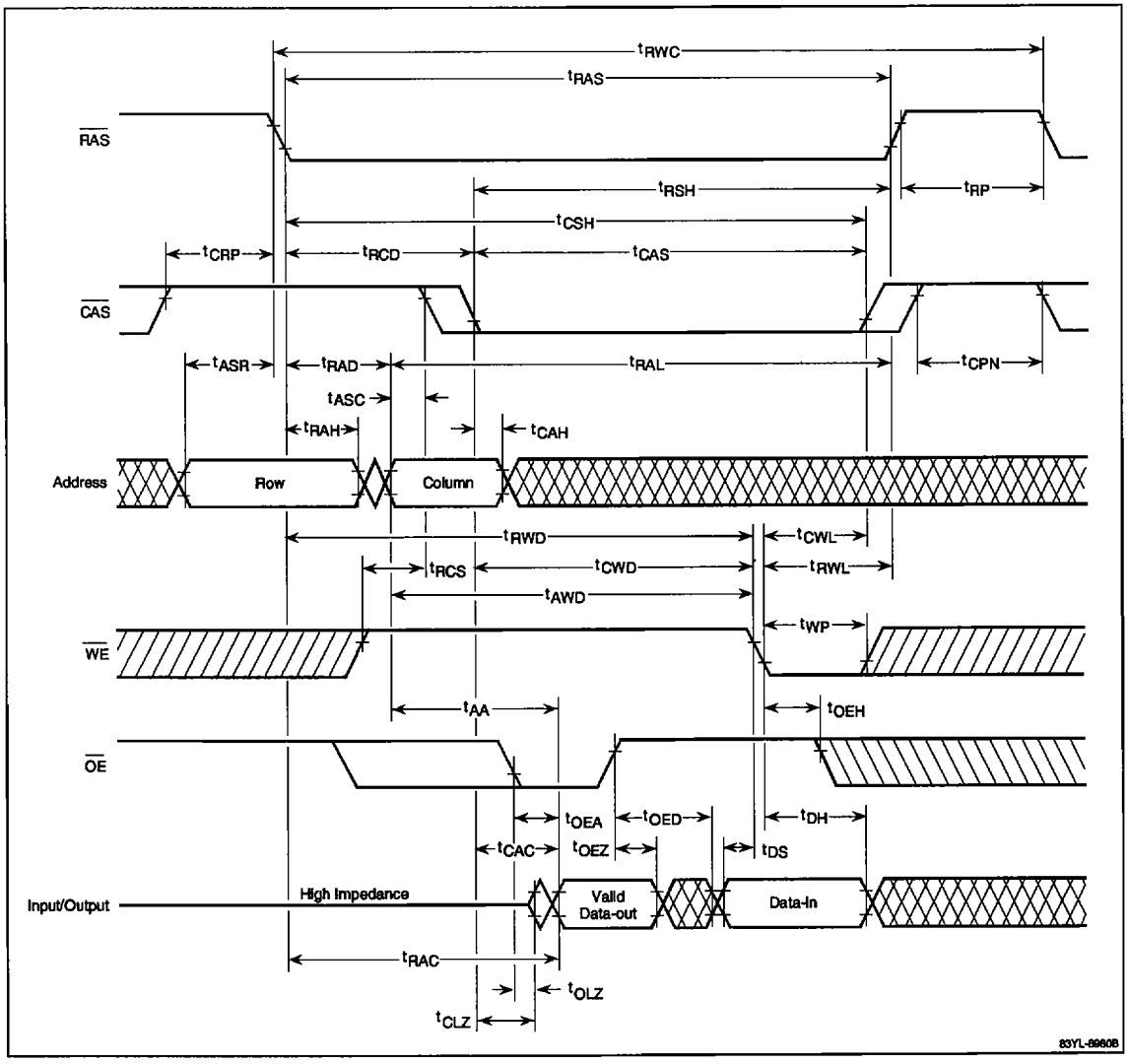
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

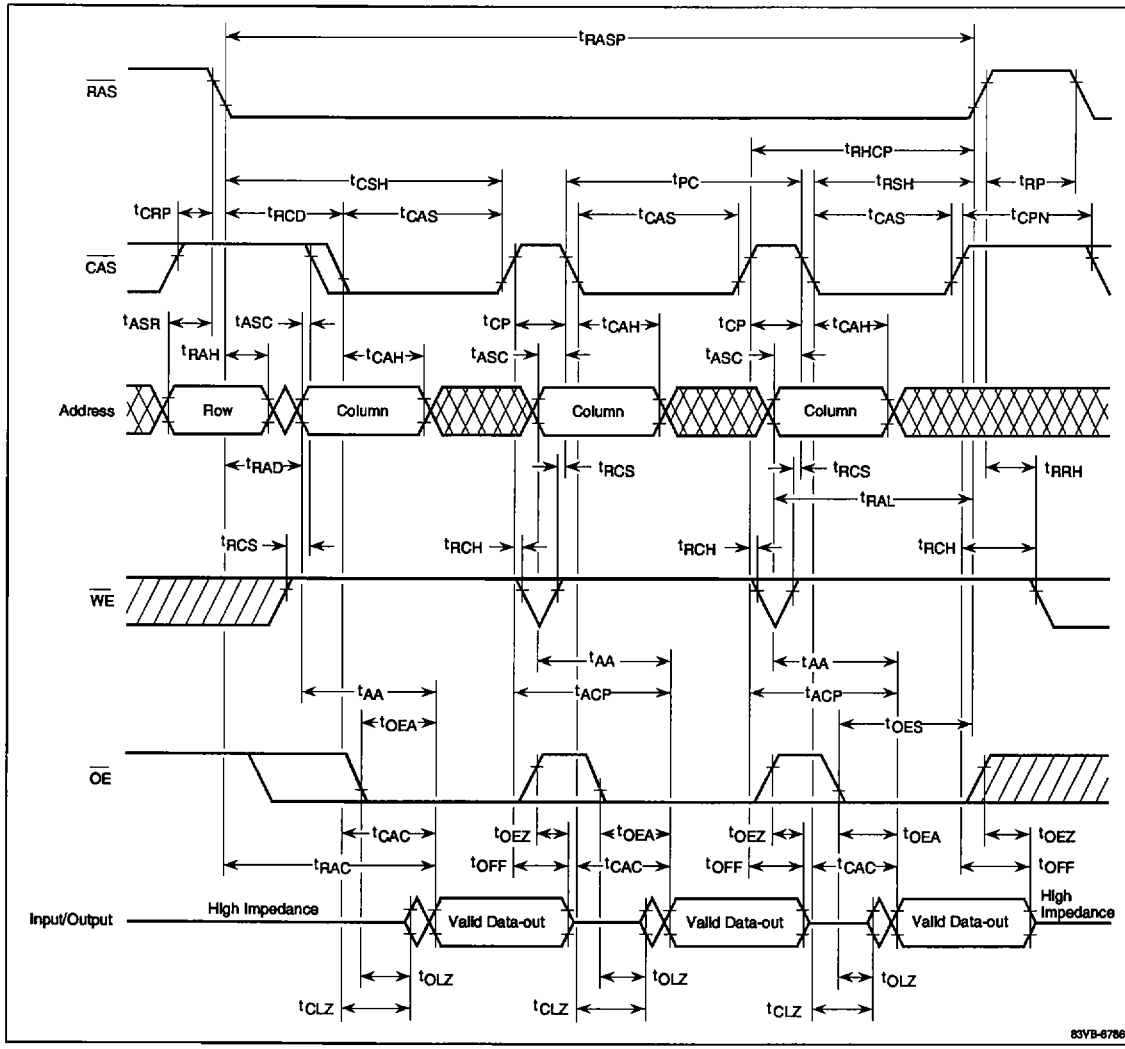
Read-Write/Read-Modify-Write Cycle



5d

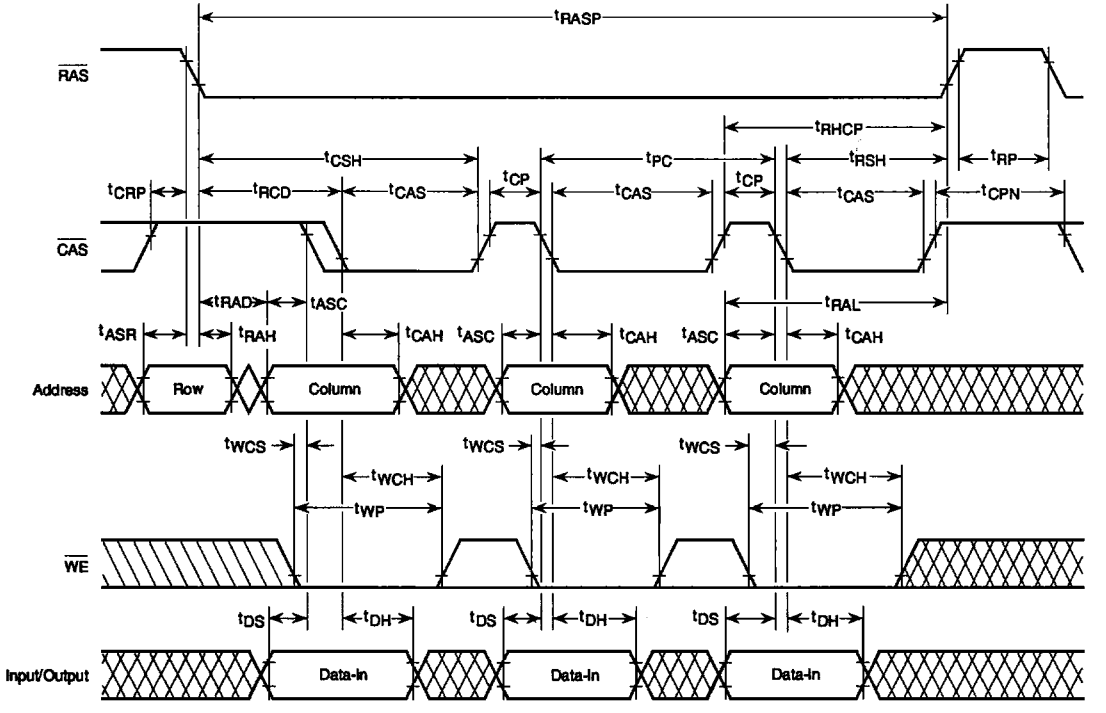
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



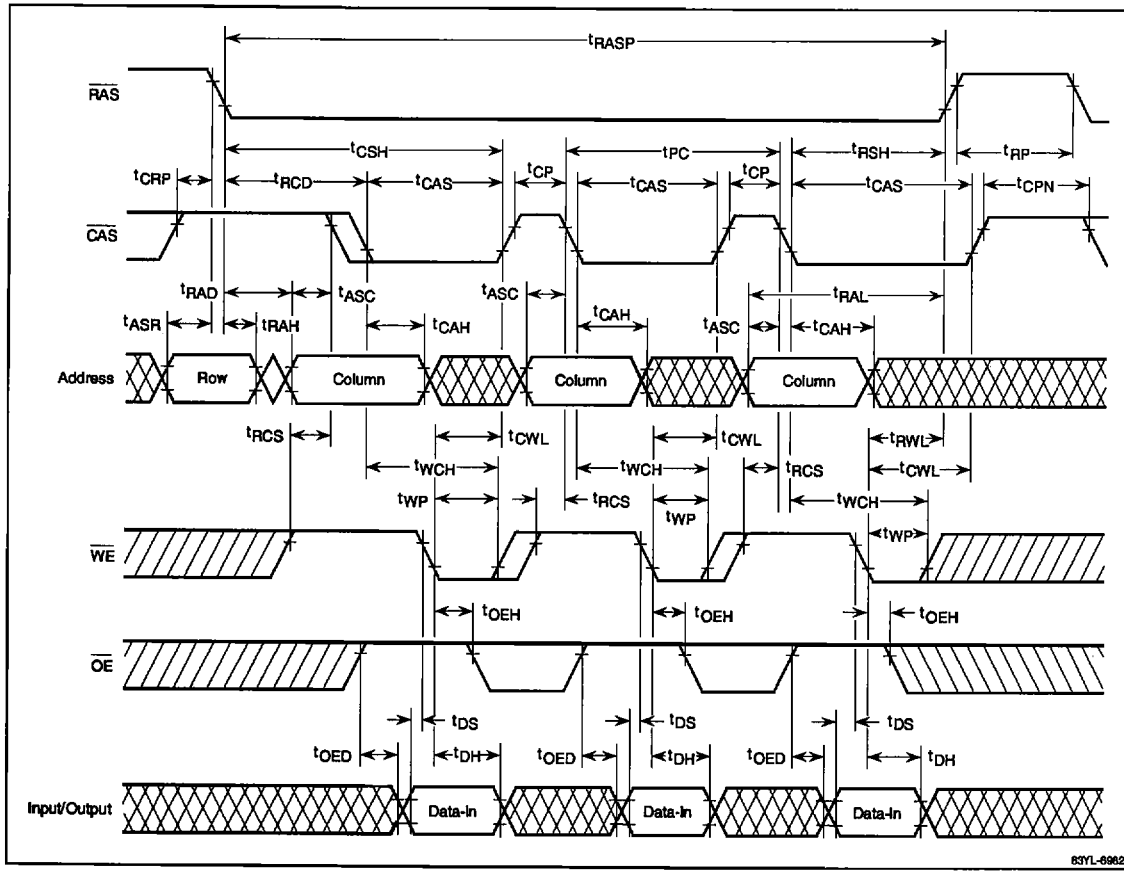
Note:
[1] $\overline{OE}$ = don't care.

83YL-8981B

5d

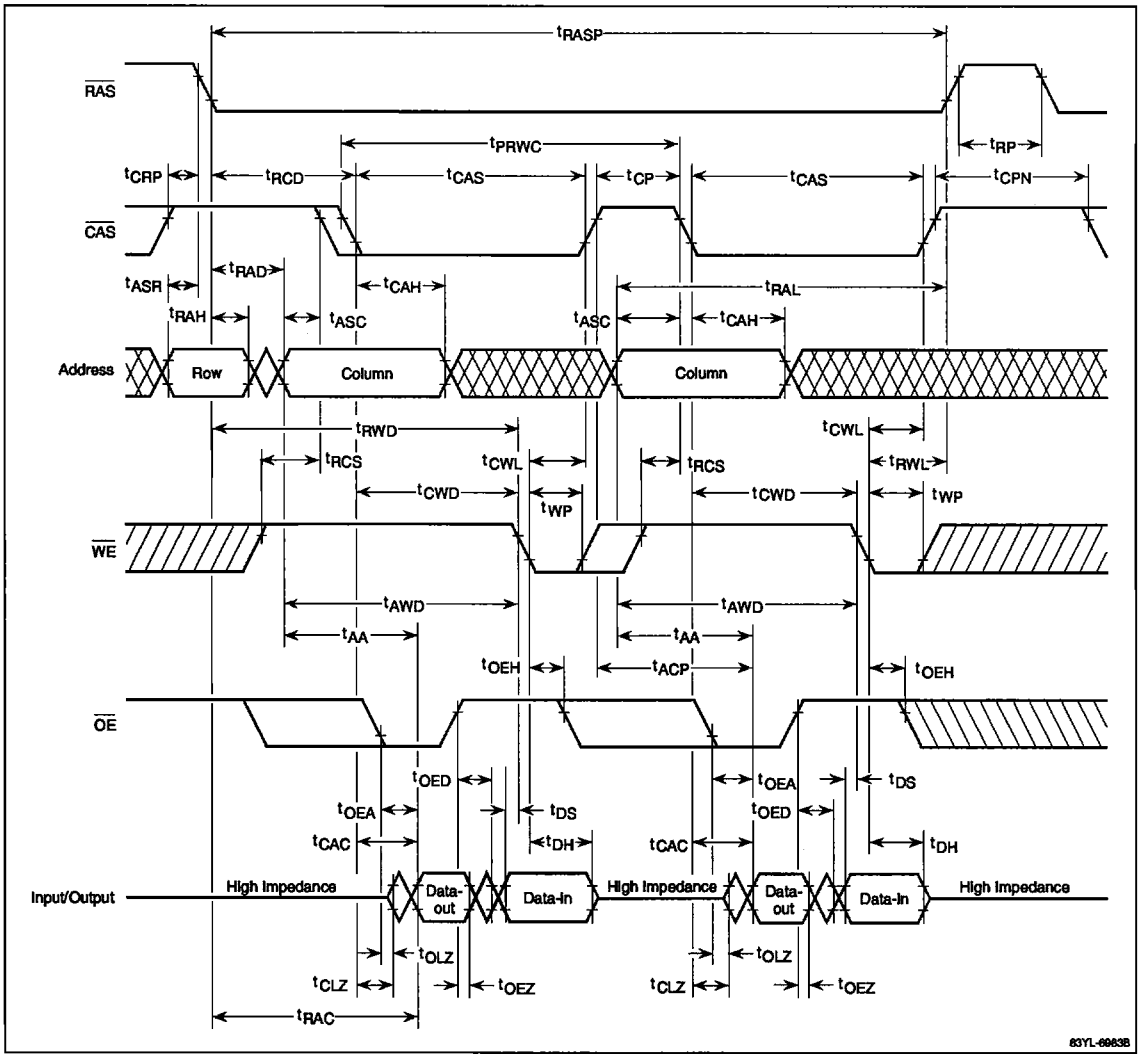
Timing Waveforms (cont)

Fast-Page Late Write Cycle



Timing Waveforms (cont)

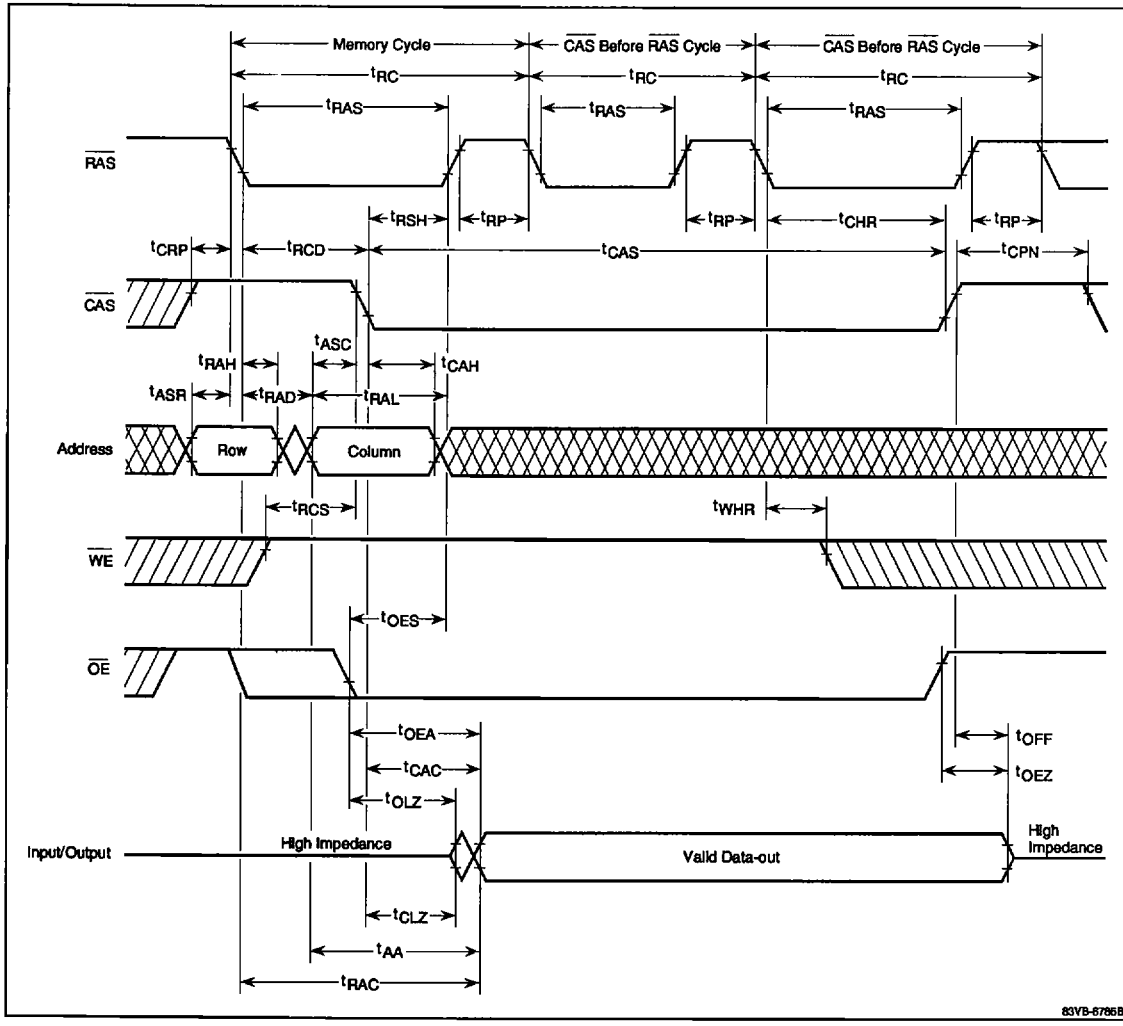
Fast-Page Read-Write/Read-Modify-Write Cycle



5d

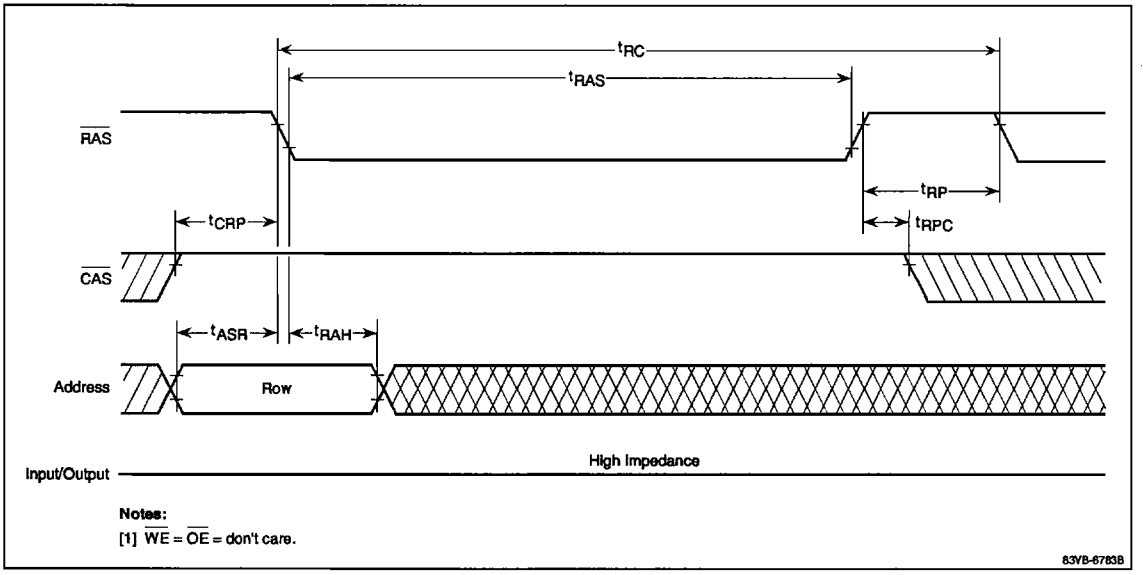
Timing Waveforms (cont)

Hidden Refresh Cycle

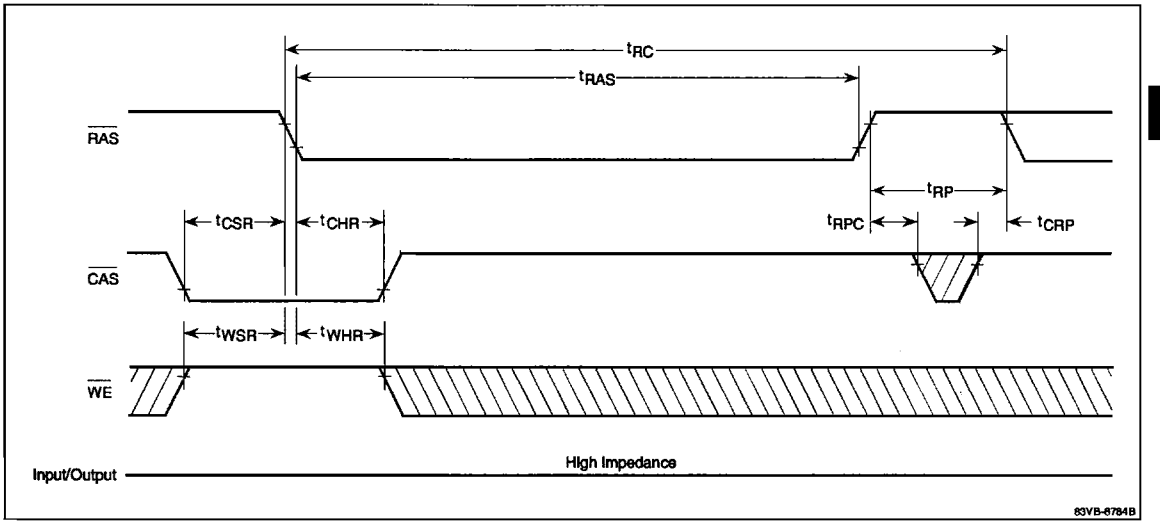


Timing Waveforms (cont)

$\overline{\text{RAS}}$-Only Refresh Cycle



$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



5d

Timing Waveforms (cont)

CBR Self-Refresh Cycle