Si3052
Si3017/11/18

GLOBAL PCI DAA CHIPSET

Features

- Si3052 PCI DAA and Si3018 global, Si3011 TBR21, or Si3017 FCC line-side DAA
- 32-bit, 33 MHz, PCI 2.3 compliant interface
- PPMI 1.1 and wake support with PME and Vaux
- Bus master and target operation, DMA controller
- 16 x 8 FIFO on DMA paths
- Interrupt controller
- Lowest cost external bill-of-material (BOM)
- Watchdog timer
- External EPROM interface
- Compliant with FCC, TBR21, JATE, and other PTTs
- 80 dB dynamic range TX/RX Path
- 2- to 4-wire Hybrid
- Patented ISOcap™ technology
- >5000 V isolation
- Wake-on-ring and ring validation
- 3.3 V digital power supply
- 64-Pin TQFP, 0 to 70 °C

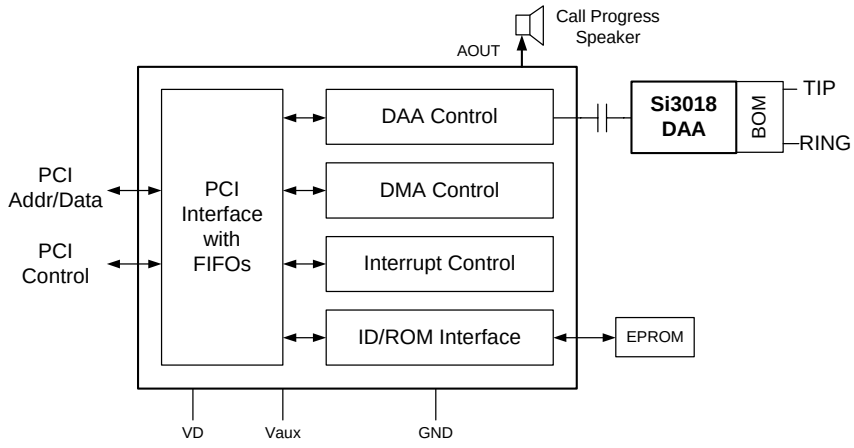
Applications

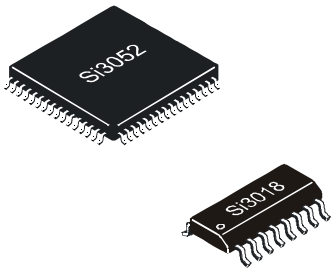
- V.92 soft data/fax modems

Description

The Si3052 is a system-side silicon direct access arrangement (DAA) device that integrates a 32-bit, 33 MHz PCI bus interface. The Si3052 is paired with the Si3018 global line-side device, Si3011 FCC/TBR21 line-side device, or Si3017 FCC line-side device. The PCI DAA chipset is compliant with global standards and includes a V.92 quality codec (80 dB SNR, –75 dB THD), dc termination (50 Ω, current limiting), ac termination (600 Ω, complex impedance), and an integrated hybrid.

Functional Block Diagram

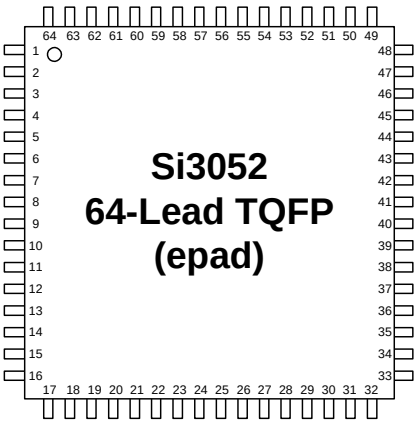




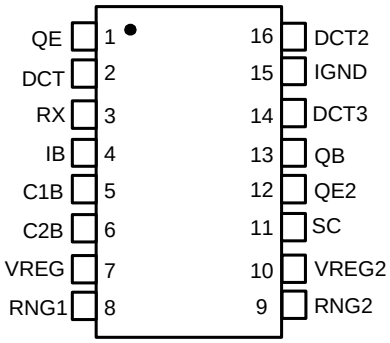
Ordering Information

See page 97.

Pin Assignments



Si3017/11/18



US Patent # 5,870,046
US Patent # 6,061,009
Patents pending

TABLE OF CONTENTS

Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	K-Grade	0	25	70	°C
Si3052 Supply Voltage, Core	VD		3.0	3.3	3.6	V
Si3052 IO Supply Voltage	V_{IO}	3.3 V Signaling	3.0	3.3	3.6	V
Si3052 IO Supply Voltage	V_{IO}	5 V Signaling	4.75	5.0	5.25	V

Note:

1. The Si3052 specifications are guaranteed when the typical application circuit (including component tolerance) and Si3052 and Si3017/11/18 are used. Refer to Figure 13 on page 16 for the typical application schematic.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.

Table 2. PCI Interface DC Characteristics for 5 V_{IO}[1]

(V_{IO} = 4.75 to 5.25 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Current, Core	$I_{D,VD}$	D0 uninitialized[2]	—	20	21	mA
		D0 initialized[3]	—	20	28	mA
		D3 wake-on-ring[4]	—	12	15	mA
		D3 deep sleep[5]	—	1	—	mA
Power Supply Current, IO	$I_{D,VIO}$	D0 uninitialized[2]	—	0.35	52	mA
		D0 initialized[3]	—	0.35	47	mA
		D3[4,5]	—	0.35	—	mA
High Level Input Voltage	V_{IH}		2.0	—	V_{IO}+0.5	V
Low Level Input Voltage	V_{IL}		–0.5	—	0.8	V
Input/Hi-Z Leakage Current	I_{IL}	$0 < V_{IN} < V_{IO}$	—	—	±10	µA
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 3 mA,6 mA[6]	—	—	0.55	V
Input Pin Capacitance	C_{in}		—	—	10	pF
CLK Pin Capacitance	C_{CLK}		5	—	12	pF
IDSEL Pin Capacitance	C_{IDSEL}		—	—	8	pF
Pin Inductance	L_{PIN}		—	4	20	nH
$\overline{PME}$ input leakage	I_{OFF}	$0 < Vo \leq 5.25$ V, V_{IO} off or floating[7]	—	—	1	µA

Notes:

1. Applies to pins AD[31:0], $\overline{CBE}$[3:0], $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{DEVSEL}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$, PAR, $\overline{INTA}$, $\overline{PME}$, $\overline{GNT}$, $\overline{REQ}$, CLK, $\overline{RESET}$, and IDSEL.
2. The D0 uninitialized condition is defined as active PCI interface and idle line-side device. Max power numbers assume constant PCI reads of worst case data using no output stepping. Typical power numbers assume no further PCI bus reads (control bits PDN = 0, PDL = 1).
3. The D0 initialized condition is defined as conducting audio through the line-side device. Max power numbers assume constant PCI reads of worst case data using no output stepping. Typical power numbers assume servicing DMA for 8 kHz audio sampling rate and two-stage output stepping (control bits PDN = 0, PDL = 0).
4. D3 condition is defined as inactive PCI bus. Wake-on-ring configuration assumes inactive PCI interface and active line-side device (control bits PDN = 1, PDL = 0).
5. D3 condition is defined as inactive PCI bus. Deep Sleep configuration assumes inactive PCI interface and line-side device (control bits PDN = 1, PDL = 1).
6. Signals without pullups have 3 mA low output current. Signals requiring pullups have 6 mA; the latter include $\overline{FRAME}$, $\overline{RDY}$, $\overline{TRDY}$, $\overline{DEVSEL}$, $\overline{STOP}$, $\overline{SERR}$, $\overline{PERR}$, $\overline{INTA}$.
7. This input leakage is the maximum leakage into the $\overline{PME}$ open drain driver when power is removed from V_{IO}, assuming that no event has occurred to cause the device to assert $\overline{PME}$.

Table 3. PCI Interface DC Characteristics for 3.3 V_{IO}[1]

(V_{IO} = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Current, Core	$I_{D,VD}$	D0 unitialized[2]	—	20	21	mA
		D0 initialized[3]	—	20	28	mA
		D3 wake-on-ring[4]	—	12	15	mA
		D3 deep sleep[5]	—	1	—	mA
Power Supply Current, IO	$I_{D,VIO}$	D0 unitialized[2]	—	0.35	36	mA
		D0 initialized[3]	—	0.35	35	mA
		D3[4,5]	—	0.35	—	mA
High Level Input Voltage	V_{IH}		0.5 V_{IO}	—	V_{IO}+0.5	V
Low Level Input Voltage	V_{IL}		–0.5	—	0.3 V_{IO}	V
Input Leakage Current	I_{IL}	$0 < V_{IN} < V_{IO}$	—	—	±10	µA
High Level Output Voltage	V_{OH}	I_O = –0.5 mA	0.9 V_{IO}	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 1.5 mA	—	—	0.1 V_{IO}	V
Input Pin Capacitance	C_{in}		—	—	10	pF
CLK Pin Capacitance	C_{CLK}		5	—	12	pF
IDSEL Pin Capacitance	C_{IDSEL}		—	—	8	pF
Pin Inductance	L_{PIN}		—	4	20	nH
$\overline{\text{PME}}$ input leakage	I_{OFF}	$0 < Vo \leq 3.6$, V_{IO} off or floating[6]	—	—	1	µA

Notes:

1. Applies to pins AD[31:0], $\overline{\text{CBE}}$[3:0], $\overline{\text{FRAME}}$, $\overline{\text{TRDY}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{STOP}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, PAR, $\overline{\text{INTA}}$, $\overline{\text{PME}}$, $\overline{\text{GNT}}$, $\overline{\text{REQ}}$, CLK, $\overline{\text{RESET}}$, and IDSEL.
2. The D0 uninitialized condition is defined as active PCI interface and idle line-side device. Max power numbers assume constant PCI reads of worst case data using no output stepping. Typical power numbers assume no further PCI bus reads (control bits PDN = 0, PDL = 1).
3. The D0 initialized condition is defined as conducting audio through the lines-side device. Max power numbers assume constant PCI reads of worst case data using no output stepping. Typical power numbers assume servicing DMA for 8 kHz audio sampling rate and 2-stage output stepping (control bits PDN = 0, PDL = 0).
4. D3 condition is defined as inactive PCI bus. Wake-on-ring configuration assumes inactive PCI interface and active line-side device (control bits PDN = 1, PDL = 0).
5. D3 condition is defined as inactive PCI bus. Deep sleep configuration assumes inactive PCI interface and line-side device (control bits PDN = 1, PDL = 1).
6. This input leakage is the maximum leakage into the $\overline{\text{PME}}$ open drain driver when power is removed from V_{IO}, assuming that no event has occurred to cause the device to assert $\overline{\text{PME}}$.

Table 4. DC Characteristics for Non-PCI pins[1]
(VD = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Max	Unit
High Level Input Voltage[2]	V_{IH}		2.0	—	V
Low Level Input Voltage[2]	V_{IL}		—	0.8	V
Input Leakage Current[2]	$I_{IL,1}$	$0 < V_{IN} < V_{IO}$	—	±10	µA
Input Leakage Current[3]	$I_{IL,2}$	$0 < V_{IN} < V_D$	—	±10	µA
High Level Output Voltage[2]	V_{OH}	IO = –2 mA	2.4	—	V
		IO = –7.5 mA	2.0	—	V
Low Level Output Voltage[2]	V_{OL}	IO = 2 mA	—	0.35	V
	V_{OL}	IO = 8 mA	—	0.8	V
Input Pin Capacitance	C_{in}		—	10	pF

Notes:
1. Applies to PIN_37, PIN_38, VAUX_SENSE, XIN, XOUT, C1A, C2A.
2. Applies to 5 V-tolerant 3.3 V pins PIN_37, PIN_38, and VAUX_SENSE.
3. Applies to 3.3 V pins XIN, XOUT, C1A, C2A.

Table 5. PCI Interface AC Characteristics for $5V_{IO}$[1]

(V_{IO} = 4.75 to 5.25 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Max	Unit
Switching Current, High[2]	$I_{OH(AC)}$	$0 < V_{OUT} < 1.4$[3]	–44	—	mA
		$1.4 < V_{OUT} < 2.4$[3]	$–44 + (V_{OUT} – 1.4)/0.024$	—	mA
		$3.1 < V_{OUT} < V_{IO}$[3]	—	$11.9 \times (V_{OUT}-5.25) \times (V_{OUT}+2.45)$	mA
		V_{OUT} = 3.1 (Test Point)	—	–142	mA
Switching Current, Low	$I_{OH(AC)}$	$V_{OUT} \geq 2.2$[3]	95	—	mA
		V_{OUT} = 1.375	32	—	mA
		$2.2 > V_{OUT} > 0.55$[3]	$V_{OUT}/0.023$	—	mA
		$0.71>V_{OUT}>0$[3]	—	$78.5 \times V_{OUT} \times (4.4 – V_{OUT})$	mA
		V_{OUT} = 0.71 (Test Point)	—	206	mA
Low Clamp Current	I_{CL}	$-5<V_{IN}<-1$	$–25 + (V_{IN}+1)/0.015$	—	mA
High Clamp Current	I_{CH}	$V_{IO} + 1 < V_{IN} < V_{IO} + 4$	$–25 + (V_{IN} – V_{IO} – 1)/0.015$	—	mA
Output Rise Slew Rate	$slew_R$	0.4 to 2.4 V[4]	1	5	V/ns
Output Fall Slew Rate	$slew_F$	2.4 to 0.4 V[4]	1	5	V/ns

Notes:

1. Applies to pins AD[31:0], $\overline{\text{CBE}}$[3:0], $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{TRDY}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{STOP}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, PAR, $\overline{\text{INTA}}$, $\overline{\text{PME}}$, $\overline{\text{GNT}}$, $\overline{\text{REQ}}$, and IDSEL.
2. Switching current High parameters do not apply to open-drain signals $\overline{\text{SERR}}$, $\overline{\text{PME}}$, and $\overline{\text{INTA}}$.
3. Outputs are characterized to meet switching current templates. I_{OH} is tested at 1.4 V and 2.4 V only. I_{OL} is tested at 0.53 V and 1.375 V only.
4. Cumulative edge rate across the specified range with load of 1 kΩ to V_{IO}, 1 kΩ to ground and 10 pF to ground.

Table 6. PCI Interface AC Characteristics for 3.3V_{IO}[1]

(V_{IO} = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Max	Unit
Switching Current, High[2]	$I_{OH(AC)}$	$0 < V_{OUT} < 0.3\ V_{IO}$[3]	$-12\ V_{IO}$	—	mA
		$0.3\ V_{IO} < V_{OUT} < 0.9\ V_{IO}$[3]	$-17.1(V_{IO} - V_{OUT})$	—	mA
		$0.7\ V_{IO} < V_{OUT} < V_{IO}$[3]	—	$(98/V_{IO}) \times (V_{OUT} - V_{IO}) \times (V_{OUT} - 0.4\ V_{IO})$	mA
		$V_{OUT} = 0.7\ V_{IO}$ (Test Point)	—	$-32\ V_{IO}$	mA
Switching Current, Low	$I_{OH(AC)}$	$V_{IO} > V_{OUT} \geq 0.6V_{IO}$[3]	$16\ V_{IO}$	—	mA
		$0.6 > V_{OUT} > 0.1V_{IO}$[3]	$26.7\ V_{OUT}$	—	mA
		$0.18\ V_{IO} > V_{OUT} > 0$[3]	—	$(256/V_{IO}) \times V_{OUT} \times (V_{IO} - V_{OUT})$	mA
		$V_{OUT} = 0.71$ (Test Point)	—	$38xV_{IO}$	mA
Low Clamp Current	I_{CL}	$-3 < V_{IN} \leq 1$	$-25 + (V_{IN} + 1)/0.015$	—	mA
High Clamp Current	I_{CH}	$V_{IO} + 1 \leq V_{IN} < V_{IO} + 4$	$-25+(V_{IN} - V_{IO} - 1)/0.015$	—	mA
Output Rise Slew Rate	$slew_R$	$0.2\ V_{IO}$ to $0.6\ V_{IO}$[4]	1	4	V/ns
Output Fall Slew Rate	$slew_F$	$0.6\ V_{IO}$ to $0.2\ V_{IO}$[4]	1	4	V/ns

Notes:

1. Applies to pins AD[31:0], $\overline{CBE}$[3:0], $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{DEVSEL}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$, PAR, $\overline{INTA}$, $\overline{PME}$, $\overline{GNT}$, $\overline{REQ}$, and IDSEL.
2. Switching current high parameters do not apply to open-drain signals $\overline{SERR}$, $\overline{PME}$, and $\overline{INTA}$.
3. Outputs are characterized to meet switching current templates. Production testing is done at the designated Test Point voltages only.
4. Cumulative edge rate across the specified range with load of 1 kΩ to V_{IO}, 1 kΩ to ground and 10 pF to ground.

Table 7. PCI Interface Timing Characteristics

(V_D = 3.0 to 3.6 V, V_{IO} = 3.0 to 5.25 V, T_A = 0 to 70 °C, see Figure 1)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PCICLK Cycle Time	t_{cyc}		30	—	—	ns
PCICLK High Time	t_{high}		11	—	—	ns
PCICLK Low Time	t_{low}		11	—	—	ns
PCICLK to Signal Valid Delay—Bused Signals[1]	t_{val}		2	—	11	ns
PCICLK to Signal Valid Delay—Point to Point[1,3]	$t_{val(ptp)}$		2	—	12	ns
Float to Active Delay[2]	t_{on}		2	—	—	ns
Active to Float Delay[2]	t_{off}		—	—	28	ns
Input Setup Time to PCICLK—Bused Signals	t_{su}		7	—	—	ns
Input Setup Time to PCICLK—Point to Point[3]	$t_{su(ptp)}$		10	—	—	ns
Input Hold Time for PCICLK	t_h		0	—	—	ns
Reset Active to Output Float Delay[2]	$t_{rst-off}$		—	—	30	ns

Notes:

1. For 5 V signaling, T_{val} is evaluated with 50 pF load to ground. For 3.3 V signaling, T_{val} is evaluated with 25 Ω in parallel with 10 pF to ground (rising) or 25 Ω to V_{IO} with 10 pF to ground (falling).
2. For purposes of identifying float timing measurements, the Hi-Z or off state is defined to be when the total current is less than or equal to the leakage current specification.
3. The point-to-point signals are $\overline{REQ}$ and $\overline{GNT}$.

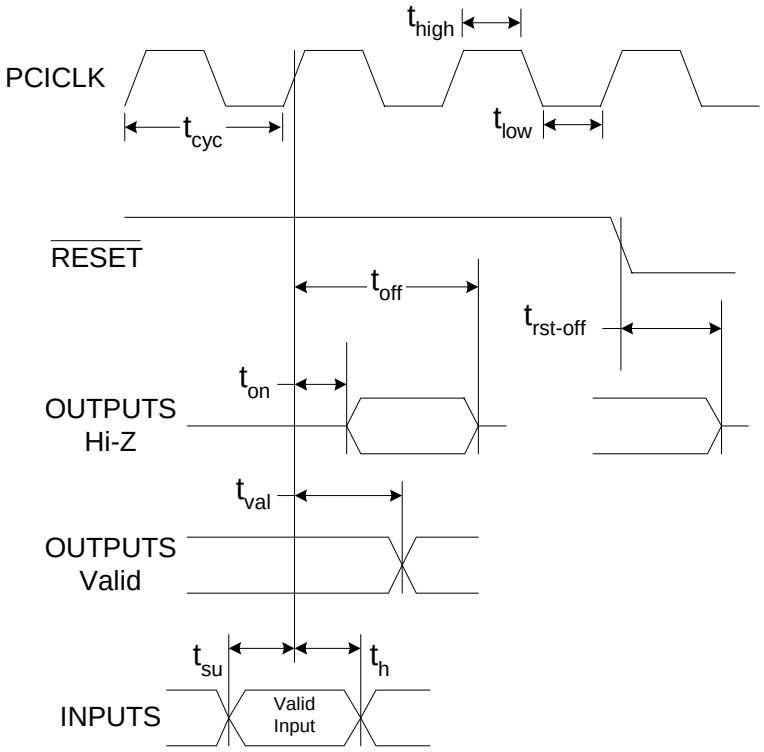


Figure 1. PCI Timing

Table 8. DAA Loop Characteristics[1]

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, see Figure 2)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0	9	—	—	V
DC Termination Voltage[2]	V_{TR}	I_L = 20 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	—	—	7.5	V
DC Termination Voltage[2]	V_{TR}	I_L = 120 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	—	—	40	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 1	—	—	16	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 1	40	—	—	V
On-Hook Leakage Current[2]	I_{LK}	V_{TR} = –48 V	—	—	5	µA
Operating Loop Current[2]	I_{LP}	MINI = 00, ILIM = 0	10	—	120	mA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 1	10	—	60	mA
DC Ring Current[2]		dc current flowing through ring detection circuitry	—	1.5	3	µA
Ring Detect Voltage[2,3]	V_{RD}	RT = 0	12	15	18	V_{rms}
Ring Detect Voltage[3]	V_{RD}	RT = 1	18	21	25	V_{rms}
Ring Frequency[2]	F_R		13	—	68	Hz
Ringer Equivalence Number[2]	REN		—	—	0.2	

Notes:

1. All parameters apply to Si3018 Global and Si3011 TBR21 line-side devices.
2. Parameter applies to Si3017 FCC line-side device.
3. The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.

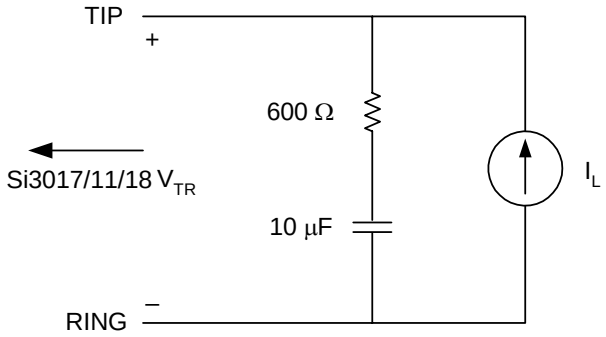


Figure 2. Test Circuit for Loop Characteristics

Table 9. DAA AC Characteristics[1]

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, Fs = 8 kHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate[2]	Fs		7.2	—	16	kHz
Receive Frequency Response[2]		Low –3 dBFS Corner	—	5	—	Hz
Transmit Full Scale Level[2,3]	V_{FS}	0 dBm	—	1.1	—	V_{PEAK}
Receive Full Scale Level[2,3,4]	V_{FS}	0 dBm	—	1.1	—	V_{PEAK}
Dynamic Range[2,5,6,7]	DR	ILIM = 0, DCV = 11, MINI = 00 DCR = 0, I_L = 100 mA	—	78	—	dB
Dynamic Range[5,6,8]	DR	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I_L = 20 mA	—	79	—	dB
Dynamic Range[5,6,9]	DR	ILIM = 1, DCV = 11, MINI = 00 DCR = 0, I_L = 50 mA	—	78	—	dB
Transmit Total Harmonic Distortion[7,8]	THD	ILIM = 0, DCV = 11, MINI = 00 DCR = 0, I_L = 100 mA	—	–72	—	dB
Transmit Total Harmonic Distortion[2,7,8]	THD	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I_L = 20 mA	—	–78	—	dB
Receive Total Harmonic Distortion[7,8]	THD	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I_L = 20 mA	—	–78	—	dB
Receive Total Harmonic Distortion[7,8]	THD	ILIM = 1,DCV = 11, MINI = 00 DCR = 0, I_L = 50 mA	—	–78	—	dB
Dynamic Range (caller ID mode)[2,7]	DR_{CID}	V_{IN} = 1 kHz, –13 dBm	—	50	—	dB
Caller ID Full Scale Level[2]	V_{CID}		—	6	—	V_{PP}

Notes:

1. All parameters apply to Si3018 Global and Si3011 TBR21 line-side devices.
2. Parameter applies to Si3017 FCC line-side device.
3. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 2.
4. Receive full scale level produces –0.9 dBFS.
5. DR = 20 x log (rms V_{FS}/rms V_{IN})+ 20 x log (rms V_{IN}/rms noise). V_{FS} is the 0 dBm full-scale level.
6. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
7. V_{IN} = 1 kHz, –3 dBFS
8. THD = 20 x log (rms distortion / rms signal).
9. DR_{CID} = 20 x log (rms V_{CID}/rms V_{IN})+ 20 x log (rms V_{IN}/rms noise). V_{CID} is the 6 V full-scale level.

Table 10. Digital FIR Filter Characteristics—Transmit and Receive
(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1 dB)	$F_{(0.1\ dB)}$	0	—	3.3	kHz
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t_{gd}	—	12/Fs	—	s
Note: Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 3, 4, 5, and 6.					

Table 11. Digital IIR Filter Characteristics—Transmit and Receive
(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.2	—	0.2	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–40	—	—	dB
Group Delay	t_{gd}	—	1.6/Fs	—	s
Note: Typical IIR filter characteristics for Fs = 8000 Hz are shown in Figures 7, 8, 9, and 10. Figures 11 and 12 show group delay versus input frequency.					

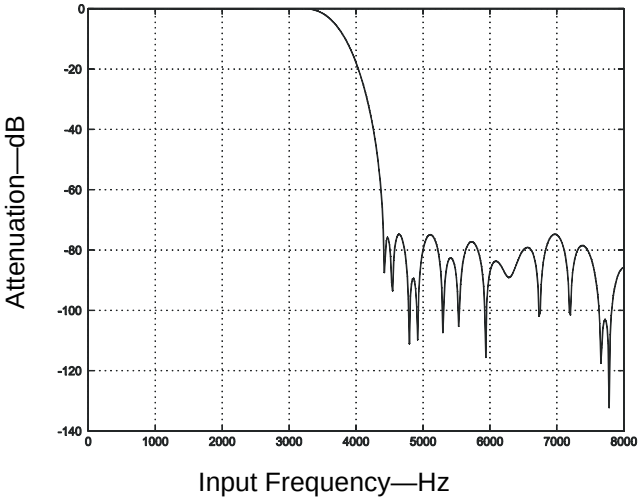


Figure 3. FIR Receive Filter Response

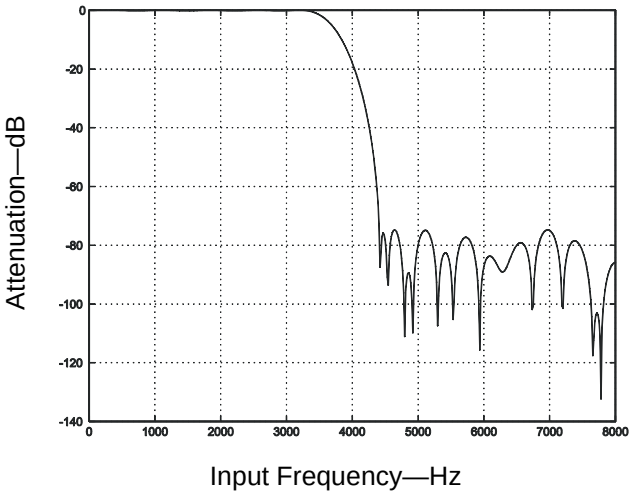


Figure 5. FIR Transmit Filter Response

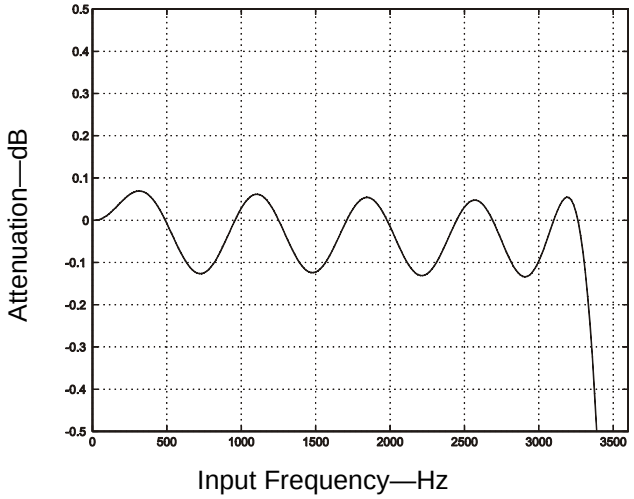


Figure 4. FIR Receive Filter Passband Ripple

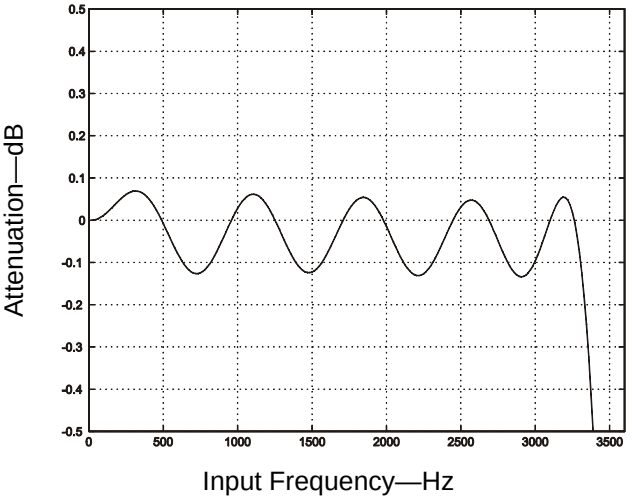


Figure 6. FIR Transmit Filter Passband Ripple

For Figures 3–6, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$F_{(0.1\ dB)}$ = 0.4125 Fs

$F_{(-3\ dB)}$ = 0.45 Fs

where Fs is the sample frequency.

For Figures 7–10, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$F_{(-3\ dB)}$ = 0.45 Fs

where Fs is the sample frequency.

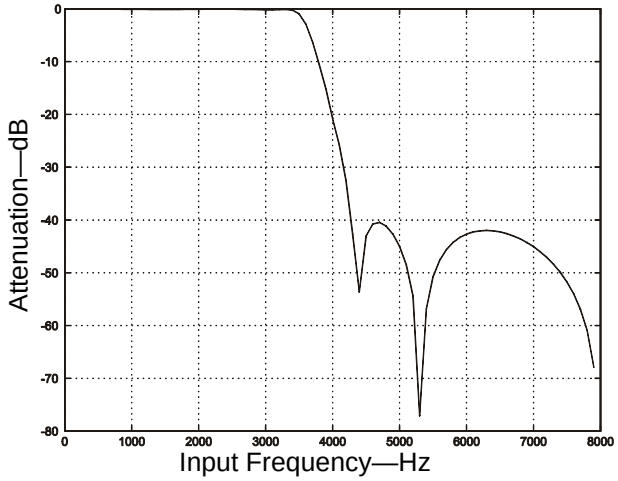


Figure 7. IIR Receive Filter Response

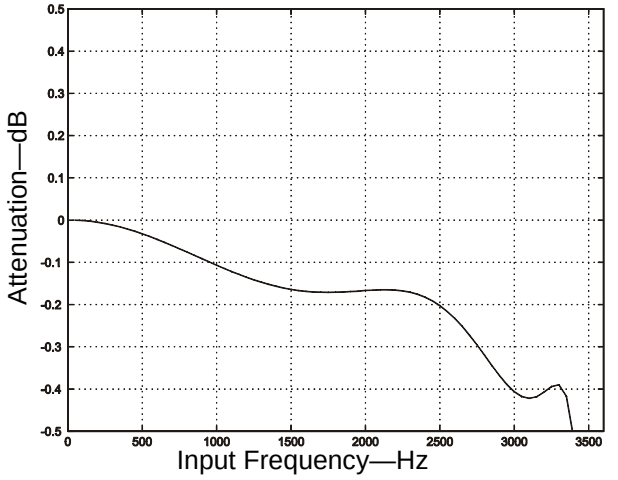


Figure 10. IIR Transmit Filter Passband Ripple

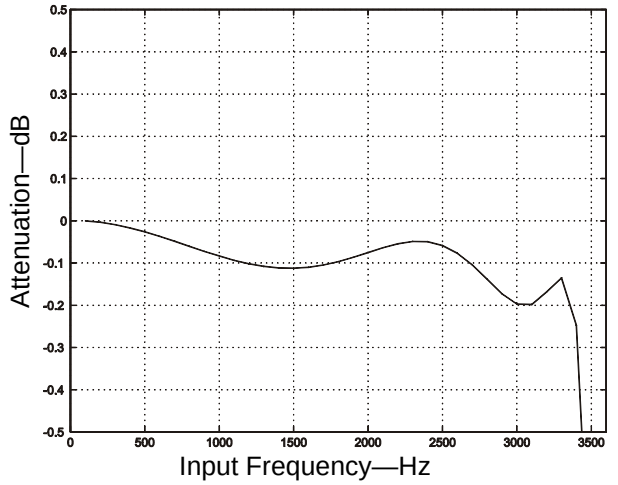


Figure 8. IIR Receive Filter Passband Ripple

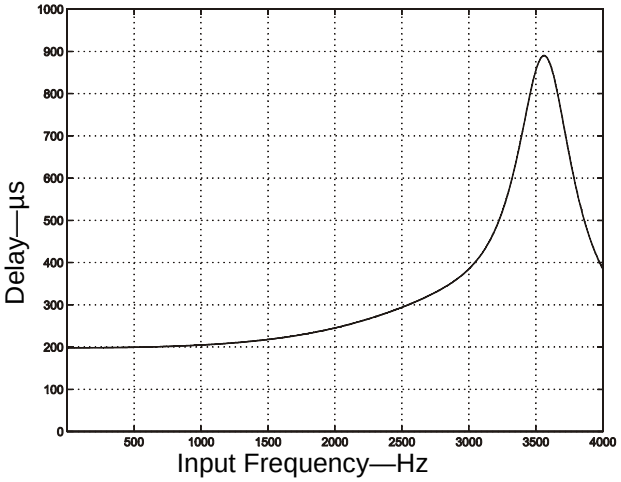


Figure 11. IIR Receive Group Delay

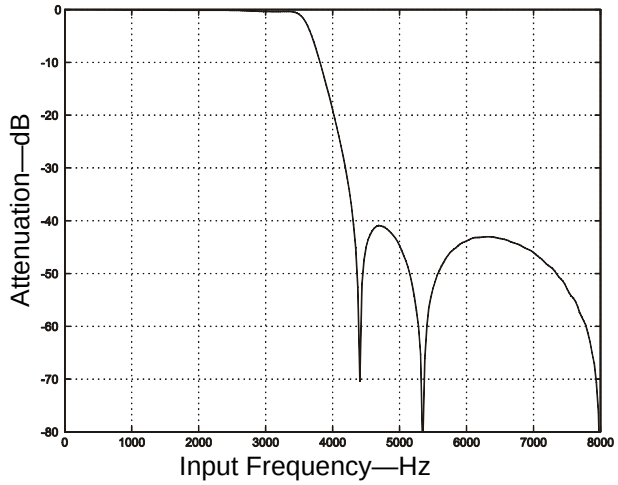


Figure 9. IIR Transmit Filter Response

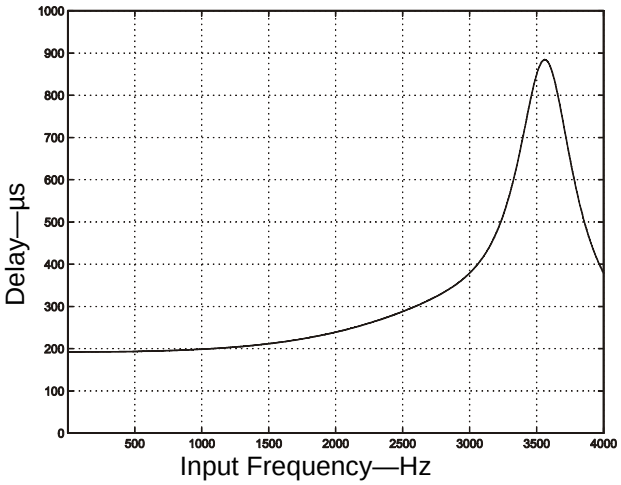


Figure 12. IIR Transmit Group Delay

Typical Application Schematic

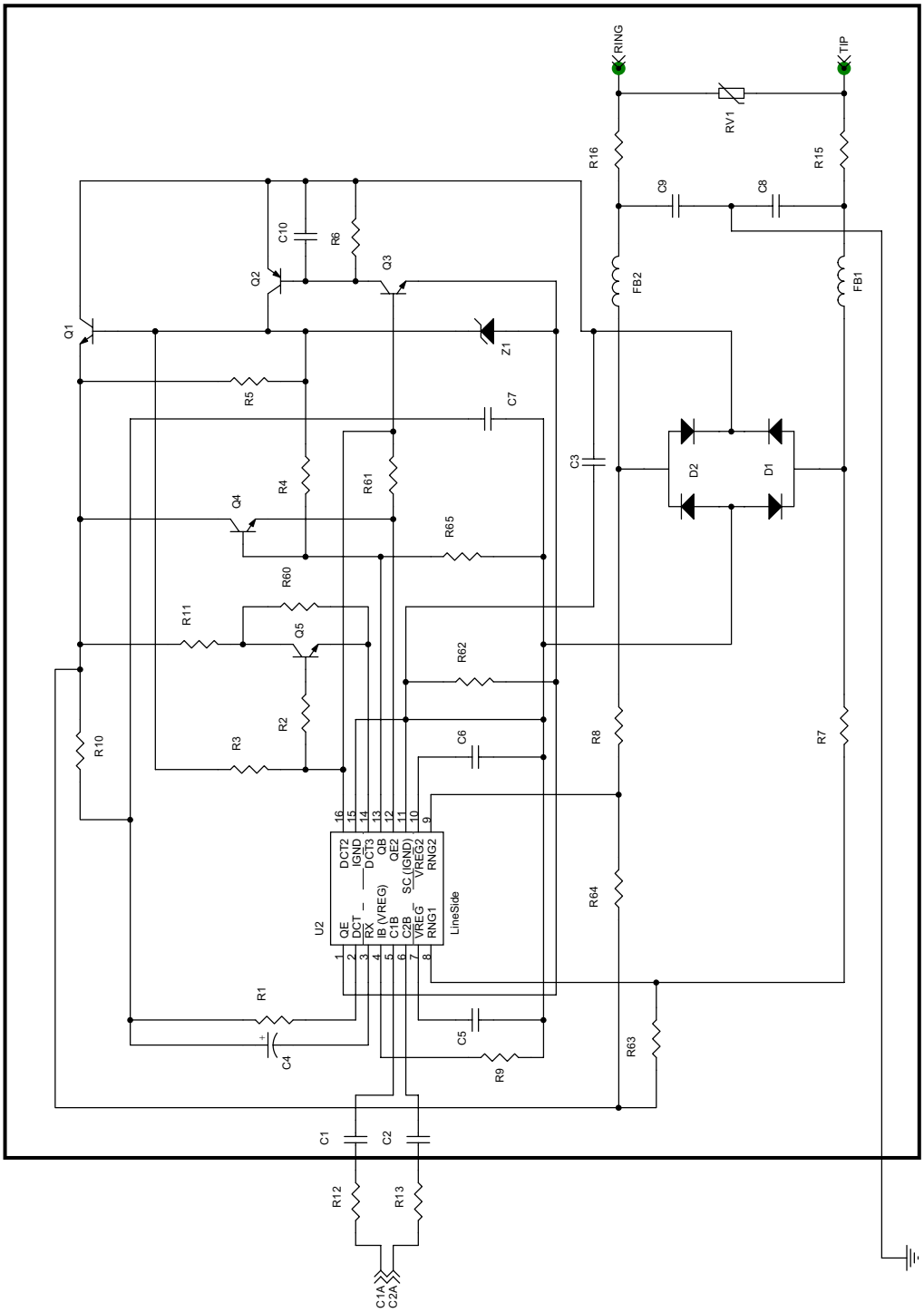


Figure 13. Si3052 and Si3017/11/18 Typical Application Schematic (1 of 2)

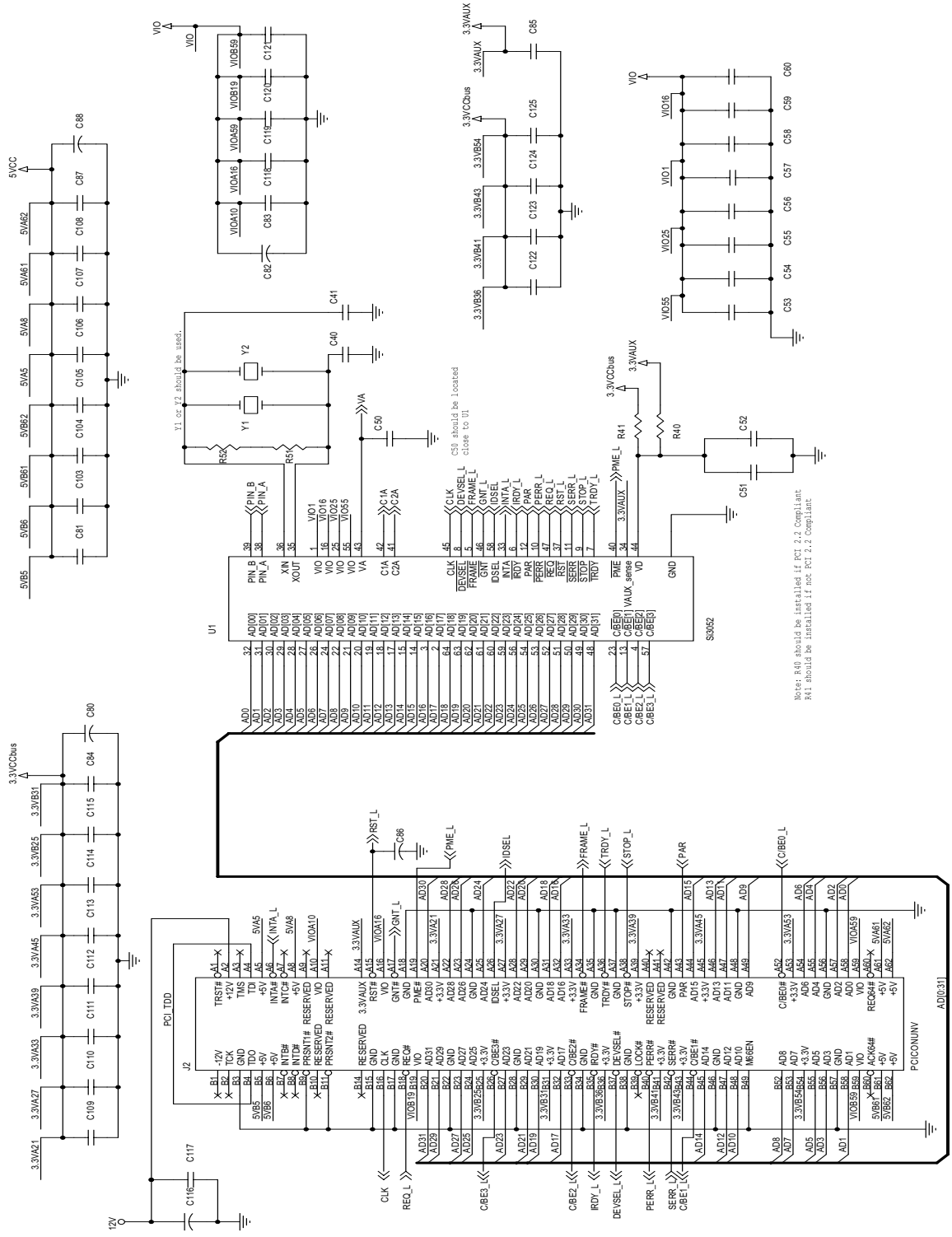


Figure 14. Si3052 and Si3017/11/18 Typical Application Schematic (2 of 2)

Bill of Materials

Component(s)	Value	Supplier(s)
C1, C2	33pF, Y2, X7R, ±20%	Panasonic, Murata, Vishay
C3	10 nF, 250 V, X7R, ±20%	Venkel, SMEC
C4	1.0 μF, 35 V, Elec/Tant, ±20%	Panasonic
C5, C6, C50, C117[1]	0.1 μF, 16 V, X7R, ±20%	Venkel, SMEC
C7	2.7 nF, 50 V, X7R, 20%	Venkel, SMEC
C8, C9	680 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C10, C52-C53, C56–C57, C60, C81, C84–C87, C103–C115, C123–C125[1]	0.01 μF, 16 V, X7R, ±20%	Venkel, SMEC
C40–41	22 pF, 50 V, COG, ±5%	Venkel, SMEC
C51,C54,C55,C58,C59[1]	1.0 μF, 16 V, X7R, ±20%	Venkel, SMEC
C81-C82, C85-C86, C88[1]	1.0uF, 16V, X7R, ±20%	Venkel, SMEC
C80, C82, C88, C116[1]	10 μF, 16 V, Elec, ±20%	Panasonic
C83, C118, C119, C120, C121[1]	0.047 μF, 16 V, X7R, ±20%	Venkel, SMEC
D1, D2[2]	Dual Diode, 225 mA, 300 V, CMPD2004S	Central Semiconductor
FB1, FB2	Ferrite Bead, BLM21AJ601S	Murata
Q1, Q3	NPN, 300 V, MMBTA42	Fairchild, OnSemi, Central Semi
Q2	PNP, 300 V, MMBTA92	Fairchild, OnSemi, Central Semi
Q4, Q5	NPN, 80 V, 330 mW, MMBTA06	Fairchild, OnSemi, Central Semi
RV1	Sidactor, 275 V, 100 A	Teccor, Protek, ST Micro
R1	1.07 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R2	150 Ω, 1/16 W, 5%	Venkel, SMEC, Panasonic
R3	3.65 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R4	2.49 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R5, R6	100 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R7, R8	20 MΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R9	1 MΩ, 1/16 W, 1%	Venkel, SMEC, Panasonic
R10	536 Ω, 1/4 W, 1%	Venkel, SMEC, Panasonic

Notes:

1. Decoupling capacitors based on PCI Specification Rev 2.2.
2. Several diode bridge configurations are acceptable; parts, such as a single DF-04S or four 1N4004 diodes, may be used (suppliers include General Semiconductor, Diodes Inc., etc.).
3. A 56 Ω, 1%, 1/16 W resistor may be used if needed for R12–R13 (0 Ω) to decrease emissions.
4. Murata BLM21AJ601S may be used if needed for R15–R16 (0 Ω) to decrease emissions.
5. R40 should be populated with a 0 Ω resistor if 3.3 V aux is present; otherwise, R41 should be populated with a 0 Ω resistor.
6. Required for compatibility with future line-side devices.

Component(s)	Value	Supplier(s)
R11	73.2 Ω, 1/2 W, 1%	Venkel, SMEC, Panasonic
R12, R13[3]	0 Ω, 1/16 W	Venkel, SMEC, Panasonic
R15, R16[5]	0 Ω, 1/16 W	Venkel, SMEC, Panasonic
R40[5]	0 Ω, 1/16 W	Venkel, SMEC, Panasonic
R41[5], R60–R64[6]	NI	Venkel, SMEC, Panasonic
R51, R52	20 MΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
U1	Si3052	Silicon Labs
U2	Si3017/11/18	Silicon Labs
Y1	32.768 kHz, 50 ppm	ECS, Epson, CTS
Z1	Zener Diode, 43 V, 1/2 W	General Semiconductor, Diodes Inc.

Notes:

1. Decoupling capacitors based on PCI Specification Rev 2.2.
2. Several diode bridge configurations are acceptable; parts, such as a single DF-04S or four 1N4004 diodes, may be used (suppliers include General Semiconductor, Diodes Inc., etc.).
3. A 56 Ω, 1%, 1/16 W resistor may be used if needed for R12–R13 (0 Ω) to decrease emissions.
4. Murata BLM21AJ601S may be used if needed for R15–R16 (0 Ω) to decrease emissions.
5. R40 should be populated with a 0 Ω resistor if 3.3 V aux is present; otherwise, R41 should be populated with a 0 Ω resistor.
6. Required for compatibility with future line-side devices.

AOUT PWM Output

Figure 15 illustrates an optional circuit to support the pulse-width modulation (PWM) output capability of the Si3052 for call progress monitoring. This mode is enabled by setting the PWME bit (Offset 0x31).

The AOUT signal is a standard digital output from PIN_39, which represents the sum of independently-scalable receive and transmit call progress contents in pulse-width modulation (PWM) form. The sampling rate of the audio path signals is 32 kHz. The format of the PWM is configurable by the PWMM bits (Offset 0x31). ARM[1:0] and ATM[1:0] (Offset 0x36) control receive and transmit gains in 6 dB steps and receive and transmit muting. Alternatively, ARM[7:0] and ATM[7:0] (Offset 0x44 and 0x45) control gains and muting with finer resolution. These registers allow the receive and transmit paths to be independently controlled and attenuated linearly. Setting these 8-bit registers to all 0s mutes the receive and transmit paths. These registers affect the call progress output only and do not affect transmit and receive operations on the telephone line.

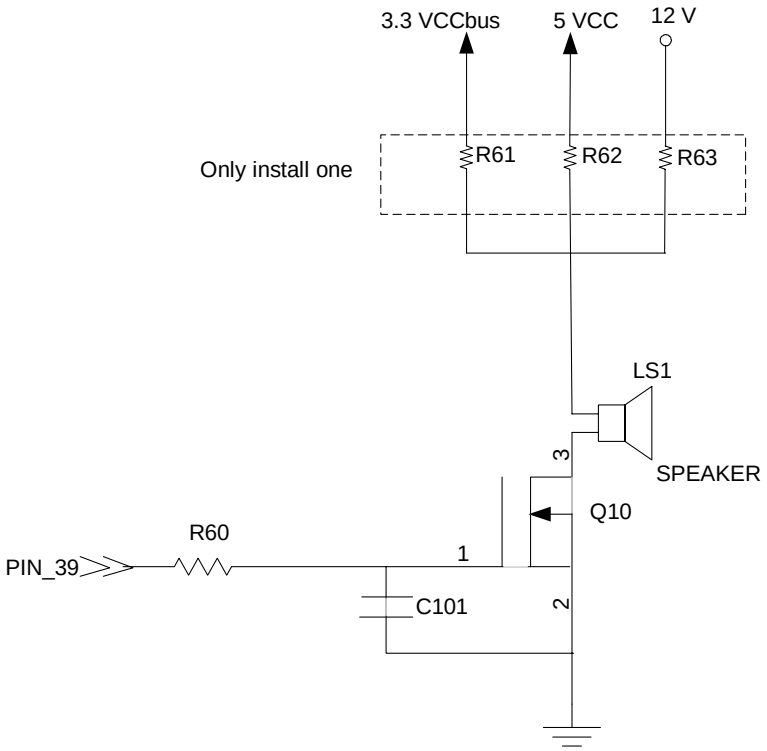


Figure 15. AOUT PWM Circuit for Call Progress

Table 12. Component Values—AOUT PWM

Component	Value	Supplier(s)
C101	1 nF, 16 V, X7R, ±20%	Venkel, SMEC
LS1	BRT1209PF-06	Intervox
Q10	MOSFET N GSD, FDV301N	Fairchild
R60	15 kΩ, 1/10 W, 5%	Venkel, SMEC, Panasonic
R61	0 Ω, 1/10 W, 5%	Venkel, SMEC, Panasonic
R62, R63	NI	

PCI Functional Description

The Si3052 provides the interface between a PCI 2.3-compliant bus and the Si3018 using the Silicon Laboratories' proprietary ISOcap™ technology. The Si3052 has several major functional blocks including DMA, bus mastering, DAA control/status, power management, PNP configuration, EPROM interface, interrupt control/status, FIFO buffering, and a watchdog timer. Table 13 on page 23 indicates which PCI commands are supported and the method of implementation. The PCI timing for write, read, and arbitration operations is shown in Figures 15 through 17.

DMA Bus Master Operation

The Si3052 supports DMA bus master for write and read operations to memory. A DMA write is a data transfer from memory to the Si3052 FIFO buffers. A DMA read is a data transfer from the Si3052 FIFO buffers to memory. Separate registers are defined and configured for independent operation of DMA read and DMA write.

DMA Master Transfer Setup

A DMA transfer is set up by programming the DMA start address register (read or write) and DMA end address register (read or write) to physical memory locations. The size of the data transfer is calculated as the difference between the DMA start and end memory address locations. The DMA start and end memory addresses must be on a double-word (4-byte) boundary.

A programming sequence for a DMA write is as follows:

1. Allocate DMA memory buffer (non-cacheable, continuous).
2. Set DMA write start address register to physical memory address.
3. Set DMA write end address register to physical memory address.
4. Fill DMA write FIFO buffer.
5. Set DMA control register start bit.

To start the DMA operation, set the DMA enable bit (Offset 0x00, bit 8). To stop the DMA operation, clear this bit. DMA restart bit (Offset 0x00, bit 9) restarts the DMA operation in single mode but is ignored in multiple mode.

When the DMA is setup, the processor can use a polling routine to monitor the current DMA status and process the FIFO read and FIFO write buffers. Base the polling interval on the size of the allocated DMA memory buffer.

DMA Master Status

DMA status is monitored by reading the current DMA address (Offset 0x14 read and 0x24 write) or by programming the DMA interrupt address register (Offset 0x10 read and 0x20 write). The current DMA address register (read or write) contains the physical memory address of the DMA operation in progress. If the DMA Interrupt Address register (read or write) is programmed, an interrupt is generated and the interrupt status register flag (Offset 0x04) is set when the DMA transfer reaches the interrupt address. When the flag is set, it is cleared by setting the interrupt status register flag.

The DMA Status register (Offset 0x04, bits 3:0) contains the status of the current DMA operation. Each bit generates an interrupt if the corresponding mask bit is set. If the PCI bus master logic detects an abort condition, the DMA Status register (Offset 0x04, bits 5:4) is set based on the abort condition. The DMA Status register is cleared by reading the register value. To recover the PCI bus master state machine, clear the DMA reset bit in the DMA Control register (Offset 0x00, bit 1) and enable DMA operation by setting the DMA enable bit in the DMA Control register (Offset 0x00, bit 8).

DMA Master Control

The DMA interrupt mode bit (Offset 0x00, bit 6) configures the interrupt mode. For level trigger mode, the interrupt occurs when the event happens and the status bit remains set as long as the conditions that created the interrupt remain active. In level trigger mode, the status bit is non-sticky. For edge trigger mode, the interrupt occurs when the event happens and the status bit remains set until cleared by setting the DMA Status register. In edge trigger mode, the status bit is sticky.

The DMA master mode bit (Offset 0x00, bit 7) configures the DMA operation mode. In multiple mode, the DMA address wraps around to the starting address when the ending address is reached. In single mode, the DMA stops when it reaches the end address. The advantage of multiple DMA mode over single DMA mode is that the Si3052 continuously transfers data without processor intervention. The single DMA mode has a control flow similar to the PC core logic DMA controller.

DAA Control

The DAA registers are accessed by either direct or indirect methods. The access mode is selected by the data mode bits (Offset 0x00, bits 11, 12).

Direct DAA Register Access

The DAA registers are accessed directly through either memory or I/O cycles. For memory accesses, the base address is set in PCI configuration register 10h. For I/O

accesses, the base address is set in PCI configuration register 14h. Memory and I/O cycles are used interchangeably to access internal registers.

Indirect DAA Register Access

The DAA registers can be indirectly accessed through the DMA master write buffer. The DMA write buffer can contain DAA control and data. This is equivalent to having a primary timeslot for modem data and a secondary timeslot for control data. If data mode (Offset 0x00, bits 12:11) is set to indirect, the LSB of the 16-bit transmit word is used as a flag to indicate control address/data in the DMA write buffer. If the LSB is 1, the transmit word is interpreted as control address/data and written to the corresponding control register. Only 15-bit data is transmitted resulting in a loss of SNR but allowing efficient access to DAA control registers.

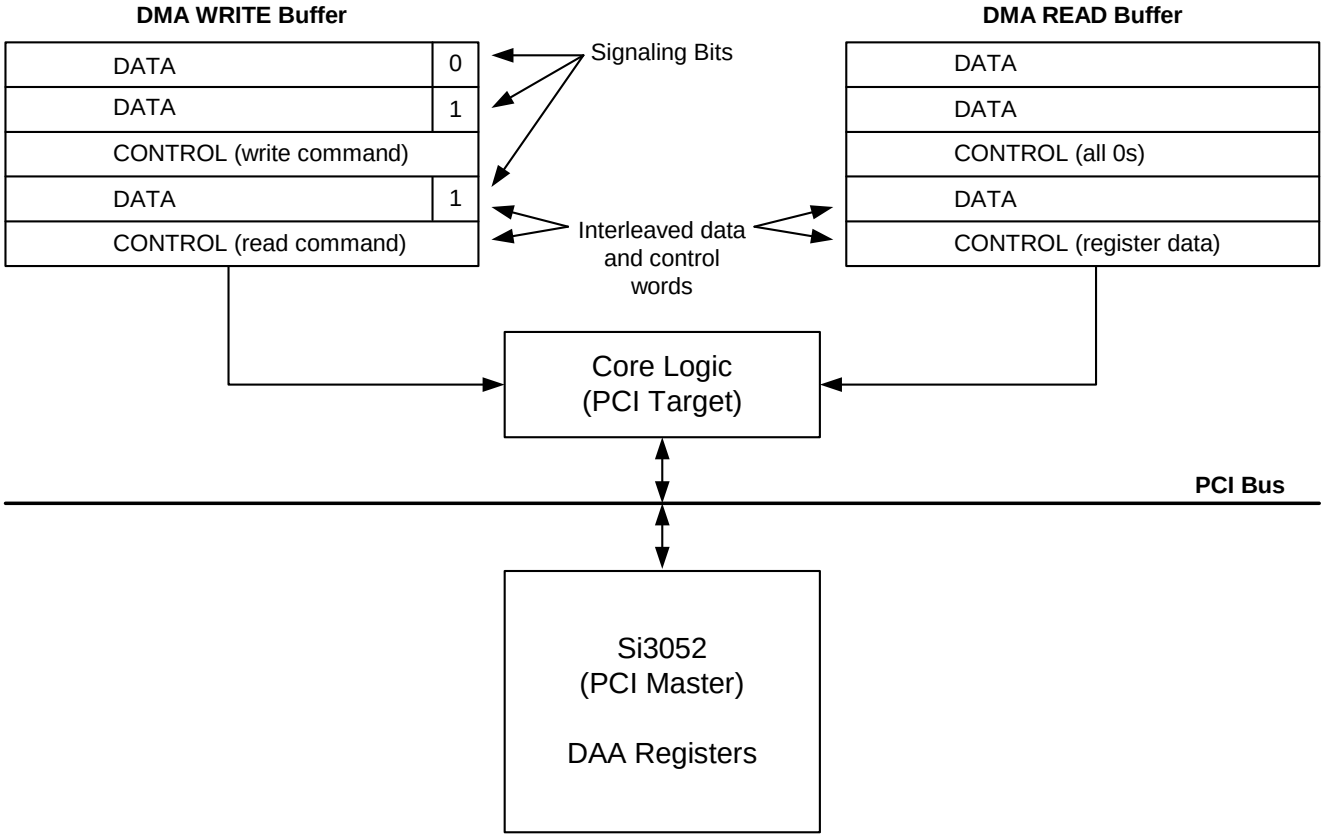


Figure 16. Indirect DAA Register Access

Table 13. PCI Command Summary

C/$\overline{BE}$[3:0]	Command Type	Implementation
0000	Interrupt Acknowledge	Not Supported
0001	Special Cycle	Not Supported
0010	I/O Read	Supported
0011	I/O Write	Supported
0100	Reserved	
0101	Reserved	
0110	Memory Read	Support only linear addressing mode
0111	Memory Write	Support only linear addressing mode
1000	Reserved	
1001	Reserved	
1010	Configuration Read	Supported
1011	Configuration Write	Supported
1100	Memory Read Multiple	Aliases to Memory Read
1101	Dual Address Cycle	Not Supported
1110	Memory Ready Line	Aliases to Memory Read
1111	Memory Write and Invalidate	Aliases to Memory Write

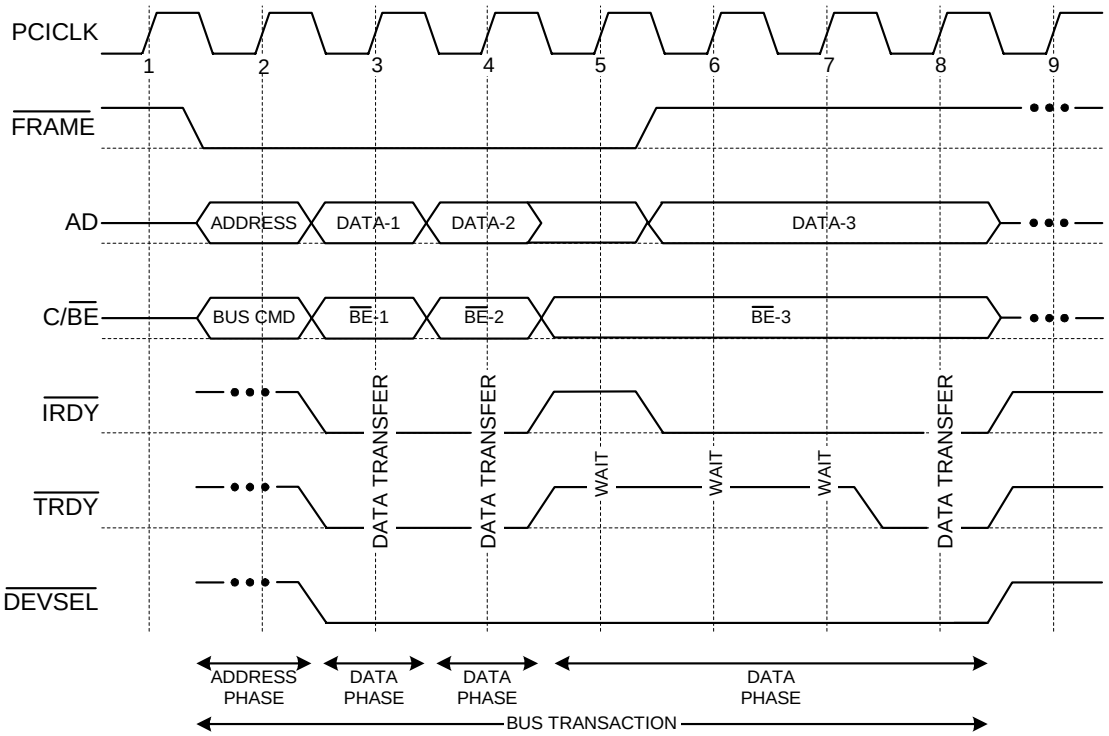


Figure 17. PCI Write Operation

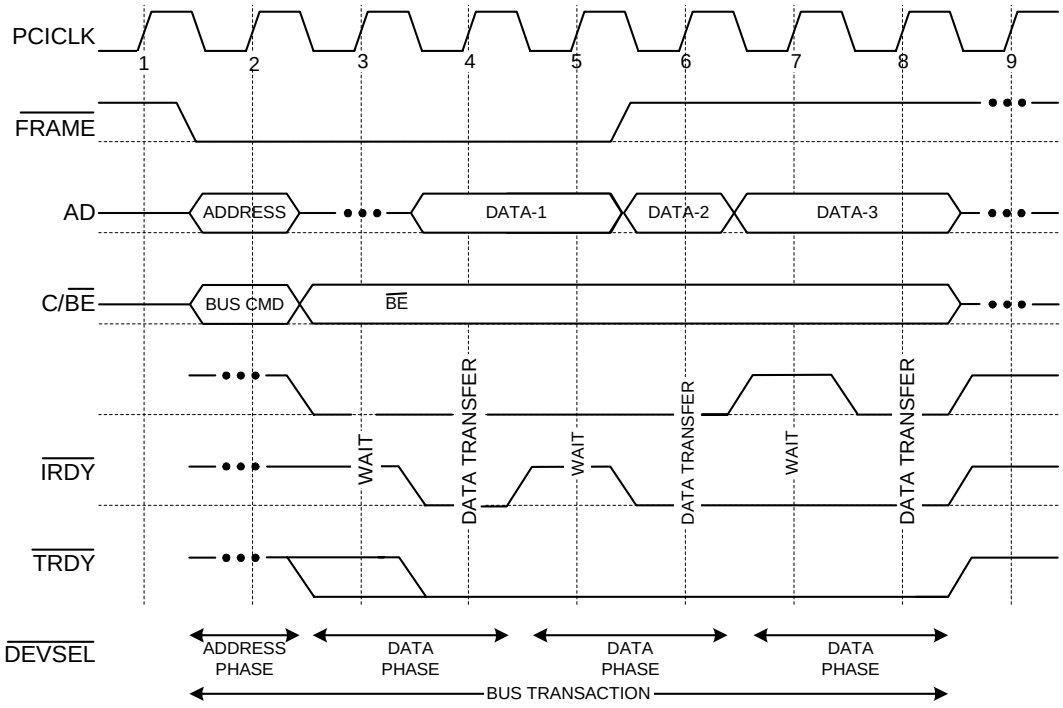


Figure 18. PCI Read Operation

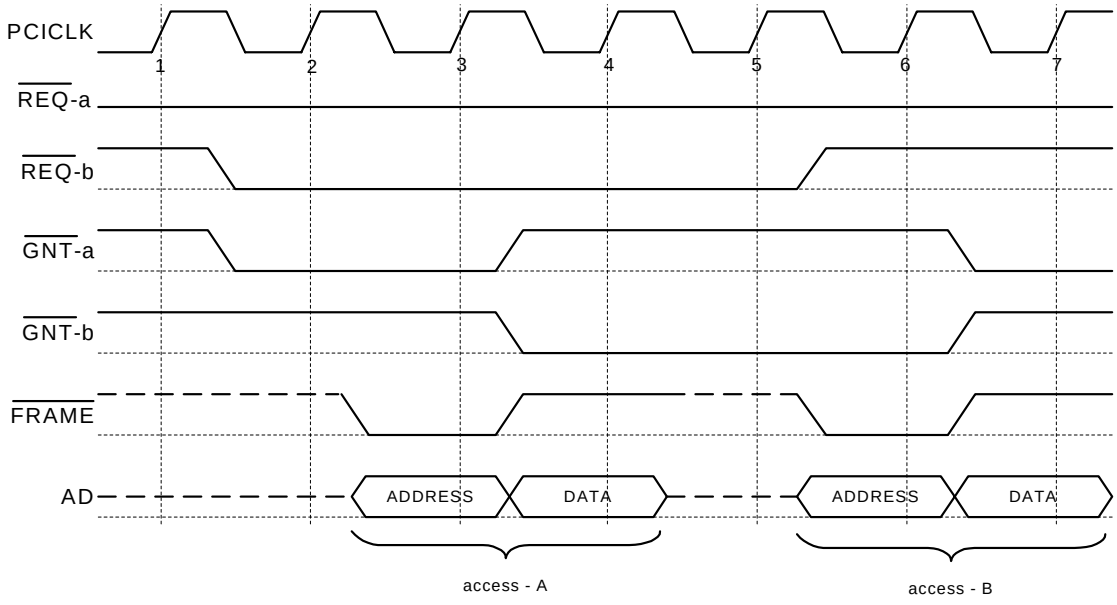


Figure 19. PCI Arbitration

Power Management

The Si3052 conforms to the PCI Bus Power Management Specification, Revision 1.1. The PCI functions operate between the D0 and D3 power states. The PCI Bus controller operates between the B0 and B3 bus power states.

D0 Uninitialized State

D0 Uninitialized is the default condition after either a warm or a cold reset. 3.3 V is available from the PCI power bus to power all PCI I/O pads and non-Vaux PCI core logic. 3.3 V Vaux is available for all Vaux-power I/O and logic. Powerdown (Offset 0x36, bit 3) defaults low (inactive) and Powerdown Link (Offset 0x36, bit 4) defaults high (active), meaning that the system-side device is fully operational except for the ISOcap, and the line-side device has no communication or power. PME-related logic is not cleared by reset.

D0 Active State

D0 active is the fully-active condition arrived at from D0 Uninitialized after software configuration. 3.3 V is available from the PCI power bus to power all PCI I/O pads and non-Vaux PCI core logic. 3.3 V Vaux is available for all Vaux-power I/O and logic.

D3 Hot State

D3 (hot) is the powered-up idle condition. 3.3 V is available from the PCI power bus to power all PCI I/O pads and non-Vaux PCI core logic; however, PCICLK can be stopped for minimal power consumption. PCI BUS signals are guaranteed to be held low during D3 (hot). 3.3 V Vaux is available for all Vaux-power I/O and logic at a max current draw of 20 mA per card if wake-on-ring is not enabled or 375 mA per card if wake-on-ring is enabled.

D3 Cold State

D3 (cold) is the powered-down idle condition. The 3.3 V PCI power bus is removed so there is no power to all PCI I/O pads and non-Vaux PCI core logic. PCI BUS signals are guaranteed to be held low during D3 (cold). Vaux is available for all Vaux-power I/O and logic at a max current draw of 20 mA per card if wake-on-ring is not enabled, or 375 mA per card if wake-on-ring is enabled.

B0 State

B0 is the fully-active bus power condition. 3.3 V is available from the PCI power bus to power to all PCI I/O pads and non-Vaux PCI core logic. 3.3 V Vaux is available for all Vaux-power I/O and logic. The PCICLK is active, and all bus transactions are available.

B3 State

B3 is the powerdown condition. The 3.3 V PCI power bus is removed so there is no power to any PCI I/O pads and non-Vaux PCI core logic. No PCI bus activity is allowed. All PCI BUS signals are guaranteed to be held static, with the exception of $\overline{\text{PME}}$. Vaux is available for all PME-related logic and I/O. Exit from B3 requires application of supply and is always accompanied by an active $\overline{\text{RESET}}$. Software must guarantee that the DAA PCI Function enters D3 before placing the PCI Bus in B3.

EPROM Interface

During Si3052 initialization, the EE_SD and EE_SC pins are examined to determine if an external EPROM is present. A pullup resistor on EE_SC and a logic high on EE_SD indicate this condition. The EPROM load sequence reads six data bytes immediately after a cold reset. The first data byte is a header of 95h. the next four data bytes are the PCI subsystem Vendor ID (SVID) and the subsystem ID (SSID) values. The final data byte is a cyclic redundancy check (CRC) code. The EPROM map is shown in Figure 20.

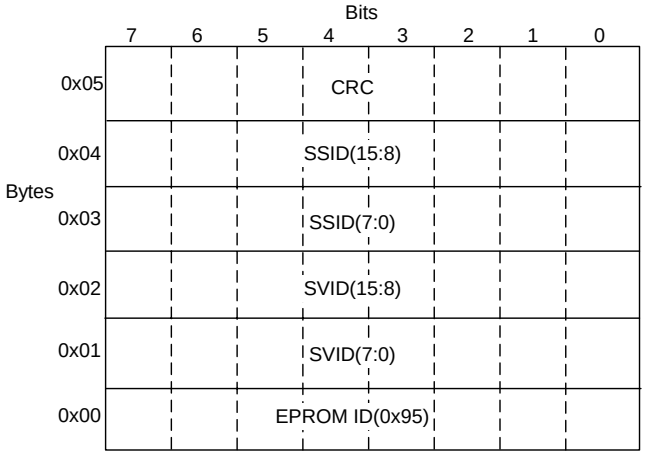


Figure 20. EPROM Map

The 8-bit CRC code indicates error detection in a faulty EPROM. The CRC is calculated using the following generator polynomial:

$$G(X) = X^8 + X^2 + X^1 + 1$$

The CRC byte is calculated by appending an all-zero byte to the end of the data bytes and dividing the string by the generator polynomial in modulo-2 fashion. The remainder of the division is the CRC byte value.

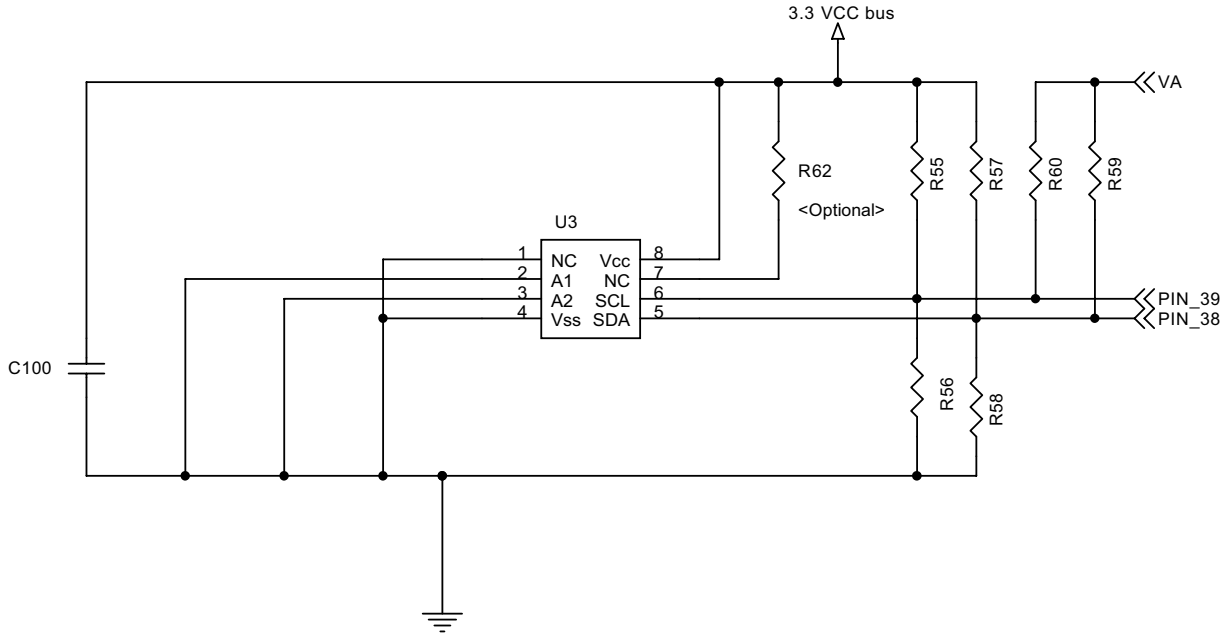
An example calculation follows.

Data Bytes:

0x95	Header byte
0x43	SVID[7:0]
0x15	SVID[15:8]
0x52	SSID[7:0]
0x30	SSID[15:8]
0x00	All zero byte

EPROM Bytes:

0x95	Header byte
0x43	SVID[7:0]
0x15	SVID[15:8]
0x52	SSID[7:0]
0x30	SSID[15:8]
0x3D	CRC byte



Option	PIN_38	PIN_39	PIN_38 Function	PIN_39 Function
0	X	0	$\overline{\text{CLKRUN}}$	AOUT
1	X	A	$\overline{\text{CLKRUN}}$	PNPID
2	X	1	$\overline{\text{CLKRUN}}$	AOUT
3	A	0	PNPID	AOUT
4	A	A	PNPID	PNPID
5	A	1	PNPID	AOUT
6	1	0	SDA	SCL/AOUT
7	1	A	---	PNPID
8	1	1	SDA	SCL/AOUT

Note: X = No Install
1 = 4.7 kW pullup to 3.3 V
0 = 4.7 kW pulldown to GND
A = Voltage divider between V_A and GND

Figure 21. EPROM Circuit

Interrupt Sources

$\overline{\text{INTA}}$ is a level triggered interrupt pin for Si3052 interrupt sources. The sources for the $\overline{\text{INTA}}$ interrupt are as follows:

- Ring Detect
- PCI Target Abort
- PCI Master Abort
- DMA Read End of Buffer
- DMA Read Interrupt Address
- DMA Write End of Buffer
- DMA Write Interrupt Address
- Interrupt Counter
- ISOcap Frame Detect
- Receive Overload
- Billing tone Detect
- Drop Out Detect
- Overload Detect

$\overline{\text{PME}}$ is a level triggered interrupt pin for PCI Power Management events. The source for the $\overline{\text{PME}}$ interrupt is ring detect with or without ring validation.

FIFO Buffers

The FIFO buffers are fixed as 16 bits wide by 8 samples deep for DMA master read and write. The sample data is contained in the lowest 16 bits of a 32-bit word. The FIFO buffers do not support DMA target operations. The FIFO buffers are not memory mapped and cannot be accessed directly.

Telephone Line Interface Functional Description

Together, the Si3052 and Si3017/11/18 comprise an integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line interface requirements. The device implements Silicon Laboratories' proprietary ISOcap™ technology, which offers the highest level of integration by replacing an analog front end (AFE), an isolation transformer, relays, opto-isolators, a 2- to 4-wire hybrid, and other circuitry.

The Si3018 can be fully programmed to meet international requirements and is compliant with FCC, TBR21, JATE, and other country-specific PTT specifications as shown in Table 14. Also, the Si3018 meets the most stringent global requirements for out-of-band energy, emissions, immunity, lightning surges, and safety. The Si3011 meets all TBR21 and FCC requirements. The Si3017 meets all FCC requirements.

Table 14. Country Specific Register Settings

	Offset 0x40					Line-Side		
Country	**OHS**	**ACT2,ACT**	**DCT[1:0]**	**RZ**	**RT**	**3018**	**3011**	**3017**
Argentina	0	00	10	0	0	✓	✓	✓
Australia	1	10	01	0	0	✓		
Austria[1]	0	10	11	0	0	✓	✓	
Bahrain	0	10	11	0	0	✓	✓	
Belgium[1]	0	10	11	0	0	✓	✓	
Brazil	0	00	01	0	0	✓		
Bulgaria	0	10	11	0	0	✓	✓	
Canada	0	00	10	0	0	✓	✓	✓
Chile	0	00	10	0	0	✓	✓	✓
China	0	00	10	0	0	✓	✓	✓
Colombia	0	00	10	0	0	✓	✓	✓
Croatia	0	10	11	0	0	✓	✓	
Cyprus	0	10	11	0	0	✓	✓	
Czech Republic	0	10	11	0	0	✓	✓	
Denmark[1]	0	10	11	0	0	✓	✓	
Ecuador	0	00	10	0	0	✓	✓	✓
Egypt	0	00	01	0	0	✓		
El Salvador	0	00	10	0	0	✓	✓	✓
Finland[1]	0	10	11	0	0	✓	✓	
France[1]	0	10	11	0	0	✓	✓	
Germany[1]	0	10	11	0	0	✓	✓	
Greece[1]	0	10	11	0	0	✓	✓	
Guam	0	00	10	0	0	✓	✓	✓
Hong Kong	0	00	10	0	0	✓	✓	✓
Hungary	0	00	10	0	0	✓	✓	✓
Iceland[1]	0	10	11	0	0	✓	✓	

Notes:

1. TBR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
2. Supported for loop currents ≥ 20 mA.
3. Products using the Si3011/17 which have been submitted for JATE approval should document a waiver for the JATE dc termination specification. This specification is met in the Si3018 global line-side device.

Table 14. Country Specific Register Settings (Continued)

	Offset 0x40					Line-Side		
Country	**OHS**	**ACT2,ACT**	**DCT[1:0]**	**RZ**	**RT**	**3018**	**3011**	**3017**
India	0	00	10	0	0	✓	✓	✓
Indonesia	0	00	10	0	0	✓	✓	✓
Ireland[1]	0	10	11	0	0	✓	✓	
Israel	0	10	11	0	0	✓	✓	
Italy[1]	0	10	11	0	0	✓	✓	
Japan	0	00	01	0	0	✓	✓[3]	✓[3]
Jordan	0	00	01	0	0	✓		
Kazakhstan	0	00	01	0	0	✓		
Kuwait	0	00	10	0	0	✓	✓	✓
Latvia	0	10	11	0	0	✓	✓	
Lebanon	0	10	11	0	0	✓	✓	
Luxembourg[1]	0	10	11	0	0	✓	✓	
Macao	0	00	10	0	0	✓	✓	✓
Malaysia[2]	0	00	01	0	0	✓		
Malta	0	10	11	0	0	✓	✓	
Mexico	0	00	10	0	0	✓	✓	✓
Morocco	0	10	11	0	0	✓	✓	
Netherlands[1]	0	10	11	0	0	✓	✓	
New Zealand	0	11	10	0	0	✓		
Nigeria	0	10	11	0	0	✓	✓	
Norway[1]	0	10	11	0	0	✓	✓	
Oman	0	00	01	0	0	✓		
Pakistan	0	00	01	0	0	✓		
Peru	0	00	10	0	0	✓	✓	✓
Philippines	0	00	01	0	0	✓		
Poland	0	00	10	1	1	✓		
Portugal[1]	0	10	11	0	0	✓	✓	
Romania	0	00	10	0	0	✓	✓	✓
Russia	0	00	01	0	0	✓		
Saudi Arabia	0	00	10	0	0	✓	✓	✓
Singapore	0	00	10	0	0	✓	✓	✓
Slovakia	0	00	10	0	0	✓	✓	✓
Slovenia	0	10	11	0	0	✓	✓	
South Africa	1	00	10	1	0	✓		
South Korea	0	00	10	1	0	✓		

Notes:

1. TBR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
2. Supported for loop currents ≥ 20 mA.
3. Products using the Si3011/17 which have been submitted for JATE approval should document a waiver for the JATE dc termination specification. This specification is met in the Si3018 global line-side device.

Table 14. Country Specific Register Settings (Continued)

	Offset 0x40					Line-Side		
Country	**OHS**	**ACT2,ACT**	**DCT[1:0]**	**RZ**	**RT**	**3018**	**3011**	**3017**
Spain[1]	0	10	11	0	0	✓	✓	
Sweden[1]	0	10	11	0	0	✓	✓	
Switzerland[1]	0	10	11	0	0	✓	✓	
Syria	0	00	01	0	0	✓		
Taiwan	0	00	10	0	0	✓	✓	✓
Thailand	0	00	01	0	0	✓		
UAE	0	00	10	0	0	✓	✓	✓
United Kingdom[1]	0	10	11	0	0	✓	✓	
USA	0	00	10	0	0	✓	✓	✓
Yemen	0	00	10	0	0	✓	✓	✓

Notes:

1. TBR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
2. Supported for loop currents ≥ 20 mA.
3. Products using the Si3011/17 which have been submitted for JATE approval should document a waiver for the JATE dc termination specification. This specification is met in the Si3018 global line-side device.

Initialization

When the Si3052 is initially powered up, the $\overline{\text{RESET}}$ pin must be asserted. When the $\overline{\text{RESET}}$ pin is de-asserted, the registers have their default values. The DAA registers cannot be accessed during the crystal warm-up period. The following is an example initialization procedure:

1. Select the crystal frequency using the XTAL bit (Offset 0x28, bit 24).
2. Poll the DAA status bit (Offset 0x4, bit 23) until it indicates the DAA is ready.
3. Select the desired sample rate using the SRC bits (Offset 0x37, bits 3:0).
4. Power up the line side by clearing the PDL bit (Offset 0x36, bit 4).
5. Enable AOUT by setting ARM[1:0] (Offset 0x36, bits 5:0) and ATM[1:0] (Offset 36, bits 6:1) to the desired level.
6. Set the required line interface parameters (i.e., DCT[1:0], ACT, OHS, and RT) as defined in Table 14.
7. Prior to receiving or transmitting data, ensure FDT (Offset 3C, bit 6) is set indicating the Si3018 is ready for normal operation.

After the procedure is complete, the DAA is ready for off-hook, on-hook line monitoring, and ring detection.

Isolation Barrier

The Si3052 achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Silicon Laboratories' proprietary ISOcap™ signal processing techniques. These techniques eliminate signal degradation from capacitor mismatches, common mode interference, or noise coupling. The C1, C2, C8, and C9 capacitors isolate the Si3052 system-side device from the Si3017/11/18 line-side device. All transmit, receive, control, ring detect, and caller ID data are communicated through this barrier. Y2 class capacitors can be used to achieve surge performance of 5 kV or greater.

The ISOcap communications link is disabled by default. To enable it, the PDL bit (Offset 0x36, bit 4) must be cleared. No communication between the Si3052 and Si3017/11/18 can occur until this bit is cleared and the FDT bit (Offset 0x3C, bit 6) is high.

Parallel Handset Detection

The Si3052 can detect a parallel handset going off-hook. When the Si3052 is off-hook, the loop current can be monitored via the LCS bits (Offset 0x3C, bits 4:0). A significant drop in loop current can signal a parallel handset going off-hook. If a parallel handset causes the LCS bits to read 0s, the DropOut Detect Interrupt bit (Offset 0x34, bit 3) can be checked to verify that a valid line still exists.

For the Si3052 to operate in parallel with another handset, the parallel handset must have a sufficiently high dc termination to support two DAAs off-hook on the same line. Improved parallel handset operation can be achieved by changing the dc impedance from 50 to 800 Ω by setting the DCR bit (Offset 0x4A, bit 0) and setting DCV[1:0] (Offset 0x4A, bits 7:6) to 00b. MAP = 1 is necessary to access the DCR and DCV bits.

Loop Current Sensing

The Si3052 measures loop current. The LCS[4:0] bits (Offset 0x3C, bits 4:0) report loop current measurements when off-hook. The following can be determined with the LCS bits:

- When off-hook, detect if a parallel phone goes on- or off-hook.
- Determine if sufficient loop current is available to operate.
- Detect if there is an overload condition (see "Overload Detection" on page 37).

Loop Current Measurement

When the Si3052 is off-hook, the LCS bits measure loop current in 3.3 mA/bit resolution. These bits detect another phone going off-hook by monitoring the dc loop current. The line current sense transfer function is shown in Figure 22 and is detailed in Table 15. The LCS bits display loop current down to the minimum operation loop current for the DAA, which is set by the MINI[1:0] bits.

When the LCS bits have reached their maximum value, the Loop Current Sense Overload Interrupt bit fires; however, LCSI firing does not necessarily guarantee that an overload situation has occurred. An overload situation in the DAA is determined by the status of the OPD bit. After the LCSI interrupt fires, the OPD bit should be checked to determine if an overload situation exists. The OPD bit indicates an overload situation when loop current exceeds either 160 mA (ILIM = 0) or 60 mA (ILIM = 1).

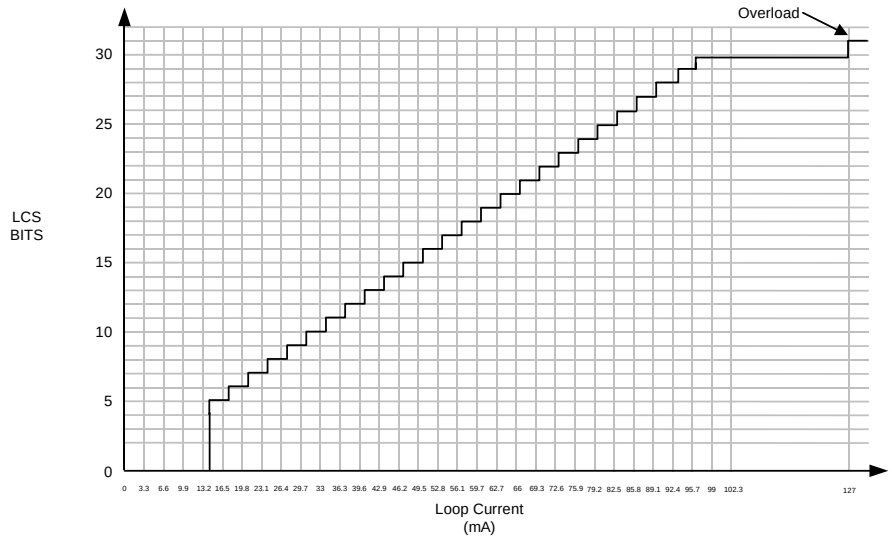


Figure 22. Typical LCS Transfer Function (ILIM = 0)

Table 15. Loop Current Transfer Function

LCS[4:0]	Condition
00000	Insufficient line current for normal operation. Use the DODI bit (Offset 0x34, bit 3) to determine if a line is still connected.
00100	Minimum line current for normal operation. (MINI[1:0] = 01)
11111	Loop current may be excessive. For FCC, low voltage, and JATE termination, current may be >120 mA. For TBR21, current may be >60 mA. Use the OPD bit (Offset 0x43, bit 1) to determine if an overload condition exists.

Off-Hook

The software generates an off-hook command by setting the OH bit (Offset 0x35, bit 0). This state seizes the line for incoming/outgoing calls and can also be used for pulse dialing. When on-hook, negligible dc current flows through the hookswitch. When off-hook, the hookswitch transistor pair, Q1 and Q2, turn on. A termination impedance is applied across TIP and RING and causes dc loop current to flow. The termination impedance has an ac and dc component.

Several events occur internally to the DAA when the OH bit is set. There is a 250 µs latency for the off-hook command to communicate to the line-side device. When the line-side device goes off-hook, an off-hook counter forces a delay before transmission or reception can occur. This off-hook counter time is controlled by the FOH[1:0] bits (Offset 0x4F, bits 6:5). The default setting for the off-hook counter time is 128 ms, but can be adjusted up to 512 ms or down to either 64 or 8 ms. After the off-hook counter expires, a resistor calibration is performed for 17 ms. The resistor calibration can be disabled by setting the RCALD bit (Offset 0x49, bit 5). After the resistor calibration is performed, an ADC calibration is performed for 256 ms. The ADC calibration can be disabled by setting the CALD bit (Offset 0x41, bit 5). Refer to "Calibration" on page 37 for information on automatic and manual calibration. Disabling the resistor and the ADC calibrations should only be done when a fast response is needed after going off-hook, such as when responding to a Type II caller-ID signal. See "Caller ID" on page 36. To calculate the total time required to go off-hook and start transmission or reception, the digital filter delay (typically 1.5 ms with the FIR filter) should be included in the calculation.

DC Termination

The Si3052 has four programmable dc termination modes that are selected with the DCT[1:0] bits (Offset 0x40, bits 3:2).

FCC mode (DCT[1:0] = 10_b), shown in Figure 23, is the default dc termination mode and supports a transmit full scale level of –0.5 dBm at TIP and RING. This mode meets FCC requirements and the requirements of many other countries.

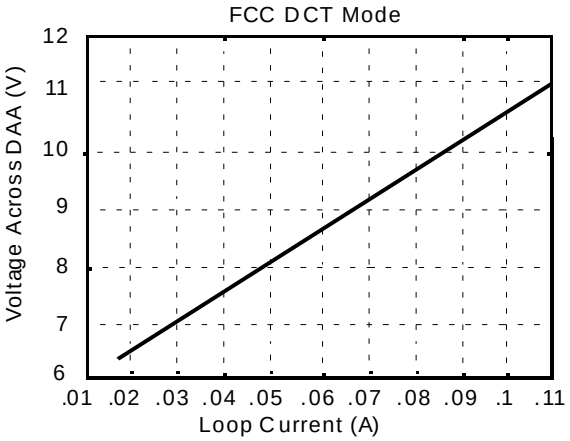


Figure 23. FCC Mode I/V Characteristics

TBR21 mode (DCT[1:0] = 11_b), shown in Figure 24, provides current limiting while maintaining a transmit full-scale level of –0.5 dBm at TIP and RING. The dc termination current limits before reaching 60 mA.

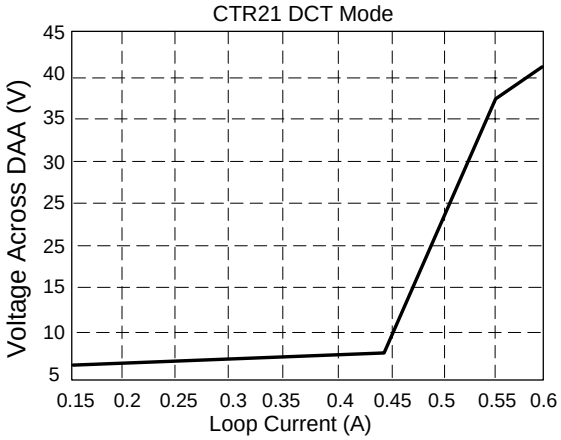


Figure 24. TBR21 Mode I/V Characteristics

Japan mode (DCT[1:0] = 01_b), shown in Figure 25, is a lower voltage mode and supports a transmit full-scale level of –0.5 dBm. The low voltage requirement is dictated by countries, such as Japan and Malaysia.

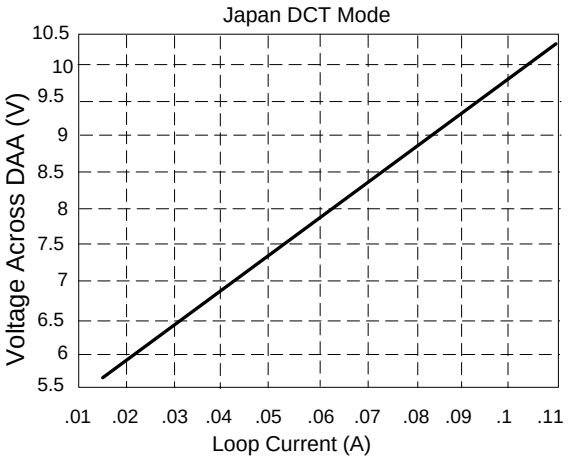


Figure 25. Japan Mode I/V Characteristics

Low-voltage mode (DCT[1:0] = 00_b), shown in Figure 26, is the lowest line voltage mode supported on the Si3052, with a transmit full-scale level of –0.5 dBm. This low-voltage mode is offered for situations that require low line voltage operation.

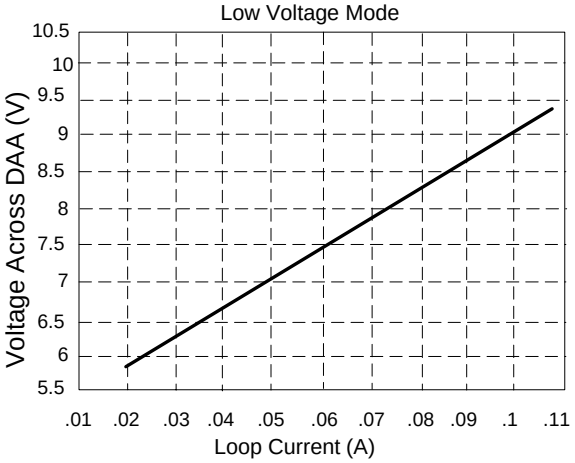


Figure 26. Low-Voltage Mode I/V Characteristics

AC Termination

The Si3052 has four ac termination impedance settings. The ACT and ACT2 bits select the ac impedance. The available ac termination settings are listed in Table 16.

Table 16. AC Termination Settings

ACT2	ACT	AC Termination
0	0	Real, nominal 600 Ω termination that satisfies the impedance requirements of FCC part 68, JATE, and other countries.
0	1	Complex impedance that satisfies global complex impedance requirements.
1	0	Complex impedance that satisfies global complex impedance requirements EXCEPT New Zealand. Achieves higher return loss for some complex ac termination.
1	1	Complex impedance for use in New Zealand.

Transhybrid Balance

The Si3052 contains an on-chip analog hybrid that performs the 2- to 4-wire conversion and near-end echo cancellation. This hybrid circuit is adjusted for each ac termination setting selected. The Si3052 also offers a digital hybrid for additional near-end echo cancellation. For each ac termination setting selected, the eight programmable hybrid registers (Offsets 0x5D–0x64) can be programmed with coefficients to increase cancellation of real-world line characteristics. The digital filter can produce 10 dB or greater of near-end echo cancellation in addition to the echo cancellation provided by the analog hybrid circuitry.

Ring Detection

The ring signal is connected from TIP and RING to the RNG1 and RNG2 pins. The Si3052 supports either full- or half-wave ring detection. Full-wave ring detection detects a polarity reversal and the ring signal. See “Caller ID” on page 36. The ring detection threshold is programmable with the RT bit (Offset 0x40, bit 0).

The ring detector output can be monitored with the register bits RDTP, RDTN, and RDT (Offset 0x35, bits 6, 5, and 2). Software must detect the frequency of the ring signal to distinguish a ring from pulse dialing by telephone equipment connected in parallel. Alternatively, hardware ring validation can be used. See "Ring Validation" on page 34.

The ring detector mode is controlled by the RFWE bit (Offset 0x42, bit 1). When the RFWE bit is 0 (default mode), the ring detector operates in half-wave rectifier mode. Only positive ring signals are detected. A positive ring signal is defined as a voltage greater than the ring threshold across RNG1-RNG2. Conversely, a negative

ring signal is defined as a voltage less than the negative ring threshold across RNG1-RNG2.

When the RFWE bit is 1, the ring detector operates in full-wave rectifier mode. Positive and negative ring signals are detected.

The RDTP and RDTN behavior is based on the RNG1-RNG2 voltage. When the signal on RNG1-RNG2 is above the positive ring threshold, the RDTP bit is set. When the signal on RNG1-RNG2 is below the negative ring threshold, the RDTN bit is set. When the signal on RNG1-RNG2 is between these thresholds, neither bit is set.

The RDT behavior is also based on the RNG1-RNG2 voltage. When the RFWE bit is 0, a positive ring signal sets the RDT bit for a period of time. When the RFWE bit is 1, either a positive or negative ring signal sets the RDT bit.

The RDT bit acts like a one shot. When a new ring signal is detected, the one shot is reset. If no new ring signals are detected before the one shot counter reaches 0, the RDT bit returns to 0. The length of this count (in seconds) is 65536 divided by the sample rate. The RDT bit is also reset to 0 by an off-hook event.

Ring Validation

This feature prevents false triggering of a ring detection by validating the ring parameters. Invalid signals, such as line-voltage changes when a parallel handset goes off-hook, pulse dialing, and high-voltage line tests, are ignored. Ring validation can be enabled during normal operation and in low-power sleep mode.

The ring validation circuit operates by calculating the time between alternating crossings of positive and negative ring thresholds to validate that the ring frequency is within tolerance. High- and low-frequency tolerances are programmable in the RAS[5:0] and RMX[5:0] fields. The RCC[2:0] bits define the length of time the ring signal must be within tolerance.

Once the duration of the ring frequency is validated by the RCC bits, the circuitry stops checking for frequency tolerance and begins checking for the end of the ring signal, which is defined by a lack of additional threshold crossings for a period of time configured by the RTO[3:0] bits. When the ring frequency is first validated, a timer defined by the RDLY[2:0] bits is started. If the RDLY[2:0] timer expires before the ring timeout, the ring is validated, and a valid ring is indicated. If the ring timeout expires before the RDLY[2:0] timer, a valid ring is not indicated.

Ring validation requires five parameters:

- Timeout parameter to place a lower limit on the frequency of the ring signal on the RAS[5:0] bits (Offset 0x48, bits 5:0). The frequency is measured by calculating the time between crossings of positive and negative ring thresholds.
- Minimum count to place an upper limit on the frequency on the RMX[5:0] bits (Offset 0x46, bits 5:0).
- Time interval over which the ring signal must be the correct frequency on the RCC[2:0] bits (Offset 0x47, bits 2:0).
- Timeout period that defines when the ring pulse has ended with the most recent ring threshold crossing on the RTO [3:0] bits (Offset 0x47, bits 6:3).
- Delay period between when the ring signal is validated and when a valid ring signal is indicated to help accommodate distinctive ring on the RDLY [2:0] bits (Offset 0x47, bit 7; Offset 0x46, bits 7:6)

The ring validation enable bit, RNGV (Offset 0x48,bit 7), enables or disables the ring validation feature in normal operating mode and low-power sleep mode.

Ringer Impedance and Threshold

The ring detector in many DAAs is ac coupled to the line with a large 1 μF, 250 V decoupling capacitor. The ring detector on the Si3052 is resistively coupled to the line. The network produces a high ringer impedance to the line of approximately 20 MΩ to meet the majority of country PTT specifications including FCC and TBR21.

Several countries including Poland, South Africa, and Slovenia require a maximum ringer impedance that can be met with an internally-synthesized impedance by setting the RZ bit (Offset 0x40, bit 1).

Countries also specify ringer thresholds differently. The RT bit (Offset 0x40, bit 0) selects between two different ringer thresholds: 15 V ±10% and 21.5 V ±10%. These two settings satisfy ringer threshold requirements worldwide. The thresholds are set so that a ring signal is guaranteed to not be detected below the minimum, and a ring signal is guaranteed to be detected above the maximum.

DTMF Dialing

The Si3018 meets all the country requirements for DTMF dialing listed in Table 14 on page 28. If desired, higher DTMF levels can be achieved by setting the DIAL bit (Offset 0x42, bit 6) at low loop currents (<15 mA). Higher DTMF levels can also be achieved if the amplitude is increased and the peaks of the DTMF signal are clipped at digital full scale, avoiding wrapping the waveform.

Clipping the signal produces distortion and intermodulation of the signal. Generally, increased distortion between 10–20% is acceptable during DTMF signaling. Several dB higher DTMF levels can be achieved with this technique, compared with a digital full-scale peak signal.

Pulse Dialing and Spark Quenching

Going off- and on-hook to generate make and break pulses accomplishes pulse dialing. The nominal rate is 10 pulses per second. Some countries have tight specifications for pulse fidelity including make and break times, make resistance, and rise and fall times. In a traditional solid-state dc holding circuit, there are considerations for meeting these requirements.

The Si3052 dc holding circuit has active control of the on-hook and off-hook transients to maintain pulse dialing fidelity.

Spark quenching requirements in countries, such as Italy, the Netherlands, South Africa, and Australia, address the on-hook transition during pulse dialing. These tests provide an inductive dc feed resulting in a large voltage spike. A spike is caused by the line inductance and the sudden decrease in current through the loop when going on-hook. The traditional way of addressing this problem is to put a parallel RC shunt across the hookswitch relay. The capacitor is large (~1 μF, 250 V) and relatively expensive. In the Si3052, the OHS bit (Offset 0x40, bit 6), OHS2 bit (Offset 0x4F, bit 3), and SQ[1:0] bits (Offset 0x6B, bits 6,4) can ramp down the loop current to pass these tests without requiring additional components. A slow ramp-down of the loop current introduces a delay between the time the OH bit is cleared and the time the DAA actually goes on-hook.

To ensure proper operation of the DAA during pulse dialing, disable the automatic resistor calibration that is performed each time the DAA enters the off-hook state by setting the RCALD bit.

Billing Tone Detection and Receive Overload

“Billing tones” or “metering pulses” generated by the central office can produce modem connection difficulties. The billing tone is a 12 or 16 kHz signal and is occasionally used in Germany, Switzerland, and South Africa. Depending on line conditions, the billing tone might be large enough to cause major errors related to the modem data. The Si3052 chipset can provide feedback indicating the beginning and end of a billing tone.

Billing tone detection is enabled by setting the BTE bit (Offset 0x41, bit 2). Billing tones less than 1.1 V_{PK} on the line are filtered out by the low-pass digital filter on the Si3052. The ROV bit (Offset 0x41, bit 1) is set when a line signal is greater than 1.1 V_{PK}, indicating a receive overload condition. The BTD bit (Offset 0x41, bit 0) is set when a line signal (billing tone) is large enough to excessively reduce the line-derived power supply of the Si3018 line-side device. When the BTD bit is set, the dc termination is changed to an 800 Ω dc impedance to ensure minimum line voltage levels even in the presence of billing tones.

The OVL bit (Offset 0x43, bit 2) can be pulled following a billing tone detection. When the OVL bit returns to 0, indicating that the billing tone has passed, the ROV bit remains sticky and must be written to 0 to be reset. After the billing tone passes, the DAA initiates an auto-calibration sequence that must complete before data can be transmitted.

Certain line events, such as an off-hook event on a parallel phone or a polarity reversal, can trigger the ROV or the BTD bits, after which the ROV bit must be reset. Look for multiple events before qualifying if billing tones are actually present.

Although the DAA remains off-hook during a billing tone event, the received data from the line is corrupted when a large billing tone occurs. To receive data through a billing tone, an external LC filter must be added. A modem manufacturer can provide this filter in the form of a dongle that connects on the phone line before the DAA. The manufacturer does not have to include a costly LC filter internal to the modem when it is only necessary to support a few countries.

Alternatively, when a billing tone is detected, the system software can notify the user that a billing tone has occurred. The user can contact the telephone company to disable the billing tones or to purchase an external LC filter.

Billing Tone Filter (Optional)

To operate without degradation during billing tones in Germany, Switzerland, and South Africa, an external LC notch filter is required. The Si3052 can remain off-hook during a billing tone event, but modem data is lost in the presence of large billing tone signals. The notch filter design requires two notches, one at 12 kHz and one at 16 kHz. Because these components are fairly expensive and few countries supply billing tone support, this filter is placed in an external dongle or added as a population option for these countries. Figure 27 shows an example billing tone filter.

L1 must carry the entire loop current. The series resistance of the inductors is important to achieve a narrow and deep notch. This design has more than 25 dB of attenuation at 12 and 16 kHz.

Table 17. Component Values—Optional Billing Tone Filters

Symbol	Value
C1,C2	0.027 μF, 50 V, ±10%
C3	0.01 μF, 250 V, ±10%
L1	3.3 mH, >120 mA, <10 Ω, ±10%
L2	10 mH, >40 mA, <10 Ω, ±10%

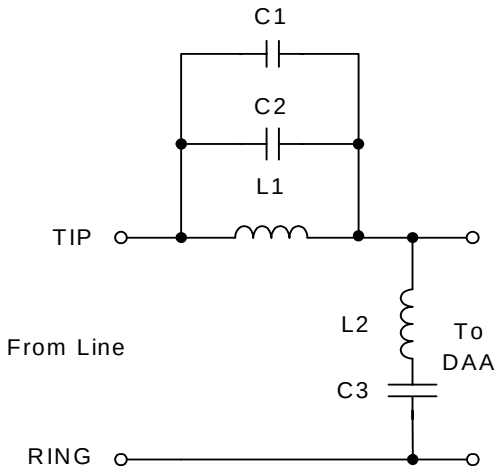


Figure 27. Billing Tone Filter

The billing tone filter affects the DAA's ac termination and return loss. The current complex ac termination passes worldwide return loss specifications with and without the billing tone filter by at least 3 dB. The ac termination is optimized for frequency response and hybrid cancellation while having greater than 4 dB of margin with or without the dongles for South Africa, Australia, TBR21, Germany, and Switzerland country-specific specifications.

On-Hook Line Monitor

The Si3052 receives line activity when in an on-hook state through the RNG1/2 pins. This mode detects caller ID data and no line current is drawn. See “Caller ID” on page 36. This mode is enabled by setting the ONHM bit (Offset 0x35, bit 3). ARX [2:0] (Offset 0x3F, bits 2:0) provides gain to the normal receive path of the DAA and functions as a gain bit for the on-hook line monitor.

Caller ID

The Si3052 can pass caller ID data from the phone line to a software caller ID decoder.

Type I Caller ID

Type I Caller ID sends the CID data while the phone is on-hook. In systems where the caller ID data is passed on the phone line between the first and second rings, utilize the following method to capture the caller ID data:

1. After identifying a ring signal using one of the methods described in "Ring Detection" on page 33, determine when the first ring has completed.
2. Assert the ONHM bit (Offset 0x35, bit 3) to enable current caller ID.
3. The low-current ADC, which is powered from the system-side device, digitizes the caller ID data passed across the RNG 1/2 pins.
4. Clear the ONHM bit after the caller ID data is received.

In systems where the caller ID data is preceded by a line polarity (battery) reversal, use the following method to capture the caller ID data:

1. Enable full-wave rectified ring detection (Offset 0x42, bit 1).
2. Monitor the RDTP and RDTN register bits to identify whether a polarity reversal or ring signal has occurred. A polarity reversal trips either the RDTP or RDTN ring detection bits, and, thus, the full-wave ring detector must be used to distinguish a polarity reversal from a ring. The lowest specified ring frequency is 15 Hz; therefore, if a battery reversal occurs, the DSP software should wait a minimum of 40 ms to verify that the event observed is a battery reversal and not a ring signal. This time is greater than half the period of the longest ring signal. If another edge is detected during this 40 ms pause, this event is characterized as a ring signal and not a battery reversal.
3. Assert the ONHM bit (Offset 0x35, bit 3) to enable the low-current caller ID ADC. The low-current ADC, which is powered from the system-side device, digitizes the caller ID data passed across the RNG 1/2 pins.
4. Clear the ONHM bit after the caller ID data is received.

Type II Caller ID

Type II Caller ID sends the CID data while the phone is off-hook and is often referred to as caller ID/call waiting (CID/CW). To receive the CID data while off-hook, use the following procedure:

1. The Caller Alert Signal (CAS) tone is sent from the Central Office (CO) and is digitized along with the line data. The software must detect the presence of this tone.
2. Since the Si3052 is the only device on the line and is Type II CID-compliant, the software must mute its upstream data output to avoid propagation of its reply tone and the subsequent CID data. After muting its upstream data output, the software must then return an acknowledgement (ACK) tone to the CO to request the

transmission of the CID data.

3. The CO then responds with the CID data, and the software unmutes the upstream data output and continues with normal operation.
4. The muting of the upstream data path by the software mutes the handset in a telephone application so the user cannot hear the acknowledgement tone and CID data being sent.

The CID data presented to the software could have up to a 10% dc offset. The software caller ID decoder must either use a high-pass or a band-pass filter to accurately retrieve the caller ID data.

Overload Detection

The Si3052 can be programmed to detect an overload condition that exceeds the normal operating power range of the DAA circuit. To use the overload detection feature, the following steps should be performed:

1. Set the OH bit (Offset 0x35, bit 0) to go off-hook, and wait 25 ms to allow line transients to settle.
2. Enable overload detection by setting the OPE bit (Offset 0x41, bit 3).

If the DAA senses an overload situation, it automatically presents an 800 Ω impedance to the line to reduce the hookswitch current. At this time, the DAA also sets the OPD bit (Offset 0x43, bit 0) to indicate that an overload condition exists. The line current detector within the DAA has a threshold that is dependant upon the ILIM bit (Offset 0x4A, bit 1). When ILIM = 0, the overload detection threshold equals 160 mA. When ILIM = 1, the overload detection threshold equals 60 mA. The OPE bit should always be cleared before going off-hook.

Gain Control

The Si3052 supports multiple receive gain and transmit attenuation settings (Offset 0x3F). The receive path supports gains of 0, 3, 6, 9, and 12 dB, as selected with the ARX[2:0] bits. The receive path can be muted with the RXM bit. The transmit path supports attenuations of 0, 3, 6, 9, and 12 dB, as selected with the ATX[2:0] bits. The transmit path can be muted with the TXM bit.

Sample Rate Converter

The SCR [3:0] bits (Offset 0x37, bits 3:0) are used to select the sample rate. The following sample rates are supported: 7200, 8000, 8229, 8400, 9000, 9600, 10286, 12000, 13714, and 16000 Hz.

Filter Selection

The Si3052 supports two filter selections for the receive and transmit signals as defined in Table 10 and Table 11 on page 13. The IIRE (Offset 0x40, bit 4) selects between the IIR and FIR filters. The IIR filter provides a lower, but non-linear, group delay than the default FIR filter.

Power Management

The Si3052 supports four basic power management operation modes: normal operation, reset operation, sleep mode, and full powerdown mode. The power management modes are controlled by the PDL and PDN bits (Offset 0x36, bits 4,3).

On powerup or following a reset, the Si3052 is in reset operation. The PDL bit is set, and the PDN bit is cleared. The Si3052 is fully-operational except for the ISOcap™ link. No communication between the Si3052 and Si3017/11/18 can occur during reset operation. Bits associated with the Si3017/11/18 are not valid in this mode.

The most common mode of operation is normal operation. The PDL and PDN bits are cleared. The Si3052 is fully-operational, and the ISOcap link is passing information between the Si3052 and the Si3017/11/18. A valid sample rate must be programmed before entering this mode.

The Si3052 supports a low-power sleep mode for the wake-up-on-ring feature of many modems. The sample rate must be programmed with a valid non-zero value before enabling sleep mode. The PDN bit must then be set and the PDL bit cleared. The Si3052 is non-functional except for the ISOcap link signal. To take the Si3052 out of sleep mode, pulse ($\overline{\text{RESET}}$) low.

In summary, the powerdown/up sequence for sleep mode is as follows:

1. SRC[3:0] must have a valid non-zero value.
2. Set the PDN bit (Offset 0x36, bit 3) and clear the PDL bit (Offset 0x36, bit 4).
3. Reset the Si3052 by pulsing the $\overline{\text{RESET}}$ pin.
4. Program registers to required settings.

The Si3052 also supports an additional powerdown mode. When the PDN and PDL bits are set, the chipset enters a complete powerdown mode and draws negligible current (deep sleep mode). Normal operation is restored using the same process for taking the Si3052 out of sleep mode.

Calibration

The Si3017/11/18 initiates an auto-calibration by default when the device goes off-hook or experiences a loss in line power. Calibration removes offsets that are present in the on-chip ADC and which could affect the ADC dynamic range. Auto-calibration is initiated after the DAA dc termination stabilizes and takes 256 ms to complete. Because of the large variation in line conditions and line card behavior that is presented to

the DAA, it might be beneficial to use manual calibration instead of auto-calibration.

Execute manual calibration as close to 256 ms as possible before valid transmit/receive data is expected.

The following steps implement manual calibration:

1. The CALD (Offset 0x41, bit 5) bit must be set to 1.
2. The MCAL bit (Offset 0x41, bit 6) must be toggled to one and then 0 to begin and complete the calibration.
3. The calibration is completed in 256 ms.

In-Circuit Testing

Four loopback modes exist allowing increased coverage of system components. For three of the test modes, an off-hook sequence must be performed.

For the start-up test mode, no line-side power is necessary, and no off-hook sequence is required. The start-up test mode is enabled by default. When the PDL bit (Offset 0x36, bit 4) is set (the default case), the line-side is in a powerdown mode, and the PCI side is in a digital loop-back mode. Data received is passed through the internal filters and transmitted. This path introduces approximately 0.9 dB of attenuation. There is a group delay of transmit and receive filters. Clearing the PDL bit disables this mode, and the data is switched to the receive data from the line-side. When the PDL bit is cleared, the FDT bit (Offset 0x3C, bit 6) becomes active indicating the successful communication between the Si3017/11/18 and the Si3052. This verifies that the ISOcap™ link is operational.

The remaining test modes require an off-hook sequence to operate. The following sequence defines the off-hook requirements:

1. Powerup or reset.
2. Program the required sample rate.
3. Enable line-side device by clearing PDL bit.
4. Issue off-hook
5. Allow calibration to occur.
6. Set required test mode.

The ISOcap™ digital loopback mode allows the data pump to provide a digital input test pattern and receive that digital test pattern back. To enable this mode, set the DL bit (Offset 0x31, bit 1). The isolation barrier is actually being tested. The digital stream is delivered across the isolation capacitors (C1 and C2) to the line-side device and returned across the same barrier. While an off-hook sequence is necessary, a valid line feed is not needed for this test.

The analog loopback mode allows an external device to drive a signal on the telephone line into the Si3017/11/18 line-side device and have it driven back out onto the line. This mode is for testing external components connecting the RJ-11 jack (TIP and RING) to the Si3017/11/18. To enable this mode, set the AL bit (Offset 0x32, bit 3).

The final testing mode, internal analog loopback, allows the system to test the basic operation of the transmit and receive paths on the line-side device and the external components. In this test mode, the data pump provides a digital test waveform. Data is passed across the isolation barrier, transmitted to and received from the line, passed back across the isolation barrier, and presented to the data pump. To enable this mode, clear the HBE bit (Offset 0x32, bit 1). The test circuit in Figure 2 on page 11 is an adequate line feed for this test.

Note: All test modes are mutually-exclusive. If more than one test mode is enabled concurrently, the results are unpredictable.

Revision Identification

The revision of the system side (Si3052) and line side (Si3017/11/18) can be determined using the SREV[3:0] bits (Offset 0x3B, bits 3:0) and LREV[3:0] bits (Offset 0x3D, bits 5:2), respectively. Table 18 lists the revision values.

Table 18. Revision Values

Revision	Si3052	Si3017/11/18
C	0011	0011
D	0100	0100

Register Map

The Si3052 is designed to provide backwards compatibility to previous designs based on the Si3035 and Si3034 DAAs. When the MAP bit (Offset 0x31, bit 6) is cleared (default value), the Si3052 operates in this backwards-compatible mode. When the MAP bit is set, several bits in the register map become available and several other bits are no longer accessible. The Si3052 is designed to operate in either MAP = 1 or MAP = 0. Following powerup or reset, the desired MAP mode should be selected prior to setting other bits, and the MAP mode should remain in the same state until the next power up or reset. Table 19 shows the bits affected by the state of the MAP bit.

Table 19. Bits selected by MAP bit

MAP = 0	MAP = 1
ATM[1:0], TXM	ATM[7:0]
ARM[1:0], RXM	ARM[7:0]
DCT[1:0]	DCV[1:0]
DIAL	MINI[1:0]
FJM	ILIM
VOL [1:0]	DCR
	HYBx[7:0]

When MAP = 1, the ATM[7:0] bits replace the ATM[1:0] and TXM bits. The ARM[7:0] replaces the ARM[1:0] and RXM bits. The DCV[1:0], MINI[1:0], and ILIM bits replace the DCT[1:0] bits. Table 20 lists the equivalent settings for dc termination.

Table 20. DC Termination Equivalents

	DCV[1:0]	MINI[1:0]	ILIM
DCT[1:0] = 00 (low voltage)	00	11	0
DCT[1:0] = 01 (JATE)	01	11	0
DCT[1:0] = 10 (FCC)	10	00	0
DCT[1:0] = 11 (TBR21)	10	00	1

Table 20 should be used to translate the DCT[1:0] bits in Table 14, “Country Specific Register Settings,” on page 28. The DIAL, FJM, and VOL[1:0] bits do not have a MAP = 1 equivalent and are unused.

The DCR bit switches the dc termination into 800 Ω mode. This is the same mode used by the billing tone detector and overload detector. The HYBx registers are described in the section, "Transhybrid Balance" on page 33.

PCI Configuration Registers

Note: Registers not listed here are reserved and must not be written.

Table 21. PCI Register Summary

Register	Name	Bits															
00h	PCI Device ID and Vendor ID	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		DID[15:0]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		VID[15:0]															
04h	PCI Status and Command	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		DPE	SSE	RMAS	RTAS	STAS	DST[1:0]		DPD	FBBC		C66	CPM	INTS			
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
							INTD	FBBM	SEE	STEP	PEN		MWI		BME	MAE	IOAE
08h	Device Revision Identification	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		CC[23:8]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		CC[7:0]								REV[7:0]							
0Ch	Cache Line Size, Master Latency Timer	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
										HT[7:0]							
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		MLTC[5:0]								CLS[7:0]							
10h	Memory Base Address	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		MBA[31:16]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		MBA[15:0]															
14h	I/O Base Address	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		IOBA[31:16]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		IOBA[15:0]															
2Ch	Subsystem ID, Subsystem Vendor ID	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		SSID[15:0]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		SVID[15:0]															

Table 21. PCI Register Summary (Continued)

Register	Name	Bits															
34h	Capabilities Pointer	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
										CPTR[7:0]							
3Ch	MAX_LAT, MIN_GNT, Interrupt Pin, Interrupt Line	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		MLAT[7:0]								MGNT[7:0]							
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		INTP[7:0]								INTL[7:0]							
40h	Retry Time-out, TRDY Timeout	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		RT[7:0]								TYT[7:0]							
80h	Power Management Capabilities	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		P3C	P3H	PD2	PD1	PD0	D2S	D1S	AUXC[2:0]			DVS		PCL	VER[2:0]		
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		NXT[7:0]								CID[7:0]							
84h	Power Management Control and Status (Vaux powered)	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		PMS	DSC[1:0]		DSE[3:0]				PME							PST[1:0]	

PCI Register 00h. PCI Device ID and Vendor ID

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	DID[15:0]															
Type	R															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	VID[15:0]															
Type	R															

Reset setting = 0x30521543

Bit	Name	Function
31:16	DID[15:0]	**Device Identification.** PCI Device ID is 3052 for the Si3052 device.
15:0	VID[15:0]	**Vendor Identification.** PCI Vendor ID is 1543 for Silicon Laboratories.

PCI Register 04h. PCI Status and Command

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	DPE	SSE	RMAS	RTAS	STAS	DST[1:0]		DPD	FBBC		C66	CPM	INTS			
Type	R	R	R	R	R	R		R	R		R	R	R			
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name						INTD	FBBM	SEE	STEP	PEN		MWI		BME	MAE	IOAE
Type						R/W	R/W	R/W	R	R/W		R/W		R/W	R/W	R/W

Reset setting = 0x02900080

Bit	Name	Function
31	DPE	**Detect Parity Error.**
30	SSE	**Signaled System Error.**
29	RMAS	**Received Master Abort Status.** Set when PCI master terminates a host-to-PCI transaction with a master abort.
28	RTAS	**Received Target Abort Status.** Set when the Si3052 initiates a PCI transaction and it is terminated by the target.
27	STAS	**Signaled Target Abort Status.**
26:25	DST[1:0]	**Device Select Timing.** Indicates timing of $\overline{\text{DEVSEL}}$ when the Si3052 responds to a PCI transaction as a target.
24	DPD	**Data Parity Detected.**
23	FBBC	**Fast Back-to-Back Capable Status Flag.**
22	Reserved	Read returns zero.
21	C66	**66 MHz Capable Status Flag.**
20	CPM	**Capabilities List.** PME supported.
19	INTS	**Interrupt Status.**
18:11	Reserved	Read returns zero.
10	INTD	**Interrupt Disable.**
9	FBBM	**Fast Back-to-Back Master Enable.**
8	SEE	**System Error Enable**
7	STEP	**Data Stepping Enable.**
6	PEN	**Parity Error Enable.**
5	Reserved	Read returns zero.
4	MWI	**Memory Write and Invalidate Enable.**
3	Reserved	Read returns zero.
2	BME	**Bus Master Enable.**
1	MAE	**Memory Access Enable.**
0	IOAE	**I/O Access Enable.**

PCI Register 08h. Device Revision Identification

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	CC[23:8]															
Type	R															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	CC[7:0]								REV[7:0]							
Type	R								R							

Reset setting = 0x07030003

Bit	Name	Function
31:8	CC[23:0]	**Class Code.**
7:0	REV[7:0]	**Revision Identification Number.**

PCI Register 0Ch. Cache Line Size, Master Latency Timer

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name									HT[7:0]							
Type	R															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	MLTC[5:0]								CLS[7:0]							
Type	R/W								R/W							

Reset setting = 0x00000000

Bit	Name	Function
31:24	Reserved	Read returns zero.
23:16	HT[7:0]	**Header Type.** A single function, non-bridge type header format.
15:10	MLTC[5:0]	**Master Latency Timer Count.** Sets the minimum number of PCI clock cycles that the Si3052 is guaranteed access to the PCI bus. After the count has expired, the Si3052 surrenders the PCI bus when other PCI master devices are granted the bus by the arbiter. Programmable in increments of 1 ms.
9:8	Reserved	Read returns zero.
7:0	CLS[7:0]	**Cache Line Size.** All cache type transactions are aliases to normal reads and writes.

PCI Register 10h. Memory Base Address

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	MBA[31:16]															
Type	R/W															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	MBA[15:0]															
Type	R/W															

Reset setting = 0x00000000

Bit	Name	Function
31:0	MBA[31:0]	**Memory Base Address.** Memory space is in 4096 byte increments.

PCI Register 14h. I/O Base Address

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	IOBA[31:16]															
Type	R/W															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IOBA[15:0]															
Type	R/W															

Reset setting = 0x00000001

Bit	Name	Function
31:0	IOBA[31:0]	**I/O Base Address.** I/O space is 256 bytes.

PCI Register 2Ch. Subsystem ID, Subsystem Vendor ID

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	SSID[15:0]															
Type	R															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SVID[15:0]															
Type	R															

Reset setting = N/A

Bit	Name	Function
31:16	SSID[15:0]	**PCI Subsystem ID.** EPROM or resistor ID configurable.
15:0	SVID[15:0]	**PCI Subsystem Vendor ID.** EPROM or resistor ID configurable.

PCI Register 34h. Capabilities Pointer

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name																
Type																
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name									CPTR[7:0]							
Type		R														

Reset setting = 0x00000080

Bit	Name	Function
31:8	Reserved	Read returns zero.
7:0	CPTR[7:0]	**Capabilities Pointer.** Location of PME information.

PCI Register 3Ch. MAX_LAT, MIN_GNT, Interrupt Pin, Interrupt Line

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	MLAT[7:0]								MGNT[7:0]							
Type	R								R							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	INTP[7:0]								INTL[7:0]							
Type	R								R/W							

Reset setting = 0x3E010100

Bit	Name	Function
31:24	MLAT[7:0]	**MAX_LAT.** Sets the value of MAX_LAT. See PCI 2.2 specification, section 6.2.4 (250 ns units). The maximum latency between bus grants is limited to 62–250 ns.
23:16	MGNT[7:0]	**MIN_GNT.** Identifies the length of the burst period, assuming a 33 MHz clock (250 ns units). A minimum grant of 250 ns is required for burst transactions.
15:8	INTP[7:0]	**Interrupt Pin.** Identifies which interrupt pin the Si3052 uses. Default interrupt pin is $\overline{\text{INTA}}$.
7:0	INTL[7:0]	**Interrupt Line.** Identifies the interrupt line register to which the Si3052 is connected.

PCI Register 40h. Retry Timeout, TRDY Timeout

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name																
Type																
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RT[7:0]								TYT[7:0]							
Type	R								R							

Reset setting = 0x00000000

Bit	Name	Function
31:16	Reserved	Read returns zero.
15:8	RT[7:0]	**Retry Timeout.** Sets number of retries that the Si3052 as master performs.
7:0	TYT[7:0]	**TRDY Timeout.** Sets number of PCI clocks that the Si3052 as master waits for TRDY.

PCI Register 80h. Power Management Capabilities

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	P3C	P3H	PD2	PD1	PD0	D2S	D1S	AUXC[2:0]			DVS		PCL	VER[2:0]		
Type	R	R	R	R	R	R	R	R			R		R	R		
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	NXT[7:0]								CID[7:0]							
Type	R								R							

Reset setting = 0xC8420001

Bit	Name	Function
31	P3C	**PME Support D3 Cold.** ANDed with 3.3 Vaux pin.
30	P3H	**PME Support D3 Hot.**
29	PD2	**PME Support D2.** Not supported.
28	PD1	**PME Support D1.** Not supported.
27	PD0	**PME Support D0.**
26	D2S	**D2 Support.** Not supported.
25	D1S	**D1 Support.** Not supported.
24:22	AUXC[2:0]	**Aux_Current.** Less than 55 mA in D3 cold.
21	DVS	**Device Specific.**
20	Reserved	Read returns zero.
19	PCL	**PME Clock.**
18:16	VER[2:0]	**Version.** Complies with PPM 1.1.
15:8	NXT[7:0]	**Next Item.**
7:0	CID[7:0]	**Capability ID.**

PCI Register 84h. Power Management Control and Status (Vaux powered register)

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name																
Type																
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PMS	DSC[1:0]		DSE[3:0]				PME							PST[1:0]	
Type	R/W	R		R				R/W							R/W	

Reset setting = 0x00000000

Bit	Name	Function
31:16	Reserved	Read returns zero.
15	PMS	**PME Status (sticky).** Write 1 to clear.
14:13	DSC[1:0]	**Data Scale.** No data register implemented.
12:9	DSE[3:0]	**Data Select.** No data register implemented.
8	PME	**PME Enable (sticky).**
7:2	Reserved	Read returns zero.
1:0	PST[1:0]	**Power State.** 00 = D0 01 = D1 (Not supported) 10 = D2 (Not supported) 11 = D3 Hot

PCI and DAA Control Registers

Note: Registers not listed here are reserved and must not be written.

Table 22. PCI Register Summary (32-Bit)

Offset	Name	Bits															
0x00	DMA and Interrupt Control	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
									MTIE	DIE	WIE	TAIE	MAIE	RBIE	RAIE	WAIE	WBIE
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
					DM[1:0]			DMAR	DMAE	DMAM	DMAI					DRST	PRST
0x04	DMA and Interrupt Status	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
										DAA	EER	WFU	WFF	WFE	RFO	RFF	RFE
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
									MTO	DIS	WIS	PTA	PMA	DRB	DRA	DWA	DWB
0x08	DMA Read Address Start	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		DRAS[31:16]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		DRAS[15:0]															
0x0C	DMA Read Address Stop	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		DRAP[31:16]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		DRAP[15:0]															
0x10	DMA Read Address Interrupt	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		DRAI[31:16]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		DRAI[15:0]															
0x14	Current DMA Read Address	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		CDRA[31:16]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		CDRA[15:0]															
0x18	DMA Write Address Start	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		DWAS[31:16]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		DWAS[15:0]															

Table 22. PCI Register Summary (32-Bit) (Continued)

Offset	Name	Bits															
0x1C	DMA Write Address Stop	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		DWAP[31:16]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		DWAP[15:0]															
0x20	DMA Write Address Interrupt	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		DWAI[31:16]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		DWAI[15:0]															
0x24	Current DMA Write Address	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
		CDWA[31:16]															
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		CDWA[15:0]															
0x28	Watchdog Timer	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
							STPM	STPE	XTAL							WTS	WTC
		D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		WDT[15:0]															

Table 23. DAA Register Summary (8-Bit)

Offset	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x31	Control 1	SR	MAP	PWMM[1:0]		PWME		DL	
0x32	Control 2				WDTE	AL	RDM	HBE	RXE
0x33	Interrupt Mask	RDTM	ROVM	FDTM	BTDM	DODM	LCSM		
0x34	Interrupt Source	RDTI	ROVI	FDTI	BTDI	DODI	LCSI		
0x35	DAA Control 1		RDTN	RDTP		ONHM	RDT		OH
0x36	DAA Control 2		ATM[1][1]	ARM[1][1]	PDL	PDN		ATM[0][1]	ARM[0][1]
0x37	Sample Rate Control					SRC[3:0]			
0x38	Reserved								
0x39	Reserved								
0x3A	DAA Control 3								DDL
0x3B	System-side Revision	LSID[3:0]				SREV[3:0]			
0x3C	Line-Side Status		FDT		LCS[4:0]				
0x3D	Line-Side Revision			LREV[3:0]					
0x3E	Reserved								
0x3F	TX/RX Gain Control	TXM[1]	ATX[2:0]			RXM[1]	ARX[2:0]		
0x40	International Control 1	ACT2	OHS	ACT	IIRE	DCT[1:0][1]		RZ	RT
0x41	International Control 2	CALZ	MCAL	CALD		OPE	BTE	ROV	BTD
0x42	International Control 3		DIAL[1]	FJM[1]	VOL[1:0][1]			RFWE	
0x43	International Control 4						OVL		OPD
0x44	AOUT RX Attenuation	ARM[7:0][2]							
0x45	AOUT TX Attenuation	ATM[7:0][2]							
0x46	Ring Validation Control 1	RDLY[1:0]		RMX[5:0]					
0x47	Ring Validation Control 2	RDLY[2]	RTO[3:0]				RCC[2:0]		
0x48	Ring Validation Control 3	RNGV		RAS[5:0]					
0x49	Resistor Calibration			RCALD					
0x4A	DC Termination Control	DCV[1:0][2]		MINI[1:0][2]				ILIM[2]	DCR[2]
0x4B	Reserved								
0x4C	Reserved								
0x4D	Reserved								

Note: All register bits are available when MAP = 0 and MAP = 1 except
1. Only available when MAP = 0
2. Only available when MAP = 1

Table 23. DAA Register Summary (8-Bit) (Continued)

Offset	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x4E	Reserved								
0x4F	DAA Control 4		FOH[1:0]			OHS2			
0x5D	Hybrid 1	HYB1[7:0][2]							
0x5E	Hybrid 2	HYB2[7:0][2]							
0x5F	Hybrid 3	HYB3[7:0][2]							
0x60	Hybrid 4	HYB4[7:0][2]							
0x61	Hybrid 5	HYB5[7:0][2]							
0x62	Hybrid 6	HYB6[7:0][2]							
0x63	Hybrid 7	HYB7[7:0][2]							
0x64	Hybrid 8	HYB8[7:0][2]							
0x65	Reserved								
0x66	Reserved								
0x67	Reserved								
0x68	Reserved								
0x69	Reserved								
0x6A	Reserved								
0x6B	Spark Quenching Control		SQ1		SQ0				

Note: All register bits are available when MAP = 0 and MAP = 1 except
1. Only available when MAP = 0
2. Only available when MAP = 1

PCI Register Offset 0x00 DMA and Interrupt Control

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name								MTIE	DIE	WIE	TAIE	MAIE	RBIE	RAIE	WAIE	WBIE
Type								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name				DM[1:0]			DMAR	DMAE	DMAM	DMAI					DRST	PRST
Type				R/W			R/W	R/W	R/W	R/W					R/W	R/W

Reset setting = 0x00000000

Bit	Name	Function
31:25	Reserved	Read returns zero.
24	MTIE	**DMA Master Timeout Interrupt Enable.** 0 = Interrupt disable. 1 = Interrupt enable.
23	DIE	**DAA Interrupt Enable.** 0 = Interrupt disable. 1 = Interrupt enable.
22	WIE	**Watchdog Timer Interrupt Enable.** 0 = Interrupt disable. 1 = Interrupt enable.
21	TAIE	**PCI Target Abort Interrupt Enable.** 0 = Interrupt disable. 1 = Interrupt enable.
20	MAIE	**PCI Master Abort Interrupt Enable.** 0 = Interrupt disable. 1 = Interrupt enable.
19	RBIE	**DMA Read End of Buffer Interrupt Enable.** 0 = Interrupt disable. 1 = Interrupt enable.
18	RAIE	**DMA Read Address Interrupt Enable.** 0 = Interrupt disable. 1 = Interrupt enable.
17	WAIE	**DMA Write Address Interrupt Enable.** 0 = Interrupt disable. 1 = Interrupt enable.
16	WBIE	**DMA Write End of Buffer Interrupt Enable.** 0 = Interrupt disable. 1 = Interrupt enable.

Bit	Name	Function
15:13	Reserved	Read returns zero.
12:11	DM[1:0]	**Data Mode.** 00 = Direct. 01 = Indirect, Parallel. 10 = Indirect, Serial, LSB first. 11 = Indirect, Serial, MSB first.
10	Reserved	Read returns zero.
9	DMAR	**DMA Restart.** 0 = DMA continue. 1 = DMA restart.
8	DMAE	**DMA Enable.** 0 = DMA disable. 1 = DMA enable.
7	DMAM	**DMA Master Mode.** 0 = Multiple mode. 1 = Single mode.
6	DMAI	**DMA Interrupt Mode.** 0 = Interrupt status bit is sticky. 1 = Interrupt status bit is non-sticky. Applies to address and end-of-buffer interrupts.
5:2	Reserved	Read returns zero.
1	DRST	**DMA Reset.** 0 = DMA continue. 1 = DMA reset.
0	PRST	**PCI DAA Soft Reset.** 0 = Normal operation. 1 = DAA reset. The PCI registers are not affected. All DAA registers are reset to default values. Write zero to clear.

PCI Register Offset 0x04 DMA and Interrupt Status

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name									DAA	EER	WFU	WFF	WFE	RFO	RFF	RFE
Type									R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name								MTO	DIS	WIS	PTA	PMA	DRB	DRA	DWA	DWB
Type								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset setting = 0x00000000

Bit	Name	Function
31:24	Reserved	Read returns zero.
23	DAA	**DAA Status.** 0 = DAA ready. 1 = DAA not ready.
22	EER	**EPROM Read Status.** 0 = No status. 1 = EPROM read failure.
21	WFU	**DMA Write FIFO Underrun.**
20	WFF	**DMA Write FIFO Full.**
19	WFE	**DMA Write FIFO Empty.**
18	RFO	**DMA Read FIFO Overrun.**
17	RFF	**DMA Read FIFO Full.**
16	RFE	**DMA Read FIFO Empty.**
15:9	Reserved	Read returns zero.
8	MTO	**DMA Master Timeout Status.** 0 = Normal operation. 1 = Master timeout from TRDY timer or retry timer. Write 1 to clear.
7	DIS	**DAA Interrupt Status.** 0 = Normal operation. 1 = DAA interrupt has occurred. Write 1 to clear.
6	WIS	**Watchdog Timer Interrupt Status.** 0 = Normal operation. 1 = Watchdog timer has expired. Write 1 to clear.
5	PTA	**PCI Target Abort Interrupt Status.** 0 = Normal operation. 1 = PCI Target Abort has occurred. Write 1 to clear.

Bit	Name	Function
4	PMA	**PCI Master Abort Interrupt Status.** 0 = Normal operation. 1 = PCI Master Abort has occurred. Write 1 to clear.
3	DRB	**DMA Read End of Buffer Interrupt Status.** 0 = Normal operation. 1 = DMA Read has reached end of buffer. Write 1 to clear.
2	DRA	**DMA Read Address Interrupt Status.** 0 = Normal operation. 1 = DMA Read has reached interrupt address. Write 1 to clear.
1	DWA	**DMA Write Address Interrupt Status.** 0 = Normal operation. 1 = DMA Write has reached interrupt address. Write 1 to clear.
0	DWB	**DMA Write End of Buffer Interrupt Status.** 0 = Normal operation. 1 = DMA Write has reached end of buffer. Write 1 to clear.

PCI Register Offset 0x08 DMA Read Address Start

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	DRAS[31:16]															
Type	R/W															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRAS[15:0]															
Type	R/W															

Reset setting = 0x00000000

Bit	Name	Function
31:0	DRAS[31:0]	**DMA Read Address Start.**

PCI Register Offset 0x0C DMA Read Address Stop

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	DRAP[31:16]															
Type	R/W															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRAP[15:0]															
Type	R/W															

Reset setting = 0x00000000

Bit	Name	Function
31:0	DRAP[31:0]	**DMA Read Address Stop.**

PCI Register Offset 0x10 DMA Read Address Interrupt

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	DRAI[31:16]															
Type	R/W															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRAI[15:0]															
Type	R/W															

Reset setting = 0x00000000

Bit	Name	Function
31:0	DRAI[31:0]	**DMA Read Address Interrupt.**

PCI Register Offset 0x14 Current DMA Read Address

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	CDRA[31:16]															
Type	R															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	CDRA[15:0]															
Type	R															

Reset setting = 0x00000000

Bit	Name	Function
31:0	CDRA[31:0]	**Current DMA Read Address.**

PCI Register Offset 0x18 DMA Write Address Start

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	DWAS[31:16]															
Type	R/W															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DWAS[15:0]															
Type	R/W															

Reset setting = 0x00000000

Bit	Name	Function
31:0	DWAS[31:0]	**DMA Write Address Start.**

PCI Register Offset 0x1C DMA Write Address Stop

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	DWAP[31:16]															
Type	R/W															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DWAP[15:0]															
Type	R/W															

Reset setting = 0x00000000

Bit	Name	Function
31:0	DWAP[31:0]	**DMA Write Address Stop.**

PCI Register Offset 0x20 DMA Write Address Interrupt

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	DWAI[31:16]															
Type	R/W															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DWAI[15:0]															
Type	R/W															

Reset setting = 0x00000000

Bit	Name	Function
31:0	DWAI[31:0]	**DMA Write Address Interrupt.**

PCI Register Offset 0x24 Current DMA Write Address

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name	CDWA[31:16]															
Type	R															
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	CDWA[15:0]															
Type	R															

Reset setting = 0x00000000

Bit	Name	Function
31:0	CDWA[31:0]	**Current DMA Write Address.**

PCI Register Offset 0x28 Watchdog Timer

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Name						STPM	STPE	XTAL							WTS	WTC
Type						R/W	R/W	R/W							R/W	R/W
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	WDT[15:0]															
Type	R/W															

Reset settings = 0x02000000

Bit	Name	Function
31:27	Reserved	Read returns zero.
26	STPM	**Address/Data Stepping Mode.** 0 = 4 steps. 1 = 2 steps.
25	STPE	**Address/Data Stepping Enable.** 0 = Disabled. 1 = Enabled.
24	XTAL	**External Crystal Frequency Select.** 0 = 16.384 MHz 1 = 32.768 kHz
25:18	Reserved	Read returns zero.
17	WTS	**PCI Watchdog Timer Status.** 0 = Watchdog timer idle/counting. 1 = Watchdog timer expired.
16	WTC	**PCI Watchdog Timer Control.** 0 = Watchdog timer disabled. 1 = Watchdog timer enabled. When set this bit is cleared by a hardware reset.
15:0	WDT[15:0]	**PCI Watchdog Timer.** Timer is free running and clocked by the PCI system clock. For 33 MHz PCI, the timer increments every (256/33 MHz) = 7.76 μs. The timer overflows in 508 ms without register accesses, generating an interrupt and stopping DMA operations.

DAA Register Offset 0x31 Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR	MAP	PWMM[1:0]		PWME		DL	
Type	R/W	R/W	R/W		R/W		R/W	

Reset settings = 0000_0000

Bit	Name	Function
7	SR	**Software Reset.** 0 = Enables Si3052 for normal operation. 1 = Sets all registers to their reset value. **Note:** Bit clears automatically after being set.
6	MAP	**Register Map.** 0 = Basic register set (Si3014 compatible) selected. 1 = Enhanced register set selected. **Note:** This bit should be set during initialization only.
5:4	PWMM[1:0]	**Pulse-Width Modulation Mode.** Selects the type of signal on the call progress AOUT pin. 00 = PWM output clocked at 16.384 MHz. A local density of 1s and 0s tracks the combined transmit and receive signal. 01 = Balanced conventional PWM output signal has high and low portions of the modulated pulse centered on the 32 kHz sample clock. 10 = Conventionally PWM output signal returns to 0 at 32 kHz intervals and rises at a time in the 32 kHz period proportional to the instantaneous amplitude. 11 = Reserved
3	PWME	**Pulse-Width Modulation Enable.** 0 = Call progress PWM AOUT disabled. 1 = Call progress PWM AOUT enabled.
2	Reserved	Read returns zero.
1	DL	**Isolation Digital Loopback.** 0 = Digital loopback across isolation barrier disabled. 1 = Enables digital loopback mode across isolation barrier. The line-side device must be enabled and off-hook before setting this mode. This data path includes RX and TX filters. A valid phone line is not necessary for this mode.
0	Reserved	Read returns zero.

DAA Register Offset 0x32 Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				WDTE	AL	RDM	HBE	RXE
Type				R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0011

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	WDTE	**DAA Watchdog Timer Enable.** 0 = Watchdog timer disabled. 1 = Watchdog timer enabled. When set, this bit is cleared only by a hardware reset. The watchdog timer monitors DAA register writes. If a register write does not occur within a 4.096 second window, the DAA is put into an on-hook state. Only a write of a DAA register restarts the timer.
3	AL	**Analog Loopback.** 0 = Analog loopback mode disabled. 1 = Enables external analog loopback mode.
2	RDM	**Ring Detect Mode.** 0 = Ring detect on positive threshold. 1 = Ring detect on positive and negative threshold.
1	HBE	**Hybrid Enable.** 0 = Disconnects hybrid in transmit path. 1 = Connects hybrid in transmit path.
0	RXE	**Receive Enable.** 0 = Receive path disabled. 1 = Enables receive path.

DAA Register Offset 0x33 Interrupt Mask

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDTM	ROVM	FDTM	BTDM	DODM	LCSM		
Type	R/W	R/W	R/W	R/W	R/W	R/W		

Reset settings = 0000_0000

Bit	Name	Function
7	RDTM	**Ring Detect Interrupt Mask.** 0 = A ring signal does not cause an interrupt. 1 = A ring signal causes an interrupt.
6	ROVM	**Receive Overload Interrupt Mask.** 0 = A receive overload does not cause an interrupt. 1 = A receive overload causes an interrupt.
5	FDTM	**Frame Detect Interrupt Mask.** 0 = ISOcap frame lock does not cause an interrupt. 1 = ISOcap frame lock causes an interrupt.
4	BTDM	**Billing Tone Detect Interrupt Mask.** 0 = A billing tone does not cause an interrupt. 1 = A billing tone causes an interrupt.
3	DODM	**Drop Out Detect Interrupt Mask.** 0 = A line supply dropout does not cause an interrupt. 1 = A line supply dropout causes an interrupt.
2	LCSM	**Loop Current Sense Overload Interrupt Mask.** 0 = Loop current sense overload does not cause an interrupt. 1 = Loop current sense overload causes an interrupt.
1:0	Reserved	Read returns zero.

DAA Register Offset 0x34 Interrupt Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDTI	ROVI	FDTI	BTDI	DODI	LCSI		
Type	R/W	R/W	R/W	R/W	R/W	R/W		

Reset settings = 0000_0000

Bit	Name	Function
7	RDTI	**Ring Detect Interrupt Status.** 0 = No ring. 1 = Ring detected. Write 0 to clear.
6	ROVI	**Receive Overload Interrupt Status.** 0 = No receive overload. 1 = Receive overload detected. Write 0 to clear.
5	FDTI	**Frame Detect Interrupt Status.** 0 = Frame detect established. 1 = Frame detect lost. Write 0 to clear.
4	BTDI	**Billing Tone Detect Interrupt Status.** 0 = No billing tone. 1 = Billing tone detected. Write 0 to clear.
3	DODI	**Drop Out Detect Interrupt Status.** 0 = Line-side power available. 1 = Line-side power unavailable. Reads 1 when off hook.
2	LCSI	**Loop Current Sense Overload Interrupt.** 0 = The LCS bits have not reached max (all ones). 1 = The LCS bits have reached max value. If the LCSM bit is set, a hardware interrupt occurs. This bit must be written to 0 to clear it. LCSI does not necessarily imply that an overload situation has occurred. An overload situation in the DAA is determined by the status of the OPD bit. After the LCSI interrupt fires, the OPD bit should be checked to determine if an overload situation exists.
1:0	Reserved	Read returns zero.

DAA Register Offset 0x35 DAA Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		RDTN	RDTP		ONHM	RDT		OH
Type		R	R		R/W	R		R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	RDTN	**Ring Detect Signal Negative.** 0 = No ring signal is occurring. 1 = A negative ring signal is occurring.
5	RDTP	**Ring Detect Signal Positive.** 0 = No ring signal is occurring. 1 = A positive ring signal is occurring.
4	Reserved	Read returns zero.
3	ONHM	**On-Hook Line Monitor.** 0 = Normal on-hook mode. 1 = Enables low-power monitoring mode allowing the DSP to receive line activity without going off-hook. This mode is used for caller-ID detection.
2	RDT	**Ring Detect.** 0 = Reset either 4.5–9 seconds after last positive ring is detected or when the system executes an off-hook. 1 = Indicates a ring is occurring.
1	Reserved	Read returns zero.
0	OH	**Off-Hook.** 0 = Line-side device on-hook. 1 = Causes the line-side device to go off-hook.

DAA Register Offset 0x36 DAA Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		ATM[1]	ARM[1]	PDL	PDN		ATM[0]	ARM[0]
Type		R/W	R/W	R/W	R/W		R/W	R/W

Reset settings = 0111_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6,1	ATM[1:0]	**AOUT Transmit Path Level Control (MAP = 0 only).** 00 = –20 dB transmit path attenuation for call progress AOUT pin only. 01 = –32 dB transmit path attenuation for call progress AOUT pin only. 10 = Mutes transmit path for call progress AOUT pin only. 11 = –26 dB transmit path attenuation for call progress AOUT pin only.
5,0	ARM[1:0]	**AOUT Receive Path Level Control (MAP = 0 only).** 00 = 0 dB receive path attenuation for call progress AOUT pin only. 01 = –12 dB receive path attenuation for call progress AOUT pin only. 10 = Mutes receive path for call progress AOUT pin only. 11 = –6 dB receive path attenuation for call progress AOUT pin only.
4	PDL	**Powerdown Line-Side Chip.** 0 = Normal operation. Program the clock generator before clearing this bit. 1 = Powers down the Si3017/11/18.
3	PDN	**Powerdown PCI DAA.** 0 = Normal operation. 1 = Powers down the DAA logic. A DAA soft reset is required to restore normal operation. The PCI interface is not affected.
2	Reserved	Read returns zero.

DAA Register Offset 0x37 Sample Rate Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					SRC[3:0]			
Type	R/W							

Reset settings = 0000_0001

Bit	Name	Function
7:4	Reserved	Read returns zero.
3:0	SRC[3:0]	**Sample Rate Control.** Sets the sampling rate. 0000 = 7200 Hz 0001 = 8000 Hz 0010 = 8229 Hz 0011 = 8400 Hz 0100 = 9000 Hz 0101 = 9600 Hz 0110 = 10286 Hz 0111 = 12000 Hz 1000 = 13714 Hz 1001 = 16000 Hz 1010–1111 = Reserved

DAA Register Offset 0x38 Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

DAA Register Offset 0x39 Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

DAA Register Offset 0x3A DAA Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								DDL
Type								R/W

Reset settings = 0000_0000

Bit	Name	Function
7:1	Reserved	Read returns zero.
0	DDL	**Digital Data Loopback.** 0 = Normal Operation. 1 = Loopback transmit to receive before the filters. Output data is identical to input data.

DAA Register Offset 0x3B System-side Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LSID[3:0]				SREV[3:0]			
Type	R				R			

Reset settings = xxxx_xxxx

Bit	Name	Function
7:4	LSID[3:0]	**Line-Side ID.** 0000 = Si3017 FCC 0001 = Si3018 Global 0100 = Si3011 TBR21 Other = Reserved
3:0	SREV[3:0]	**System-Side Revision.** Four bit value indicating the revision of the Si3052 device. 0011 = Rev C 0100 = Rev D

DAA Register Offset 0x3C Line-side Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FDT		LCS[4:0]				
Type	R			R				

Reset settings = N/A

Bit	Name	Function
7	Reserved	Read returns zero.
6	FDT	**Frame Detect.** 0 = Indicates ISOcap link has not established frame lock. 1 = Indicates ISOcap link frame lock is established.
5	Reserved	Read returns zero.
4:0	LCS[4:0]	**Loop Current Sense.** Five-bit value returning the loop current in 3.3 mA/bit resolution when the DAA is in an off-hook state. 00000 = Indicates the loop current is less than required for normal operation. 00100 = Indicates minimum loop current for normal operation. 11111 = Indicates a loop current is > 127 mA.

DAA Register Offset 0x3D Line-Side Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			LREV[3:0]					
Type	R							

Reset settings = 00xx_xx00

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:2	LREV[3:0]	**Line-Side Revision.** Four-bit value indicating the revision of the Si3017/11/18 device. 0011 = Rev C 0100 = Rev D
1:0	Reserved	Read returns zero.

DAA Register Offset 0x3E Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

DAA Register Offset 0x3F TX/RX Gain Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXM	ATX[2:0]			RXM	ARX[2:0]		
Type	R/W	R/W			R/W	R/W		

Reset settings = 0000_0000

Bit	Name	Function
7	TXM	**Transmit Mute (MAP = 0 only).** 0 = Transmit signal is not muted. 1 = Mutes the transmit signal.
6:4	ATX[2:0]	**Analog Transmit Attenuation.** 000 = 0 dB attenuation 001 = 3 dB attenuation 010 = 6 dB attenuation 011 = 9 dB attenuation 1xx = 12 dB attenuation
3	RXM	**Receive Mute (MAP = 0 only).** 0 = Receive signal is not muted. 1 = Mutes the receive signal.
2:0	ARX[2:0]	**Analog Receive Gain.** 000 = 0 dB gain 001 = 3 dB gain 010 = 6 dB gain 011 = 9 dB gain 1xx = 12 dB gain

DAA Register Offset 0x40 International Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ACT2	OHS	ACT	IIRE	DCT[1:0]		RZ	RT
Type	R/W	R/W	R/W	R/W	R/W		R/W	R/W

Reset settings = 0000_1000

Bit	Name	Function
7	ACT2	**AC Termination Select 2.** Works with the ACT bit to select one of four ac terminations. **Si3018 settings:** **ACT2 ACT AC Termination** 0 0 Real, 600 Ω 0 1 Global complex impedance 1 0 TBR21 complex impedance 1 1 New Zealand complex impedance The global complex impedance satisfies minimum return loss requirements in a country requiring a complex ac termination. The other complex impedances can be used for improved return loss performance. **Si3011 Settings:** **ACT2 ACT AC Termination** 0 0 Real, 600 Ω 0 1 TBR21 complex impedance 1 0 TBR21 complex impedance 1 1 Real, 600 Ω **Si3017 Settings:** **ACT2 ACT AC Termination** X X Real, 600 Ω
6	OHS	**On-Hook Speed.** This bit, in combination with the OHS2 bit and the SQ[1:0] bits, sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **Si3018 settings:** **OHS OHS2 SQ[1:0] Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec) **Si3011 and Si3017 settings:** **OHS OHS2 SQ[1:0] Mean On-Hook Speed** X X XX Less than 0.5 ms
5	ACT	**AC Termination Select.** When the ACT2 bit is cleared, the ACT bit selects the following: 0 = Selects the real impedance (600 W). 1 = Selects the complex impedance.
4	IIRE	**IIR Filter Select.** 0 = FIR Filter selected. 1 = IIR Filter selected.

Bit	Name	Function
3:2	DCT[1:0]	**DC Termination Select (MAP = 0 only).** **Si3018 settings:** 00 = Low voltage mode. 01 = Japan, Lower voltage mode. 10 = FCC, Standard voltage mode. 11 = TBR21, Current limiting mode. **Si3011 settings:** 00,10 = FCC, standard voltage mode. 01,11 = TBR21, current limiting mode. **Si3017 settings:** XX = FCC, standard voltage mode.
1	RZ	**Ringer Impedance.** **Si3018 settings:** 0 = Maximum (high) ringer impedance. 1 = Synthesize ringer impedance. See “Ringer Impedance and Threshold” on page 34.. **Si3011 and Si3017 settings:** X = Maximum (high) ringer impedance.
0	RT	**Ringer Threshold Select.** Satisfies country requirements on ring detection. Signals below the lower level do not generate a ring detection; signals above the upper level are guaranteed to generate a ring detection. **Si3018 settings:** 0 = 11 to 22 Vrms 1 = 17 to 33 V_{rms} **Si3011 and Si3017 settings:** X = 11 to 22 V_{rms}

DAA Register Offset 0x41 International Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CALZ	MCAL	CALD		OPE	BTE	ROV	BTD
Type	R/W	R/W	R/W		R/W	R/W	R/W	R/W

Reset Settings = 0000_0000

Bit	Name	Function
7	CALZ	**Clear Calibration.** 0 = Normal operation. 1 = Clear calibration data. This bit must be written back to 0 after being set.
6	MCAL	**Manual Calibration.** 0 = No calibration. 1 = Initiate calibration.
5	CALD	**Auto-Calibration Disable.** 0 = Enable auto-calibration. 1 = Disable auto-calibration.
4	Reserved	Read returns zero.
3	OPE	**Overload Protect Enable.** 0 = Disabled. 1 = Enabled. When the OPE bit is set, the OPD indicates when an overload condition is occurring. The OPD bit should always be cleared before going off-hook, and set 25 ms following off-hook in order to prevent false overload detections.
2	BTE	**Billing Tone Protect Enable.** When set, the DAA can detect a billing tone signal on the line and maintain an off-hook state through the billing tone. If a billing tone is detected, the BTD bit is set to indicate the event. 0 = Billing tone detection disabled. The BTD bit is not functional. 1 = Billing tone detection enabled. The BTD is functional.
1	ROV	**Receive Overload.** Set when the receive input has an excessive input level (i.e., receive pin goes below ground). Cleared by writing a zero to this location (sticky). 0 = Normal receive input level. 1 = Excessive receive input level.
0	BTD	**Billing Tone Detected.** Set if a billing tone is detected. Automatically cleared (non-sticky). 0 = No billing tone detected. 1 = Billing tone detected.

DAA Register Offset 0x42 International Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		DIAL	FJM	VOL[1:0]			RFWE	
Type		R/W	R/W	R/W			R/W	

Reset Settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	DIAL	**DTMF Dialing Mode (MAP = 0 only).** **Si3018 settings:** 0 = Normal operation. 1 = Increase headroom for DTMF dialing. **Si3011 and Si3017 settings:** X = Normal operation.
5	FJM	**Force Japan DC Termination Mode (MAP = 0 only).** **Si3018 settings:** 0 = Normal operation. 1 = When DCT[1:0], is set to 10_b (FCC mode), setting this bit forces the Japan dc termination mode. **Si3011 and Si3017 settings:** X = Normal operation.
4:3	VOL[1:0]	**Line Voltage Adjust (MAP = 0 only).** When set, this bit adjusts the TIP-RING line voltage. Lowering this voltage improves margin in low voltage countries. **Si3018 settings:** 00 = Normal operation. 01 = –0.125 V below Japan mode. 10 = equivalent to DCT[1:0] = 01 (Japan mode). 11 = equivalent to DCT[1:0] = 01 (Japan mode). **Si3011 and Si3017 settings:** XX = Normal operation.
2	Reserved	Read returns zero.
1	RFWE	**Ring Detector Full-Wave Rectifier Enable.** When RNGV is disabled, this bit controls the ring detector mode. When RNGV is enabled, this bit configures the RDT bit to either follow the ringing signal detected by the ring validation circuit, or to follow an unqualified ring detect one-shot signal initiated by a ring-threshold crossing and terminated by a fixed counter timeout of approximately five seconds. **RNGV RFWE RDT bit** 0 0 Half-Wave 0 1 Full-Wave 1 0 Validated Ring Envelope 1 1 Ring Threshold Crossing One-Shot
0	Reserved	Read returns zero.

DAA Register Offset 0x43 International Control 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						OVL		OPD
Type						R		R

Reset Settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	OVL	**Overload Detected.** Has the same function as ROV but clears itself after the overload is removed. See “Billing Tone Detection and Receive Overload” on page 35. Masked by the off-hook counter only and is not affected by the BTE bit. 0 = Normal receive input level. 1 = Excessive receive input level.
1	Reserved	Read returns zero.
0	OPD	**Overload Protect Detect.** This bit is used to indicate that the DAA has detected a line feed overload. The detector firing threshold depends on the setting of the ILIM bit. **OPD ILIM Overload Threshold Overload Status** 0 0 160 mA No overload condition exists 0 1 60 mA No overload condition exists 1 0 160 mA An overload condition has been detected 1 1 60 mA An overload condition has been detected This bit must be enabled by setting the OPE bit. OPD is a sticky bit and is cleared by writing OPE to zero.

DAA Register Offset 0x44 Call Progress Receive Attenuation (MAP = 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ARM[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	ARM[7:0]	**AOUT Receive Path Attenuation.** When decremented from the default setting, these bits linearly attenuate the AOUT receive path signal used for call progress monitoring. Setting the bits to 0s mutes the AOUT receive path. 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB ... 0000_0000 = Mute
Note: Function available when DAA Register offset 0x31 bit 6 is set to 1 (MAP = 1).		

DAA Register Offset 0x45 Call Progress Transmit Attenuation (MAP = 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ATM[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	ATM[7:0]	**AOUT Receive Path Attenuation.** When decremented from the default setting, these bits linearly attenuate the AOUT transmit path signal used for call progress monitoring. Setting the bits to 0s mutes the AOUT transmit path. 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB ... 0000_0000 = Mute
Note: Function available when DAA Register offset 0x31 bit 6 is set to 1 (MAP = 1).		

DAA Register Offset 0x46 Ring Validation Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDLY[1:0]		RMX[5:0]					
Type	R/W		R/W					

Reset settings = 1001_0110

Bit	Name	Function
7:6	RDLY[1:0]	**Ring Delay.** These bits, in combination with the RDLY[2] bit, set the amount of time between when a ring signal is validated and when a valid ring signal is indicated. RDLY[2] RDLY[1:0] Delay 0 00 0 ms 0 01 256 ms 0 10 512 ms ... 1 11 1792 ms
5:0	RMX[5:0]	**Ring Assertion Maximum Count.** These bits set the maximum ring frequency for a valid ring signal within a 10% margin of error. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. When a subsequent TIP/RING event occurs, the timer value is compared to the RMX[5:0] field, and, if it exceeds the value in RMX[5:0], the frequency of the ring is too high and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RMX[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $RMX[5:0] \geq RAS[5:0] - \frac{1}{2 \times f\_max \times 2\ ms}, RMX \leq RAS$ To compensate for error margin and ensure a sufficient ring detection window, it is recommended that the calculated value of RMX[5:0] be incremented by 1.

DAA Register Offset 0x47 Ring Validation Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDLY[2]	RTO[3:0]				RCC[2:0]		
Type	R/W	R/W				R/W		

Reset settings = 0010_1101

Bit	Name	Function
7	RDLY[2]	**Ring Delay Bit 2.** This bit, in combination with the RDLY[1:0] bits, sets the amount of time between when a ring signal is validated and when a valid ring signal is indicated. **RDLY[2] RDLY[1:0] Delay** 0 00 0 ms 0 01 256 ms 0 10 512 ms ... 1 11 1792 ms
6:3	RTO[3:0]	**Ring Timeout.** Determine when ringing is finished after the most recent ring threshold crossing. 0000 = Invalid 0001 = 128 x 1 = 128 ms 0010 = 128 x 2 = 256 ms ... 1111 = 128 x 15 = 1920 ms
2:0	RCC[2:0]	**Ring Confirmation Count.** Determine the time interval over which the ring signal must meet tolerances defined by RAS[5:0] and RMX[5:0] to be classified as a valid ring signal. 000 = 100 ms 001 = 150 ms 010 = 200 ms 011 = 256 ms 100 = 384 ms 101 = 512 ms 110 = 640 ms 111 = 1024 ms

DAA Register Offset 0x48 Ring Validation Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RNGV		RAS[5:0]					
Type	R/W		R/W					

Reset settings = 0001_1001

Bit	Name	Function
7	RNGV	**Ring Validation Enable.** 0 = Ring validation feature is disabled. 1 = Ring validation feature is enabled in normal operating mode and low-power mode.
6	Reserved	Read returns zero.
5:0	RAS[5:0]	**Ring Assertion Time.** These bits set the minimum ring frequency for a valid ring signal. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. If a second or subsequent TIP/RING event occurs after the timer has timed out then the frequency of the ring is too low and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RAS[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $$RAS[5:0] \geq \frac{1}{2 \times f\_min \times 2\ ms}$$

DAA Register Offset 0x49 Resistor Calibration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			RCALD					
Type	R/W							

Reset settings = 000x_xxxx

Bit	Name	Function
7:6	Reserved	Read returns zero.
5	RCALD	**Resistor calibration disable.** 0 = Internal resistor calibration enabled. 1 = Internal resistor calibration disabled.
4:0	Reserved	Read returns zero or one.

DAA Register Offset 0x4A DC Termination Control (MAP = 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCV[1:0]		MINI[1:0]				ILIM	DCR
Type	R/W		R/W				R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:6	DCV[1:0]	**TIP/RING Voltage Adjust.** Adjust the voltage on the DCT pin of the line-side device, which affects the TIP/RING voltage on the line. Low voltage countries should use a lower TIP/RING voltage. Raising the TIP/RING voltage improves signal headroom. **Si3018 settings:** **DCV[1:0] DCT Pin Voltage** 00 3.1 V 01 3.2 V 10 3.35 V 11 3.5 V **Si3011 and Si3017 settings:** **DCV[1:0] DCT Pin Voltage** XX 3.35 V
5:4	MINI[1:0]	**Minimum Operational Loop Current.** Adjusts the minimum loop current so the DAA can operate. Increasing the minimum operational loop current improves signal headroom at a lower TIP/RING voltage. **Si3018 settings:** **MINI[1:0] Min Loop Current** 00 10 mA 01 12 mA 10 14 mA 11 16 mA **Si3011 and Si3017 settings:** **MINI[1:0] Min Loop Current** XX 10 mA
3:2	Reserved	Read returns zero.
1	ILIM	**Current Limiting Enable.** **Si3018 and Si3011 settings:** 0 = Current limiting mode disabled. 1 = Current limiting mode enabled. Limits loop current to a maximum of 60 mA per the TBR21 standard. **Si3017 settings:** X = Current limiting mode disabled.
0	DCR	**DC Impedance Selection.** 0 = 50 W dc termination is selected. Use this mode for all standard applications. 1 = 800 Ω dc termination is selected.
Note: Function available when DAA Registers offset 0x31 bit 6 is set to 1 (MAP = 1).		

DAA Register Offset 0x4B Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_xxxx

Bit	Name	Function
7:0	Reserved	Read returns zero or one.

DAA Register Offset 0x4C Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

DAA Register Offset 0x4D Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

DAA Register Offset 0x4E Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

DAA Register Offset 0x4F DAA Control 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FOH[1:0]			OHS2			
Type	R/W				R/W			

Reset settings = 0010_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6:5	FOH[1:0]	**Fast Off-Hook Selection.** Determines the length of the off-hook counter. 00 = 512 ms 01 = 128 ms (default) 10 = 64 ms 11 = 8 ms
4	Reserved	Read returns zero.
3	OHS2	**On-Hook Speed 2.** **Si3018 settings:** This bit, in combination with the OHS bit and the SQ[1:0] bits on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS OHS2 SQ[1:0] Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec) **Si3011 and Si3017 settings:** **OHS OHS2 SQ[1:0] Mean On-Hook Speed** X X XX Less than 0.5 ms
2:0	Reserved	Read returns zero.

DAA Register Offset 0x5D Programmable Hybrid Register 1 (MAP = 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB1[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB1[7:0]	**Hybrid 1.** Programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the first tap in the four-tap filter. When this register is set to 0s, this filter stage does not effect on the hybrid response. Refer to “AN84: Digital Hybrid with the Si305x DAAs” for more information on selecting coefficients for the programmable hybrid.
Note: Function available when DAA Registers offset 0x31 bit 6 is set to 1 (MAP = 1).		

DAA Register Offset 0x5E Programmable Hybrid Register 2 (MAP = 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB2[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB2[7:0]	**Hybrid 2.** Programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the first tap in the four-tap filter. When this register is set to 0s, this filter stage does not effect on the hybrid response. Refer to “AN84: Digital Hybrid with the Si305x DAAs” for more information on selecting coefficients for the programmable hybrid.
Note: Function available when DAA Registers offset 0x31 bit 6 is set to 1 (MAP = 1).		

DAA Register Offset 0x5F Programmable Hybrid Register 3 (MAP = 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB3[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB3[7:0]	**Hybrid 3.** Programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the first tap in the four-tap filter. When this register is set to 0s, this filter stage does not effect on the hybrid response. Refer to “AN84: Digital Hybrid with the Si305x DAAs” for more information on selecting coefficients for the programmable hybrid.
Note: Function available when DAA Registers offset 0x31 bit 6 is set to 1 (MAP = 1).		

DAA Register Offset 0x60 Programmable Hybrid Register 4 (MAP = 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB4[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB4[7:0]	**Hybrid 4.** Programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the first tap in the four-tap filter. When this register is set to 0s, this filter stage has no effect on the hybrid response. Refer to “AN84: Digital Hybrid with the Si305x DAAs” for more information on selecting coefficients for the programmable hybrid.
Note: Function available when DAA Registers offset 0x31 bit 6 is set to 1 (MAP = 1).		

DAA Register Offset 0x61 Programmable Hybrid Register 5 (MAP = 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB5[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB5[7:0]	**Hybrid 5.** Programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the first tap in the four-tap filter. When this register is set to 0s, this filter stage does not effect on the hybrid response. Refer to “AN84: Digital Hybrid with the Si305x DAAs” for more information on selecting coefficients for the programmable hybrid.
Note: Function available when DAA Registers offset 0x31 bit 6 is set to 1 (MAP = 1).		

DAA Register Offset 0x62 Programmable Hybrid Register 6 (MAP = 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB6[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB6[7:0]	**Hybrid 6.** Programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the first tap in the four-tap filter. When this register is set to all 0s, this filter stage does not effect on the hybrid response. Refer to “AN84: Digital Hybrid with the Si305x DAAs” for more information on selecting coefficients for the programmable hybrid.
Note: Function available when DAA Registers offset 0x31 bit 6 is set to 1 (MAP = 1).		

DAA Register Offset 0x63 Programmable Hybrid Register 7 (MAP = 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB7[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB7[7:0]	**Hybrid 7.** Programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the first tap in the four-tap filter. When this register is set to all 0s, this filter stage does not effect on the hybrid response. Refer to “AN84: Digital Hybrid with the Si305x DAAs” for more information on selecting coefficients for the programmable hybrid.
Note: Function available when DAA Registers offset 0x31 bit 6 is set to 1 (MAP = 1).		

DAA Register Offset 0x64 Programmable Hybrid Register 8 (MAP = 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB8[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB8[7:0]	**Hybrid 8.** Programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the first tap in the four-tap filter. When this register is set to all 0s, this filter stage does not effect on the hybrid response. Refer to “AN84: Digital Hybrid with the Si305x DAAs” for more information on selecting coefficients for the programmable hybrid.
Note: Function available when DAA Registers offset 0x31 bit 6 is set to 1 (MAP = 1).		

DAA Register Offset 0x6B Spark Quenching Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	SQ1	0	SQ0	0	0	0	0
Type	R/W			R/W				

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Always write this bit to zero.
6, 4	SQ[1:0]	**Spark Quenching.** These bits, in combination with the OHS bit and the OHS2 bit, set the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **Si3018 settings:** **OHS** **OHS2** **SQ[1:0]** **Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec) **Si3011 and Si3017 settings:** **OHS** **OHS2** **SQ[1:0]** **Mean On-Hook Speed** X X XX Less than 0.5 ms
5	Reserved	Always write this bit to zero.
3:0	Reserved	Always write these bits to zero.

Pin Descriptions: Si3052

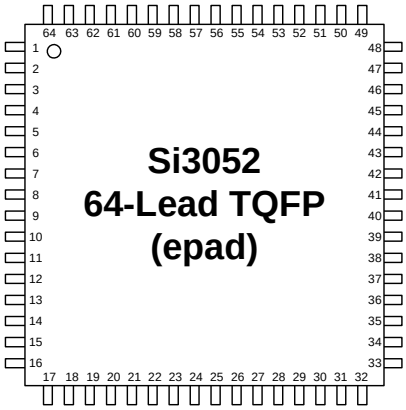


Table 24. Pin Descriptions

Pin #	Pin Name	Description
1	V_{IO}	**3.3/5 V IO Digital Supply Input.**
2	AD[17]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
3	AD[16]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
4	C/$\overline{BE}$[2]	**Command/Byte Enable Bit Input/Output.** Multiplexed command/byte enables for the PCI interface. The pin is an output during master operation and an input during slave operation. The pin indicates cycle type during the address phase and byte enable during the data phase of a transaction.
5	$\overline{FRAME}$	**Cycle Frame Indicator Input/Output.** PCI bus master output indicating the beginning and duration of a bus transfer.
6	$\overline{IRDY}$	**Initiator Ready Input/Output.** PCI bus master output indicating that the initiator device is ready to transmit or receive data.
7	$\overline{TRDY}$	**Target Ready Input/Output.** PCI bus target output indicating that the target device is ready to transmit or receive data.
8	$\overline{DEVSEL}$	**Device Select Input/Output.** PCI bus target output indicating the device has decoded the address of the current transaction that matches the target device's select range.
9	$\overline{STOP}$	**Stop Transaction Input/Output.** PCI bus target output indicating a request to the bus master to stop the current transaction.
10	$\overline{PERR}$	**Parity Error Input/Output.** Reports PCI bus data parity errors.

Table 24. Pin Descriptions (Continued)

Pin #	Pin Name	Description
11	$\overline{\text{SERR}}$	**System Error Input/Output.** Reports PCI bus system errors.
12	PAR	**Address/Data Parity Bit Input/Output.** Even parity across AD[31:0] and C/BE[3:0] for address and data bus phases. The parity is delayed one PCI clock cycle from the corresponding address or data bus phase.
13	C/$\overline{\text{BE}}$[1]	**Command/Byte Enable Bit Input/Output.** Multiplexed command/byte enables for the PCI interface. The pin is an output during master operation and an input during slave operation. The pin indicates cycle type during the address phase and byte enable during the data phase of a transaction.
14	AD[15]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
15	AD[14]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
16	V_{IO}	**3.3/5 V_{IO} Digital Supply Input.**
17	AD[13]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
18	AD[12]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
19	AD[11]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
20	AD[10]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
21	AD[09]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
22	AD[08]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
23	C/$\overline{\text{BE}}$[0]	**Command/Byte Enable Bit Input/Output.** Multiplexed command/byte enables for the PCI interface. The pin is an output during master operation and an input during slave operation. The pin indicates cycle type during the address phase and byte enable during the data phase of a transaction.
24	AD[07]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
25	V_{IO}	**3.3/5 V IO Digital Supply Input.**
26	AD[06]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.

Table 24. Pin Descriptions (Continued)

Pin #	Pin Name	Description
27	AD[05]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
28	AD[04]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
29	AD[03]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
30	AD[02]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
31	AD[01]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
32	AD[00]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
33	$\overline{\text{INTA}}$	**PCI Interrupt Output (Open Drain).** Level triggered interrupt pin for internal device interrupt sources.
34	3.3VAUX	**3.3 Vaux Sense Input.**
35	XOUT	**Crystal Output.** Connection to 16.384 MHz crystal.
36	XIN	**Crystal Input.** Connection to 16.384 MHz crystal.
37	$\overline{\text{RST}}$	**PCI Device Reset Input.** PCI bus master reset signal.
38	$\overline{\text{CLKRUN}}$/ PNPID/ EE_SD	**System Clock Control Input/Output (Open Drain).** An optional PCI signal defined for mobile applications. As an input, high indicates that PCICLK is active. The signal is driven low when the bus controller wants to stop PCI-CLK. As an output, low indicates a request to activate PCICLK. If unused, this pin requires a weak pulldown. **PCI PnP ID select Input.** Resistor selection for PCI Plug-n-Play (PnP) identification. **EPROM Serial Data Input/Output.** Serial data input/output to external PnP EPROM.
39	AOUT/ PNPID/ EE_SC	**Call Progress Monitor Output.** Pulse-Width Modulation (PWM) signal for driving a call progress speaker. **PCI PnP ID Select Input.** Resistor selection for PCI Plug-n-Play (PnP) Identification. **EPROM Serial Clock Output.** Serial clock output to external PnP EPROM.

Table 24. Pin Descriptions (Continued)

Pin #	Pin Name	Description
40	$\overline{\text{PME}}$	**Power Management Event Output (Open Drain).** Indicates a PCI power management event. This pin powers up in the high impedance state.
41	C2A	**Isolation Capacitor 2 A Input/Output.** Differential isolation for communication with the DAA line-side device.
42	C1A	**Isolation Capacitor 1 A Input/Output.** Differential isolation for communication with the DAA line-side device.
43	VA	**Voltage Regulator Bypass Output.**
44	VD	**3.3 V Digital Supply Input.**
45	PCICLK	**PCI Bus Clock Input.** PCI bus clock for all bus transaction timing. All synchronous signals are driven and sampled on the rising edge of this clock.
46	$\overline{\text{GNT}}$	**Master Grant Input.** Indicates that the system arbiter has granted PCI bus access.
47	$\overline{\text{REQ}}$	**Master Request Output (Tri-State).** Indicates a request to the system arbiter for access to the PCI bus. When $\overline{\text{RST}}$ is low, this pin is high-impedance.
48	AD[31]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
49	AD[30]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
50	AD[29]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
51	AD[28]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
52	AD[27]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
53	AD[26]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
54	AD[25]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
55	V_{IO}	**3.3/5 V ID Digital Supply Input.**
56	AD[24]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.

Table 24. Pin Descriptions (Continued)

Pin #	Pin Name	Description
57	C/$\overline{BE}$[3]	**Command/Byte Enable Bit Input/Output.** Multiplexed command/byte enables for the PCI interface. The pin is an output during master operation and an input during slave operation. The pin indicates cycle type during the address phase and byte enable during the data phase of a transaction.
58	IDSEL	**Initialize Device Select Input.** Chip select during PCI configuration register read/write cycles.
59	AD[23]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
60	AD[22]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
61	AD[21]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
62	AD[20]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
63	AD[19]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
64	AD[18]	**Address/Data Bit Input/Output.** Multiplexed address/data bit for the PCI interface.
epad	GND	**Exposed Die Paddle Ground.**

Pin Descriptions: Si3017/11/18

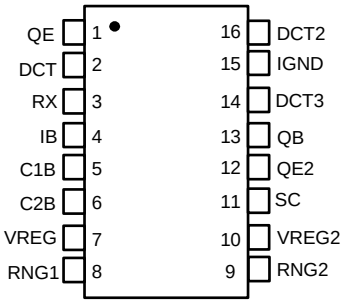


Table 25. Si3017/11/18 Pin Descriptions

Pin #	Pin Name	Description
1	QE	**Transistor Emitter.** Connects to the emitter of Q3.
2	DCT	**DC Termination.** Provides dc termination to the telephone network.
3	RX	**Receive Input.** Serves as the receive side input from the telephone network.
4	IB	**Internal Bias 1.** Provides internal bias.
5	C1B	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1 and communicates with the Si3052.
6	C2B	**Isolation Capacitor 2B.** Connects to one side of isolation capacitor C2 and communicate with the Si3052.
7	VREG	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
8	RNG1	**Ring 1.** Connects through a capacitor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si3052.
9	RNG2	**Ring 2.** Connects through a capacitor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si3052.
10	VREG2	**Voltage Regulator 2.** Connects to an external capacitor to provide bypassing for an internal power supply.
11	SC	**Circuit Enable.** Enables transistor network.
12	QE2	**Transistor Emitter 2.** Connects to the emitter of Q4.
13	QB	**Transistor Base.** Connects to the base of transistor Q3. Used to go on- and off-hook.
14	DCT3	**DC Termination 3.** Provides the dc termination to the telephone network.
15	IGND	**Isolated Ground.** Connects to ground on the line-side interface.
16	DCT2	**DC Termination 2.** Provides dc termination to the telephone network.

Ordering Guide

Region	Interface	System-Side		Line-Side		Temperature
		Part #	Package	Part #	Package	
FCC	PCI	Si3052-KQ	TQFP	Si3017-KS	SOIC	0 to 70 °C
TBR21	PCI	Si3052-KQ	TQFP	Si3011-KS	SOIC	0 to 70 °C
Global	PCI	Si3052-KQ	TQFP	Si3018-KS	SOIC	0 to 70 °C
Global	PCI	Si3052-KQ	TQFP	Si3018-KT	TSSOP	0 to 70 °C
Global	AC-Link	Si3054-KS	SOIC	Si3018-KS	SOIC	0 to 70 °C
Global	AC-Link	Si3054-KT	TSSOP	Si3018-KT	TSSOP	0 to 70 °C

Package Outline: 64-Pin TQFP

Figure 28 illustrates the package details for the Si3052. Table 26 lists the values for the dimensions shown in the illustration.

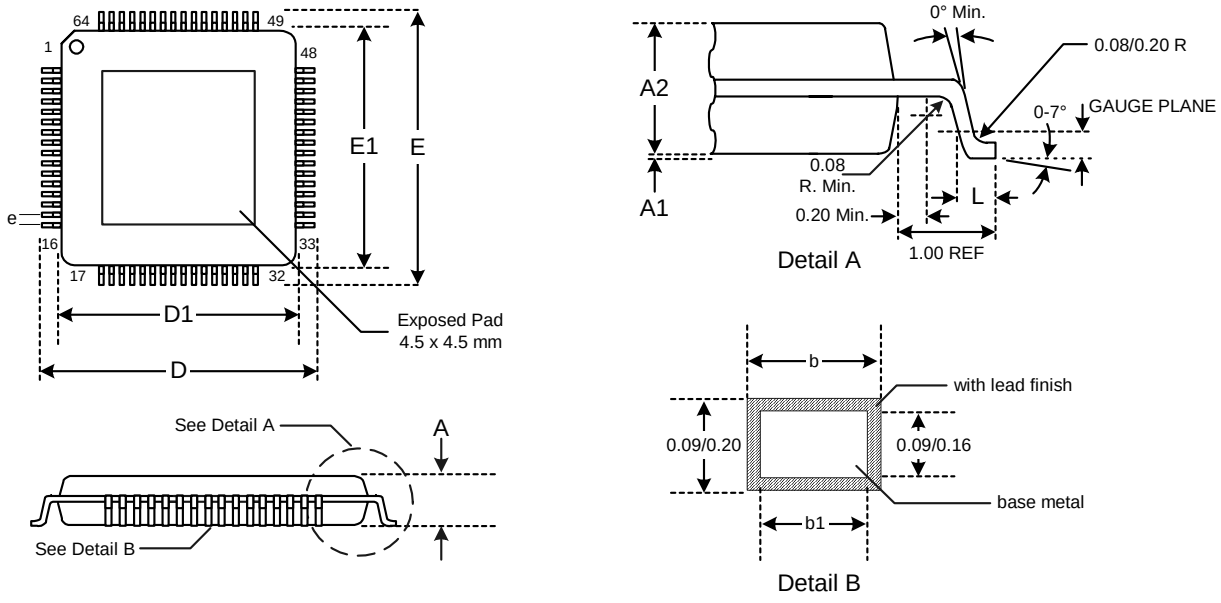


Figure 28. 64-Pin Thin Quad Flat Package (TQFP)

Table 26. 64-Pin Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
e	0.50 BSC		
b	0.17	0.22	0.27
b1	0.17	0.20	0.23

Package Outline: 16-Pin SOIC

Figure 29 illustrates the package details for the Si3017/11/18. Table 27 lists the values for the dimensions shown in the illustration.

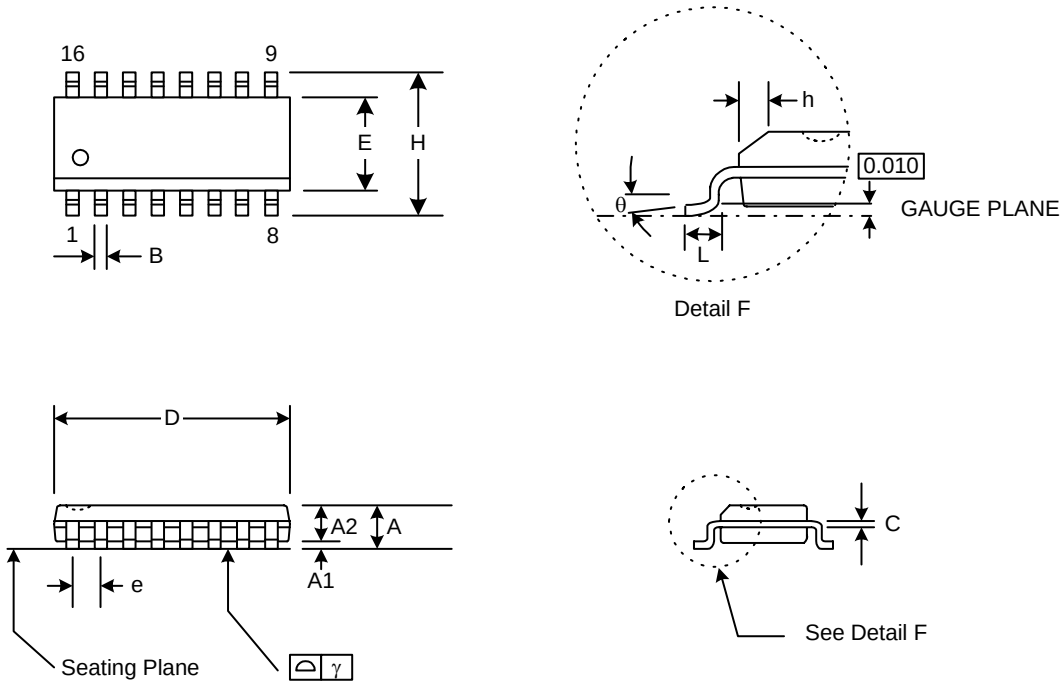


Figure 29. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 27. Package Diagram Dimensions

Symbol	Millimeters		Typical*
	Min	Max	
A	1.35	1.75	✓
A1	.10	.25	✓
A2	1.30	1.50	
B	.33	.51	
C	.19	.25	✓
D	9.80	10.01	
E	3.80	4.00	
e	1.27 BSC	—	
H	5.80	6.20	
h	.25	.50	
L	.40	1.27	
γ	—	0.10	
θ	0º	8º	✓

***Note:** Typical parameters are for information purposes only.

Document Change List

Revision 0.86 to Revision 1.0

- Si3017 descriptions added.
- Si3011 descriptions added.
- Table 2 on page 5 TBD values defined.
- Table 3 on page 6 TBD values defined.
- Figure 13 on page 16 updated.
- Figure 14 on page 17 updated.
- "Bill of Materials" on page 18 updated.
- Figure 14 on page 17 updated.
- Table 14 on page 28 updated.
- "Initialization" on page 30 updated.
- "Parallel Handset Detection" on page 30 updated.
- Table 15 on page 31 updated.
- "DC Termination" on page 32 updated.
- "Ring Detection" on page 33 updated.
- "DTMF Dialing" on page 34 updated.
- "Billing Tone Detection and Receive Overload" on page 35 updated.
- "On-Hook Line Monitor" on page 36 updated.
- "Overload Detection" on page 37 updated.
- "In-Circuit Testing" on page 38 updated.
- "Revision Identification" on page 38 updated.
- "Register Map" on page 38 updated.
- Table 19 and Table 20 added.
- Register descriptions updated.

Notes:

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