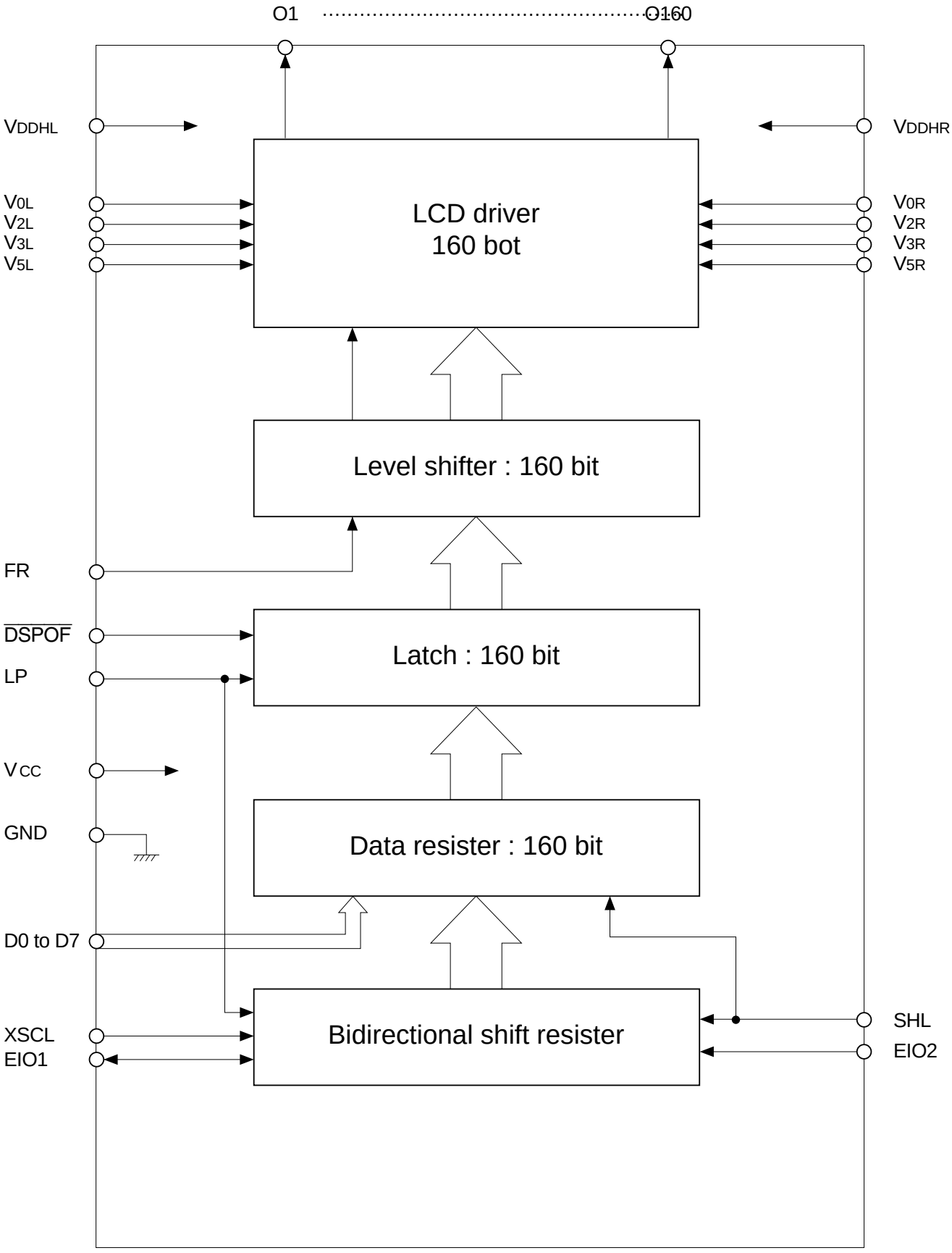
1. DESCRIPTION

S1D17508 is a 160 output segment (column) LCD driver suitable for driving of colored STN dot-matrix LCD panels of a larger capacity, for use in combination with S1D17043.
Contributing to making clearer LCD picture quality, this IC employs the high speed enable chain method and is slim-chip configuration which is more advantageous for miniaturization of the LCD panel. S1D17508 is also capable of low-voltage and high-speed logic operations and fits to a wide range of applications.

2. FEATURES

- Number of LCD drive output segments: 160
- Low voltage operation: 2.7V min.
- High duty drive: 1/500 (an example)
- Wide LCD drive voltage range: + 8 to + 42V (V_{DD} = 3 to 5.5V)
- High speed and low power consumption data transfer is possible by adoption of the 8-bit bus enable chain method:
  Shift clock frequencies: 18.0 MHz (5V ±10%)
  10.0 MHz (2.7V)
- Slim-chip configuration
- Non-bias display off function
- Pin-selection of the output shift direction is available
- Offset bias regulation of LCD power for respective V_{DDH} and GND levels is possible
- Logic operation power supply: 2.7 to 5.5V
- Shipped status: CHIP S1D17508D00B*
  TCP S1D17508T****
- This IC is not radiation resistant

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Numbers of pins</th></tr>
<tr><td>O1 to O160</td><td>O</td><td>LCD driving segment (column) output.
The output varies at the falling edge of LP.</td><td>160</td></tr>
<tr><td>D0 to D7</td><td>I</td><td>Display data input terminals</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>For input of the shift clock signals of the display data
(falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>For input of the latch pulse signals of the display data
(falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable I/O.
Setting to I or O is determined by the SHL input level.
The output is reset by the LP input and when 160 bit equivalent data are received, it falls to LOW automatically.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO terminal I/O control signal input.
When data are input to terminals (D_0, D_1 .....D_7) in the order of (a_0, a_1 .....a_6 and a_7), (b_0.....b_6 and b_7) .....(t_0, t_1.....t_6 and t_7), the relations between the data and segment outputs become as follows:
<table>
<tr><th rowspan="2">SHL</th><th colspan="8">Output</th><th colspan="2">EIO</th></tr>
<tr><th>O1</th><th>O2</th><th>O3</th><th></th><th>O158</th><th>O159</th><th>O160</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>LOW</td><td>a7</td><td>a6</td><td>a5</td><td>...</td><td>t2</td><td>t1</td><td>t0</td><td>Input</td><td>Output</td></tr>
<tr><td>HIGH</td><td>t0</td><td>t1</td><td>t2</td><td>...</td><td>a5</td><td>a6</td><td>a7</td><td>Output</td><td>Input</td></tr>
</table>
(Note) The relations between the data and segment outputs are determined independent from the number of the shift clocks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>For input of alternating current LCD drive signals.</td><td>1</td></tr>
<tr><td>V_{CC}, GND</td><td>Power supply</td><td>Logic operation power supply: GND: 0V
V_{CC}: +3.3, +5V</td><td>2</td></tr>
<tr><td>V_{DDHL}, V_{DDHR}
V_{0L},V_{0R}
V_{2L}, V_{2R}
V_{3L}, V_{3R}
V_{5L}, V_{5R}</td><td>Power supply</td><td>LCD drive power supply V_{DDH}
" V_0
" V_2
" V_3
" V_5
GND: 0V V_{DDH}:14 to 42V
$V_{DDH} \geq V_0 \geq V_2 \geq 7/9V_0$
$2/9\ V_0 \geq V_3 \geq V_5 \geq V_{SS}$</td><td>10</td></tr>
<tr><td>$\overline{DSPOF}$</td><td>I</td><td>For forced bias fixed input.
LOW level output is forcefully made to V_5 level.
* When using this function, combined use with S1D17003 is not applicable.</td><td>1</td></tr>
<tr><td colspan="3">Total</td><td>187</td></tr>
</table>

5. FUNCTION OF EACH BLOCK

5-1 Enable shift resister

The enable shift register is a bidirectional shift register of which the shift direction is being selected by the SHL input and the shift register output is used to store data bus signals into the data register.
When the enable signal is in disabled state, the internal clock signal and the data bus are fixed to LOW, thus going into a power saving mode.
When using multiple number of segment drivers, make cascade connection of EIO terminals of respective drivers to connect the EIO terminal of the top driver to "GND". (Refer to Clause 10. Connection examples)
Since the enable control circuit automatically senses completion of receiving 160 bit equivalent data to transfer the enable signal automatically, control signal of a separate control LSI is not needed.

5-2 Data register

This register works to make series or parallel conversion of data bus signals according to the enable shift register output. Consequently, the relations between the serial display data and segment outputs are determined independent from the number of the shift clock inputs.

5-3 Latch

It takes in the content of the data register at the falling edge trigger to transfer the output to the level shifter.

5-4 Level shifter

This is a level interface circuit to convert the voltage level of signals from the logic operation level to LCD drive level.

5-5 LCD driver

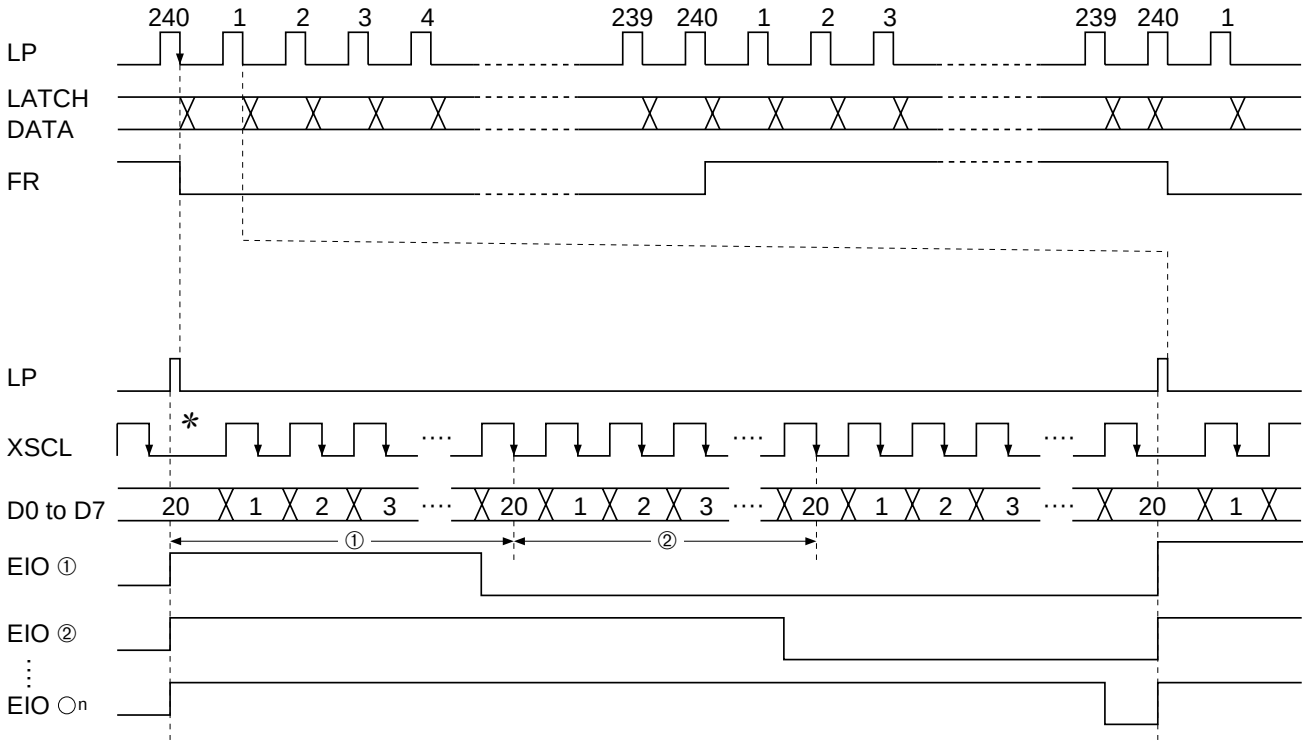
It outputs the LCD driving voltage.
Given below are the relations between data bus signals, alternating current signal FR levels and segment output voltages.

$\overline{\text{DSPOF}}$	Data bus signals	FR	Voltage outputs of the driver
HIGH	HIGH	HIGH	V_0
		LOW	V_5
	LOW	HIGH	V_2
		LOW	V_3
LOW	–	–	V_5

5-6 Timing diagram

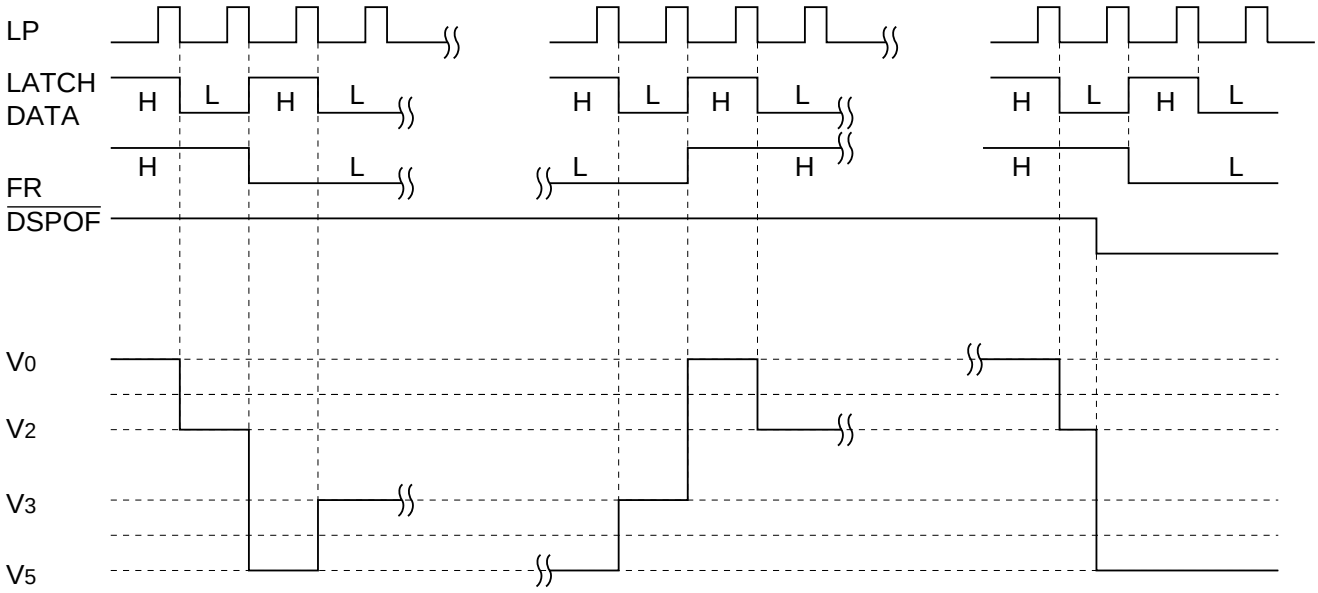
Timing diagram

In case of 1/240 Duty (an example)



① to ⓝ stands for the cascade numbers of the driver.

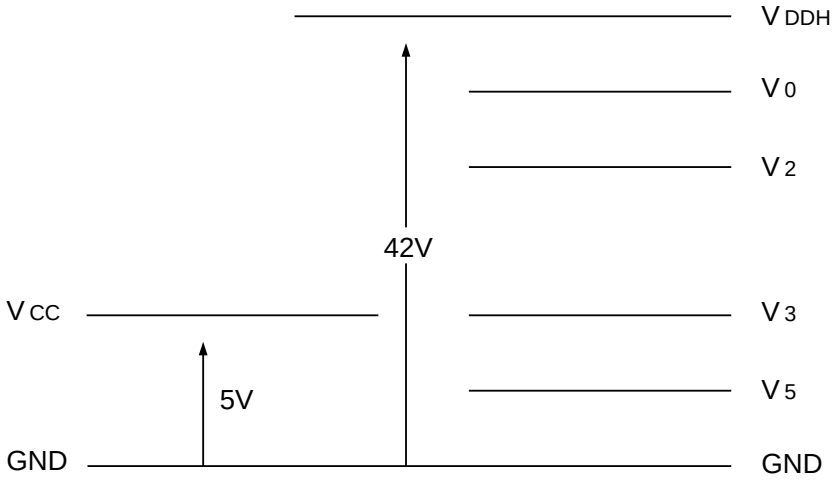
* When making high speed data transfer, it becomes necessary to secure a longer XSCL cycle when determining the LP pulse insertion timing in order to maintain the specified value of LP → XSCL (t_{LH}).



6. ABSOLUTE MAXIMUM RATINGS

Items	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_2, V_3, V_5	–0.3 to V_{DDH} + 0.3	V
Input voltage	V_I	–0.3 to V_{CC} + 0.3	V
Output voltage	V_O	–0.3 to V_{CC} + 0.3	V
EIO output current	I_{O1}	20	mA
Working temperature	Topr	–30 to +85	°C
Storage temperature 1	Tstg1	–65 to +150	°C
Storage temperature 2	Tstg2	–55 to +100	°C

(Note 1) All the voltage ratings are based on GND = 0V.
(Note 2) The storage temperature 1 is applicable to independent chips and the storage temperature 2 is applicable to the TCP modular state.
(Note 3) V_0, V_2, V_3 and V_5 should always be in the order of $V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq GND$.



(Note 4) If the logic operation power goes into a floating state or if V_{CC} drops to 2.6V or below while the LCD driving power is being applied, the LSI may be damaged. Therefore, keep from occurrence of the aforementioned status.
Specifically, pay close attention to the power supply sequence at times of turning the system power on and off.

7. ELECTRICAL CHARACTERISTICS

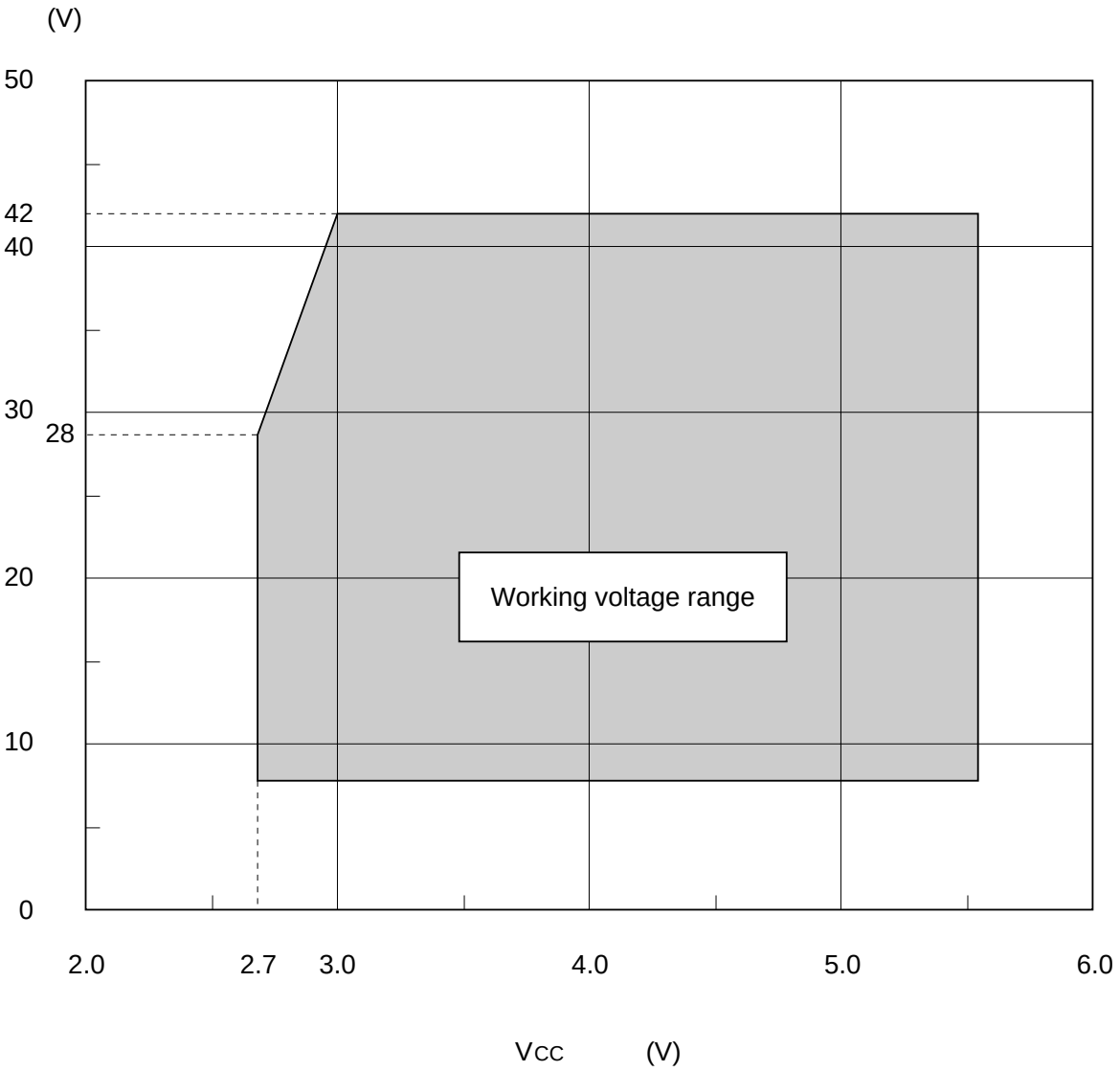
7-1 DC characteristics

Unless otherwise specified, GND = 0V, V_{CC} = +5.0 V ±10%, Ta = –30 to 85°C

Item	Symbol	Condition		Applicable pin	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{CC}			V_{CC}	2.7		5.5	V
Recommended operating voltage	V_0			V_{0L},V_{DDHL} V_{0R},V_{DDHL}	14.0		40.0	V
Operating voltage	V_0	Function only			8.0		42.0	V
Supply voltage (2)	V_2	Recommended value		V_{2L}, V_{2R}	7/9 V_0		V_0	V
Supply voltage (3)	V_3	Recommended value		V_{3L}, V_{3R}	GND		2/9 V_0	V
High level input voltage	V_{IH}	V_{DD} = 2.7 to 5.5V		EIO1,EIO2,FR D0 to D7,XSCL SHL,LP,$\overline{DSPOF}$	0.8V_{CC}			V
Low level input voltage	V_{IL}						0.2V_{CC}	V
High level output voltage	V_{OH}	V_{CC}= 2.7 to 5.5V	I_{OH} = –0.6mA	EIO1, EIO2	V_{CC}–0.4			V
Low level output voltage	V_{OL}		I_{OL} = 0.6mA				0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		D0 to D7,LP,FR XSCL, SHL $\overline{DSPOF}$			2.0	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		EIO1, EIO2			5.0	µA
Rest current	I_{GND}	V_0 = 14.0 to 42.0V V_{IH} = V_{CC}, V_{IL}=GND		GND			25	µA
Output resistance	R_{SEG}	△V_{ON} =0.5V Recom-mended condition	V_0 =+36.0V, 1/24	O1 to O160		0.85	2.6	kΩ
			V_0 =+26.0V, 1/20			0.90	2.6	
In-chip deviation of output resistance	△R_{SEG}	△V_{ON}=0.5V V_0 = +36.0V, 1/24		O1 to O160			90	Ω
Mean working current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC} V_{IL} = GND, f_{XSCL} = 5.38MHz f_{LP} = 33.6kHz, f_{FR} = 70Hz Input data: Checkered indication, no-load		V_{CC}		0.5	1.1	mA
		V_{CC} = +3.0V Other conditions are the same as those when V_{CC} = 5V.				0.2	0.6	
Mean working current consumption (2)	I_O	V_0 = +30.0V V_{CC} = +5.0V, V_3 = +4.0V V_2 = +26.0V, V_5 = +0.0V Other conditions are the same as those in the I_{DD} column.		V0L, V0R		0.15	0.9	mA
Input terminal capacity	C_I	Freq. = 1 MHz Ta = 25°C Independent chips		D0 to D7, LP, FR, XSCL, SHL, $\overline{DSPOF}$			8	pF
I/O terminal capacity	$C_{I/O}$			EIO1, EIO2			15	pF

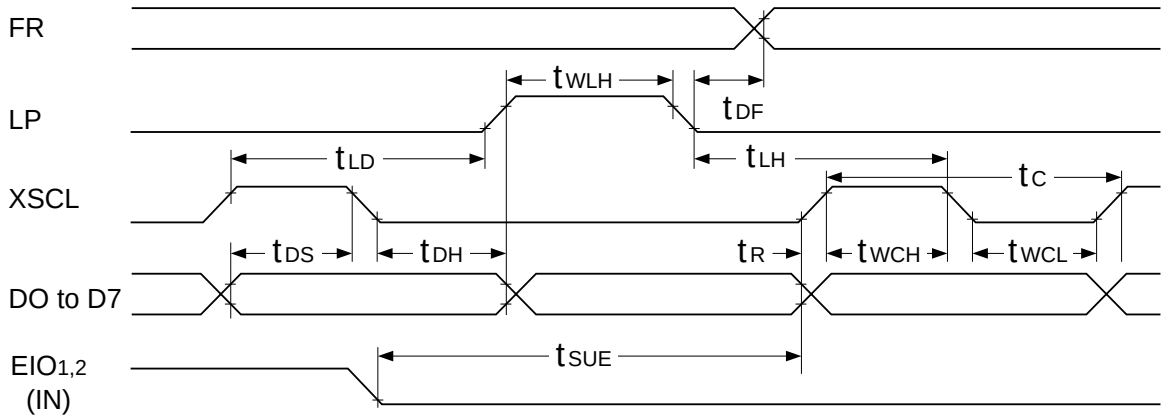
Working voltage range V_{CC} - V_0

The V_0 voltage should be set up within the V_{CC} - V_0 working voltage range given below.



7-2 AC characteristics

Input timing characteristics



V_{CC} = 5.0V ±10%, Ta = –30 to 85°C

Items	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	tc	tr, tf≤11ns *3	62		ns
XSCL high level pulse duration	tWCH		20		ns
XSCL low level pulse duration	tWCL		20		ns
Data setup time	tDS		10		ns
Data hold time	tDH		10		ns
XSCL → LP rise time	tLD		–5		ns
LP → XSCL fall time	tLH		30		ns
LP high level pulse duration	tWLH	*1	40		ns
		*2	35		ns
FR delay allowance	tDF		–300	+300	ns
EIO setup time	tSUE		30		ns
Input signal variation time	tr, tf	*4		50	ns

V_{CC} = 2.7V to 4.5V, Ta = –30 to 85°C

Items	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	tc	tr, tf≤15ns *3	100		ns
XSCL high level pulse duration	tWCH		35		ns
XSCL low level pulse duration	tWCL		35		ns
Data setup time	tDS		15		ns
Data hold time	tDH		10		ns
XSCL → LP rise time	tLD		–10		ns
LP → XSCL fall time	tLH		60		ns
LP high level pulse duration	tWLH	*1	75		ns
		*2	65		ns
FR delay allowance	tDF		–300	+300	ns
EIO setup time	tSUE		40		ns
Input signal variation time	tr, tf	*4		50	ns

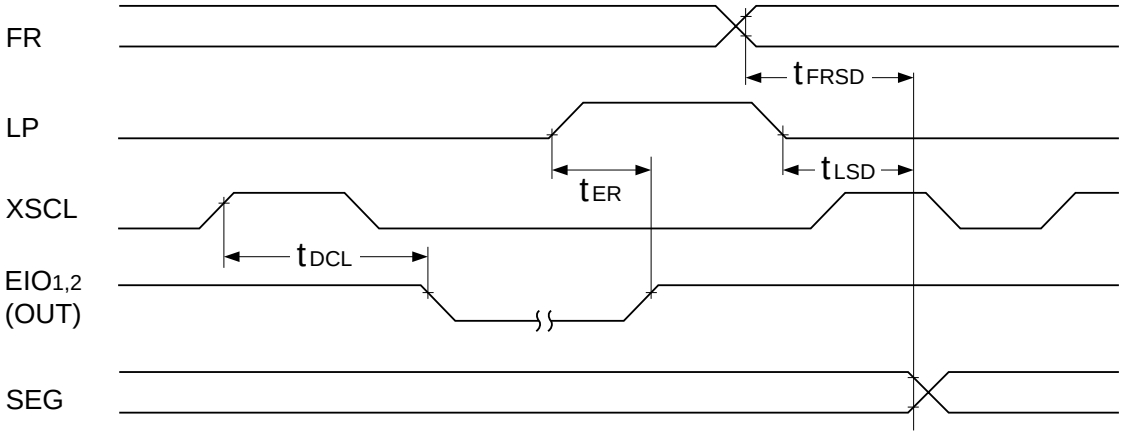
Notes: *1 The "t_{WLH}" specifies the time when the LP is at HIGH and, at the same time, when XSCL is at LOW, when LP is being input while the XSCL is at LOW.

* 2 The "t_{WLH}" (its definition is same as *1) when LP rises while XSCL is at HIGH.

* 3 High speed operation of the shift clocks (XSCL) should only be made under a condition of $t_r + t_f \leq (t_C - t_{WCL} - t_{WCH})$.

* 4 When making high speed data transfer using continuous shift clocks, $t_r + t_f$ of the LP signals should be upto $(t_C + t_{WCH} - t_{LD} - t_{WLH} - t_{LH})$ at the maximum.

Output timing characteristics



V_{CC} = +5.0V ±10%, V_0 = +14.0 to +42.0V

Items	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	CL = 15 pF (EIO)		120	ns
EIO output delay time	t_{DCL}			55	ns
LP → SEG output delay time	t_{LSD}	CL = 100 pF (O n)		200	ns
FR → SEG output delay time	t_{FRSD}			400	ns

V_{CC} = +2.7V to 4.5V, V_0 = +14.0 to +28.0V

Items	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	CL = 15 pF (EIO)		240	ns
EIO output delay time	t_{DCL}			85	ns
LP → SEG output delay time	t_{LSD}	CL = 100 pF (O n)		400	ns
FR → SEG output delay time	t_{FRSD}			800	ns

8. LCD DRIVING POWER SUPPLY

8-1 Setting up respective voltage levels

When setting up respective voltage levels for LCD drive, it is the best way to resistively divide the potential between V_0 - GND to drive the LCD by means of voltage follower using an operation amplifier.
In consideration of the case of using an operation amplifier, the LCD driving minimum potential level V_5 and GND are separated and independent terminals are used.
However, since the efficacy of the LCD driving output driver deteriorates when the potential of V_5 goes up beyond the GND potential to enlarge the potential difference, always keep the potential difference of V_5 - V_{SS} at 0V to 2.5V.
When a resistance exists in series in the power supply line of V_0 (GND), Io at signal changes causes voltage drop at V_0 (GND) of the supply terminals of the LSI disabling it to maintain the relations of the LCD with intermediate potentials of ($V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq$ GND), thus leading to breakdown or destruction of the LSI.
When using a protective resistor, do not fail to stabilize the voltage using an appropriate capacitance.

8-2 Precautions when turning the power on and off

Since the LCD drive voltage of these LSIs is comparatively high, if a high voltage of 30V or more is applied to the LCD drive circuit with the logic operation power made floating or with the V_{CC} lowered to 2.6V or less, or when LCD drive signals are output before applied voltage to the LCD drive circuits is stabilized, excess current flows through to possibly lead to breakdown or to destroy the LSI.
It is therefore suggested to maintain the potential of the LCD drive output to V_5 level until the LCD drive circuit voltage is stabilized, using the display off function ($\overline{DSPOF}$).
Maintain the following sequences when turning the power on and off:

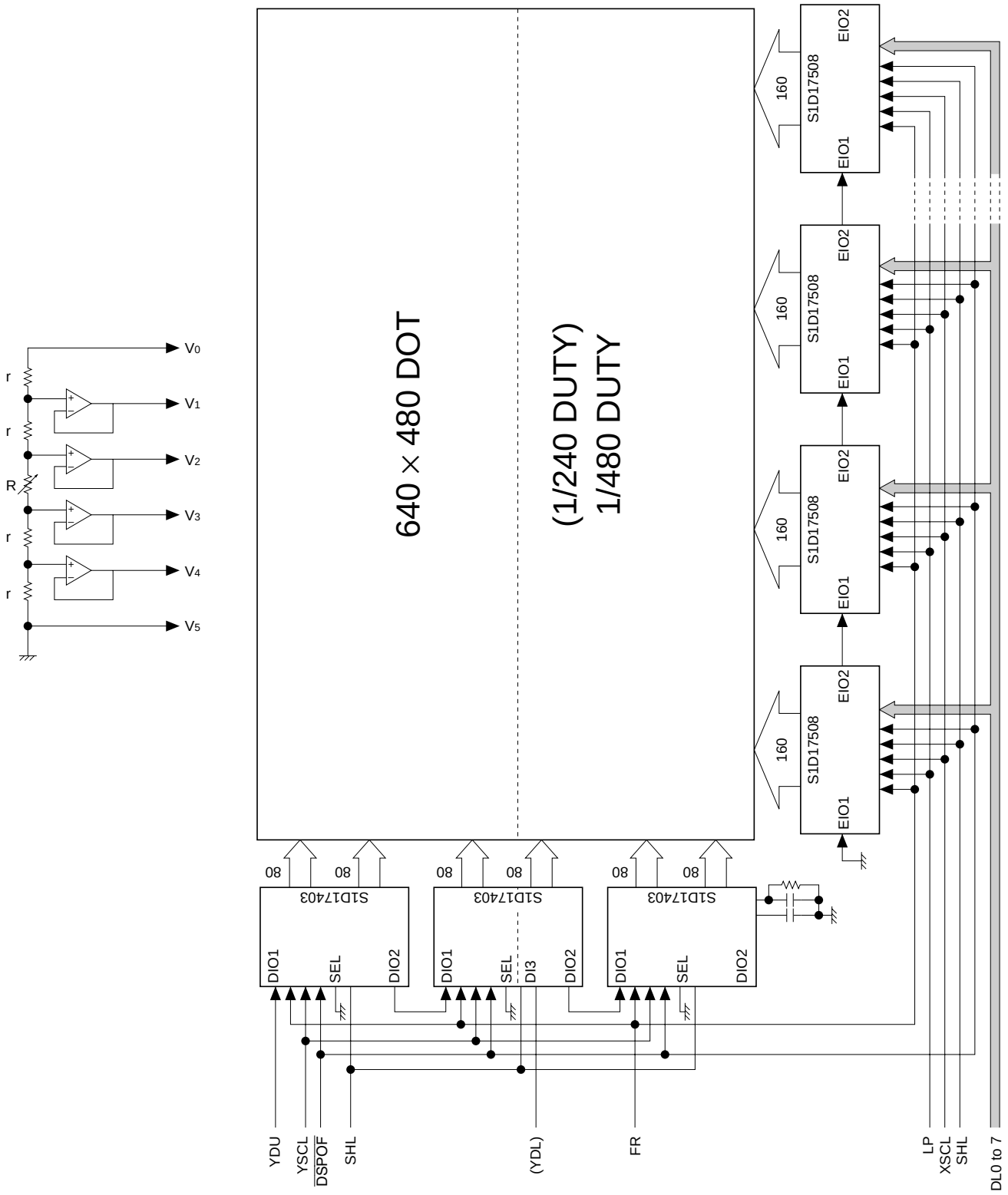
When turning the power on: Turn on the logic operation power → turn on the LCD drive power or turn them on simultaneously.

When turning the power off: Turn off the LCD drive power → turn off the logic operation power or turn them off simultaneously.

For protection against excess current, insert a quick melting fuse in series in the LCD drive power line.
When using a protective resistor, select the optimum resistance value depending on the capacitance of the LCD cells.

9. A CONNECTION EXAMPLE

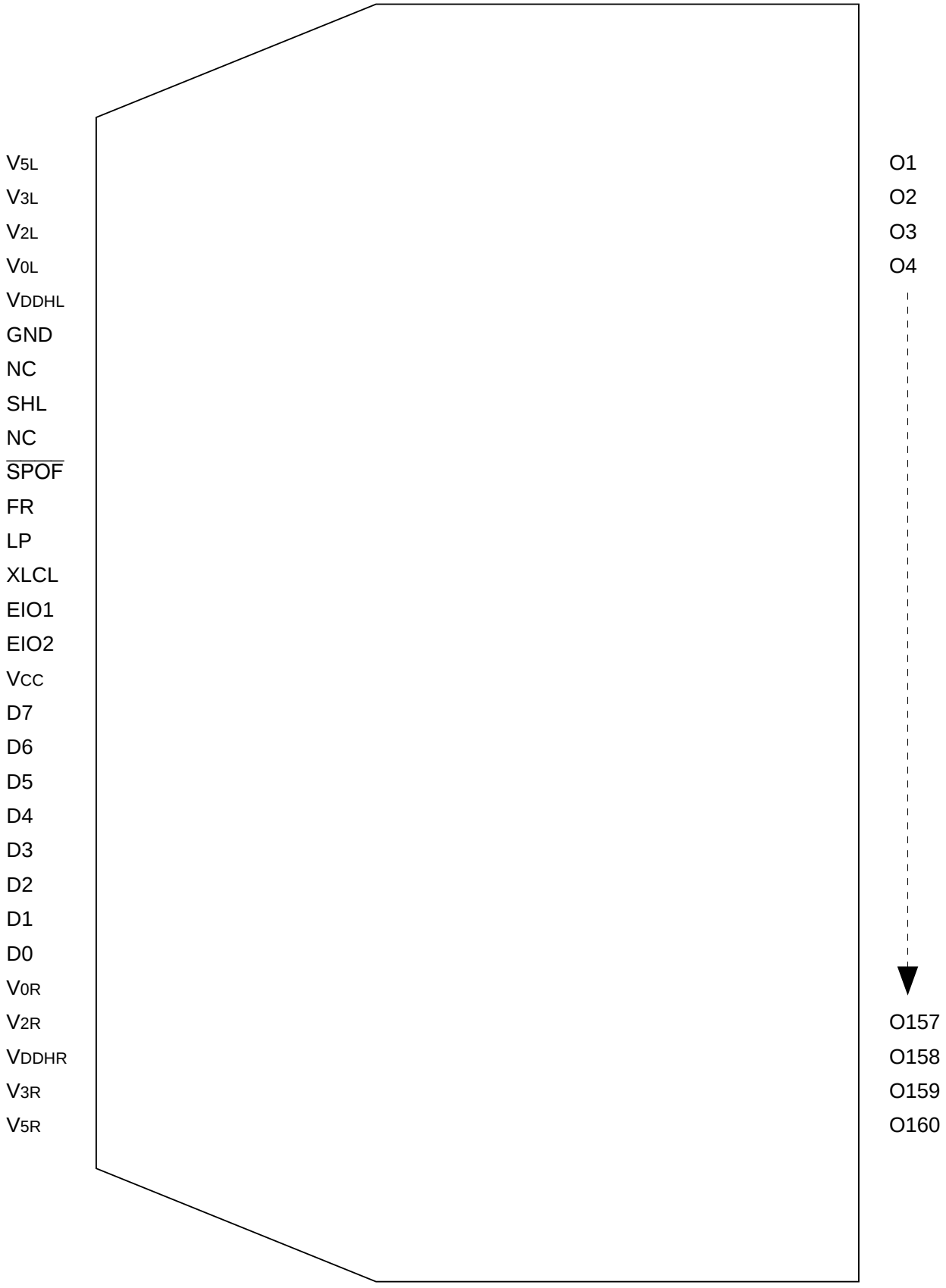
Block diagram of a large-plane LCD



10. S1D17508T* TCP PIN ARRANGEMENT EXAMPLE

For reference

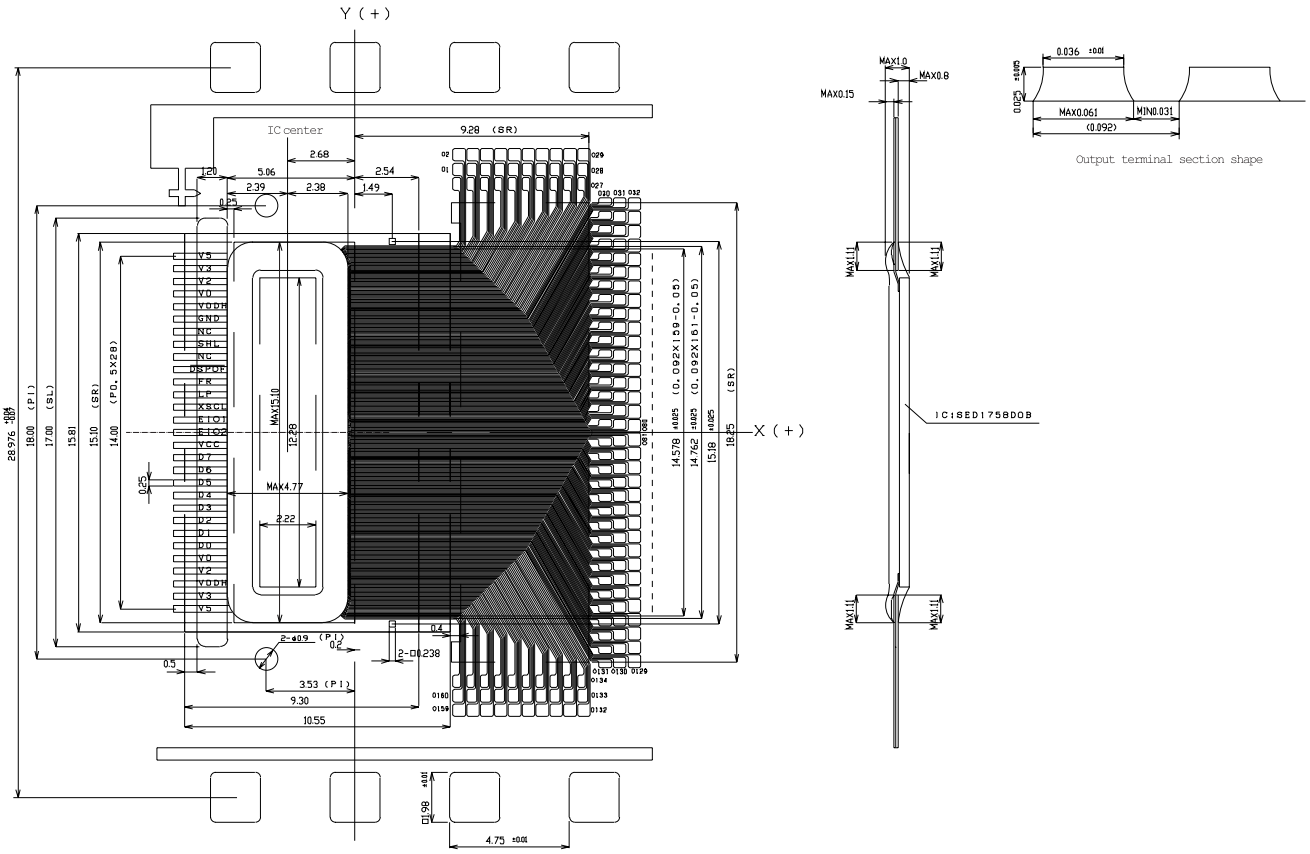
Remark: This drawing is not meant to determine the contour of the TCP.



11. DIMENSIONAL OUTLINE DRAWING

S1D17508T00A*

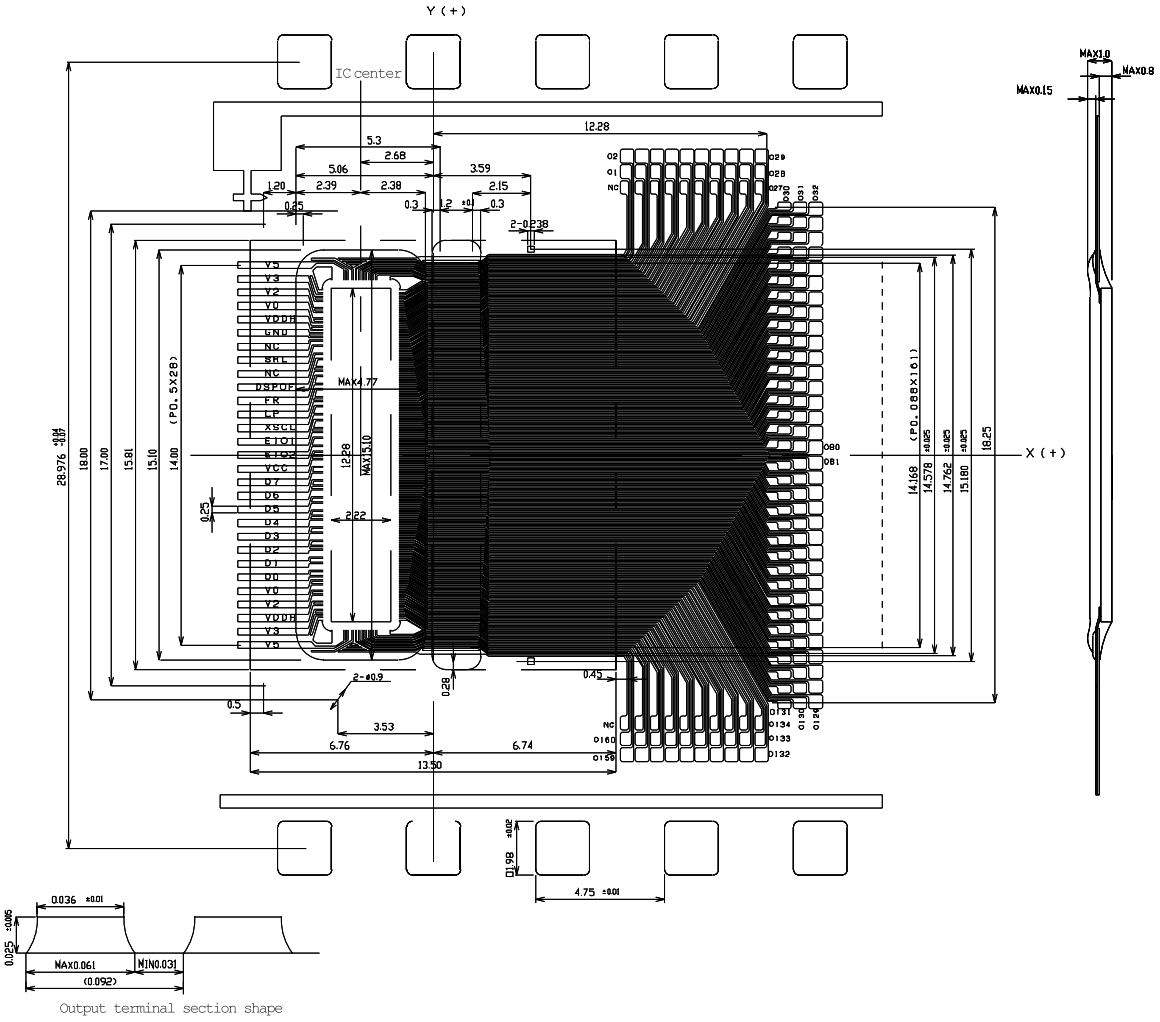
For reference



Unit: mm

For reference

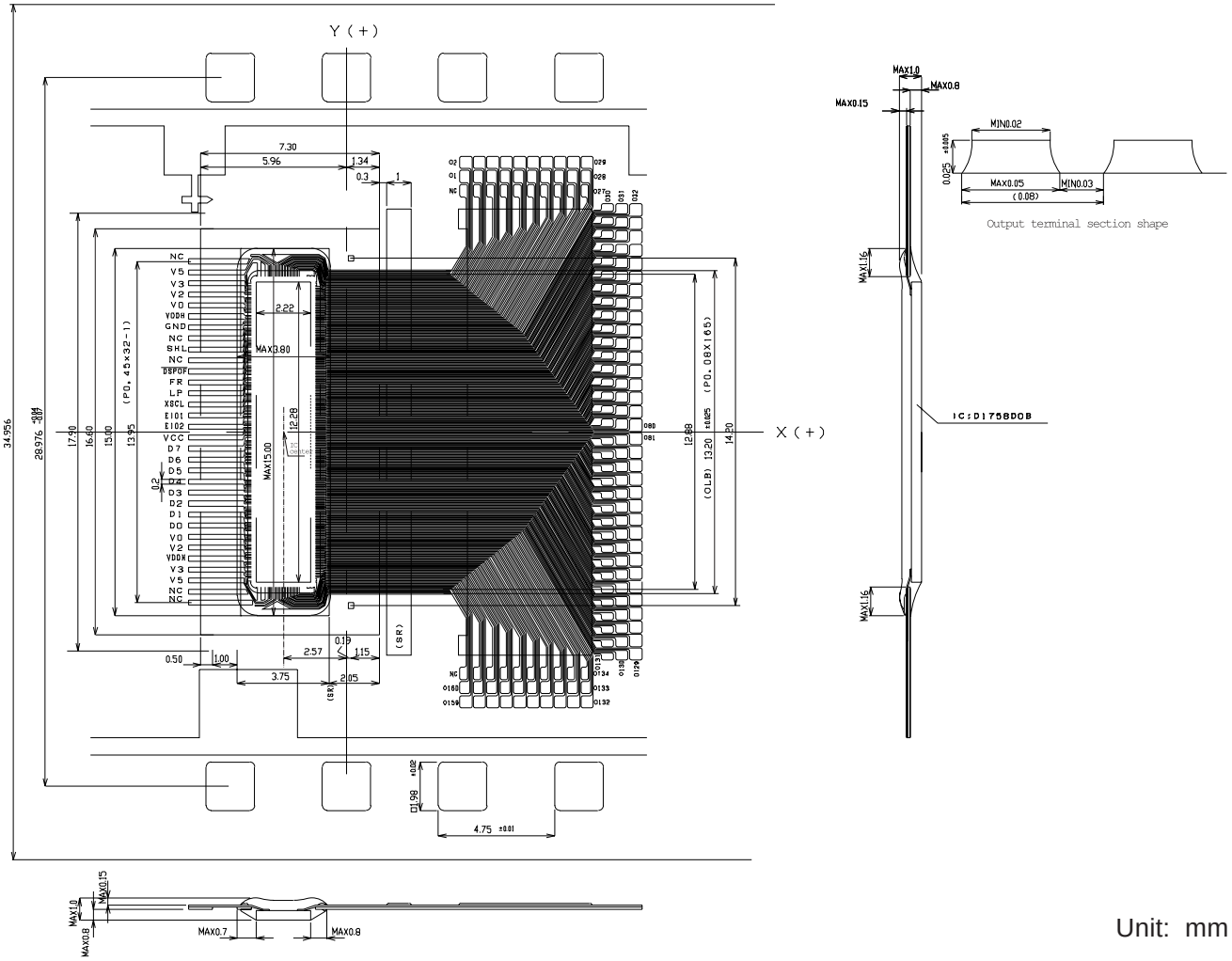
S1D17508T00B*



Unit: mm

For reference

S1D17508T00G*



Unit: mm