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DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

μPD78C10A(A), 78C11A(A), 78C12A(A)

8-BIT SINGLE-CHIP MICROCOMPUTER (WITH A/D CONVERTER)

Phase-out/Discontinued

DESCRIPTION

The μPD78C11A(A) is a CMOS 8-bit microcomputer that features single-chip integration of a 16-bit ALU, ROM, RAM, an A/D converter, a multifunctional timer/event counter, and a universal serial interface, as well as up to 60 Kbytes of expandable external memory (ROM/RAM). The μPD78C10A(A) is the ROMless version of the μPD78C11A(A) which can directly address up to 64 Kbytes of external memory. The μPD78C12A(A) is a version of the μPD78C11A(A) that has greater on-chip ROM capacity and is expandable to up to 56 Kbytes of external memory (ROM/RAM). The μPD78C10A(A), μPD78C11A(A), and μPD78C12A(A) all use CMOS technology to enable low-power operation and they also feature standby functions to enable data retention and other operations using very low power consumption.

In addition, the μPD78CP14(A) and 78CP18(A) are available as on-chip PROM versions appropriate for evaluating and prototyping during system development as well as for early development of application sets and low-volume production.

Detailed functional descriptions are provided in the following User's Manual. This manual is required reading for design work.

87AD Series μPD78C18 User's Manual: IEU-1314

FEATURES

- Higher reliability than μPD78C10A, 78C11A, or 78C12A
- 159 instructions: the 87AD Series instruction set with multiply and divide instructions and 16-bit arithmetic instructions
- 0.8 μs instruction cycle time (15-MHz operation)
- On-chip ROM: 4096-W x 8 (μPD78C11A(A)), 8192-W x 8 (μPD78C12A(A)), or none (μPD78C10A(A))
- On-chip RAM: 256-W x 8
- High-precision 8-bit A/D converter: 8 analog inputs
- Universal serial interface: asynchronous, synchronous, and I/O interface modes
- Multifunctional 16-bit timer/event counter
- Two 8-bit timers
- I/O lines: 32 in μPD78C10A(A) and 44 in μPD78C11A(A) or 78C12A(A)
- Interrupt functions (3 external, 8 internal): 1 nonmaskable interrupt and 10 maskable interrupts
- Standby functions: HALT mode and hardware/software STOP mode
- Zero-cross detection function: 2 inputs
- On-chip mask optional pull-up resistors are available (for ports A, B, and C on μPD78C11A(A) or 78C12A(A) only)

Caution Mask options are not available on the μPD78C10A(A).

The information in this document is subject to change without notice.

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Date Published May 1995 P
Printed in Japan

The mark ★ shows revised points.

ORDERING INFORMATION

Part No.	Package	On-chip ROM
μPD78C10AGF(A)-3BE	64-pin plastic QFP (14 x 20 mm)	None
μPD78C10AGQ(A)-36	64-pin plastic QUIP	None
μPD78C10AL(A)	68-pin plastic QFJ (950 x 950 mil)	None
μPD78C11AGF(A)-xxx-3BE	64-pin plastic QFP (14 x 20 mm)	Mask ROM
μPD78C11AGQ(A)-xxx-36	64-pin plastic QUIP	Mask ROM
μPD78C11AL(A)-xxx	68-pin plastic QFJ (950 x 950 mil)	Mask ROM
μPD78C12AGF(A)-xxx-3BE	64-pin plastic QFP (14 x 20 mm)	Mask ROM
μPD78C12AGQ(A)-xxx-36	64-pin plastic QUIP	Mask ROM
μPD78C12AL(A)-xxx	68-pin plastic QFJ (950 x 950 mil)	Mask ROM

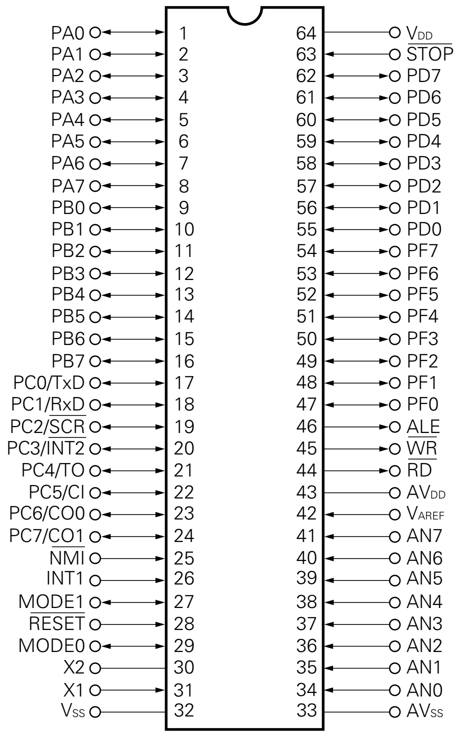
Quality Grade

Special (for high-reliability electronic devices)

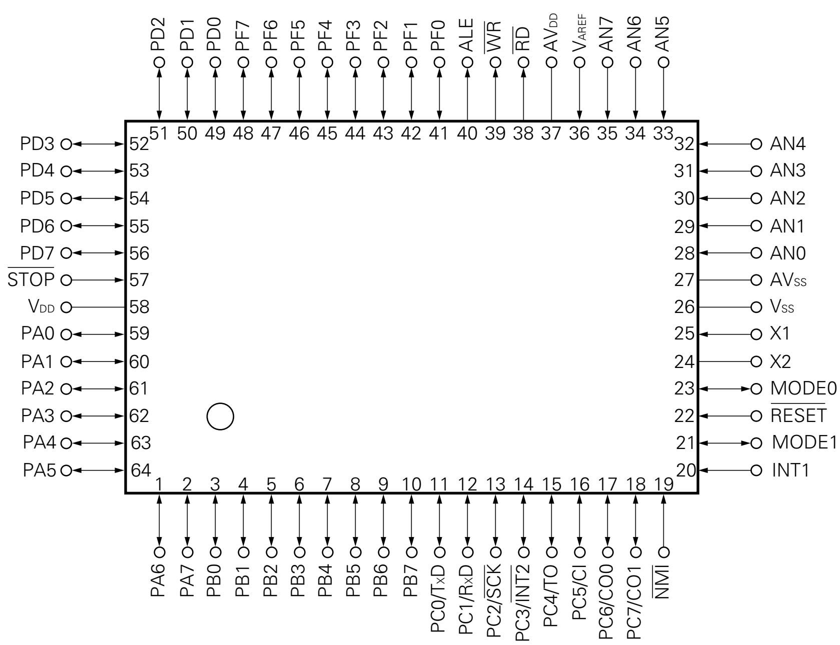
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATION (Top View)

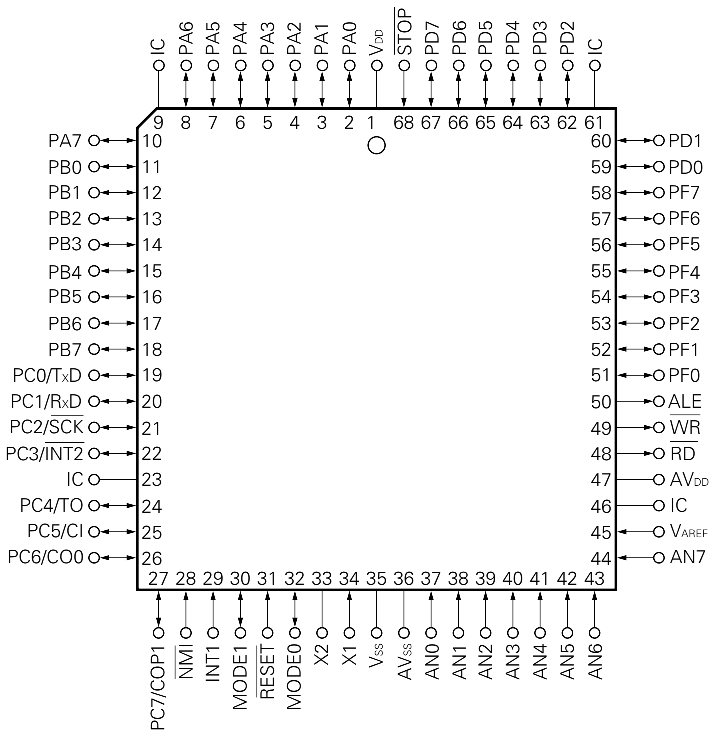
- μPD78C10AGQ(A)-36, 78C11AGQ(A)-xxx-36, or 78C12AGQ(A)-xxx-36



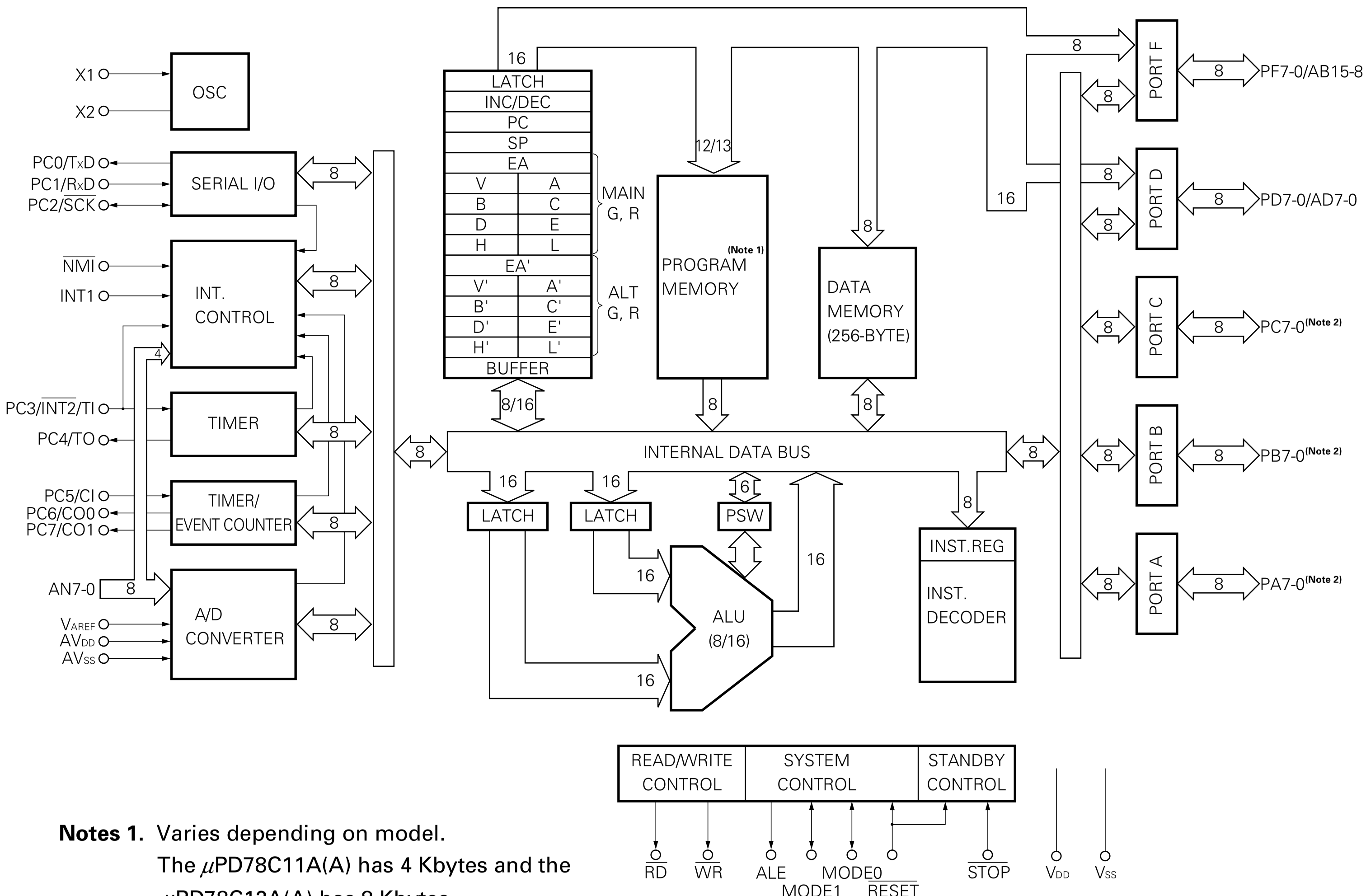
- μPD78C10AGF(A)-3BE, 78C11AGF(A)-xxx-3BE, or 78C12AGF(A)-xxx-3BE



• μPD78C10AL(A), 78C11AL(A)-xxx, or 78C12AL(A)-xxx



Block Diagram



Notes 1. Varies depending on model.
The μPD78C11A(A) has 4 Kbytes and the μPD78C12A(A) has 8 Kbytes.
The μPD78C10A(A) does not have any program memory.

2. On-chip mask optional pull-up resistors are available (μPD78C11A(A) or 78C12A(A) only).

Differences between (1) μPD78C10A(A), 78C11A(A), and 78C12A(A) and (2) μPD78C10A, 78C11A, and 78C12A

Part / Category	μPD78C10A(A), 78C11A(A), 78C12A(A)	μPD78C10A, 78C11A, 78C12A
Quality grade	Special (for high-reliability electronic equipment)	Standard (for ordinary electronic equipment)
Electrical specifications	Input leakage current AN0 to AN7, ±1 μA (max)	Input leakage current AN0 to AN7, ±10 μA (max)
Packages	• 64-pin plastic QFP (14 x 20 mm) • 64-pin plastic QUIP • 68-pin plastic QFJ (950 x 950 mil)	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QUIP • 64-pin plastic QUIP straight (Note) • 64-pin plastic QFP (14 x 20 mm) • 68-pin plastic QFJ (950 x 950 mil)

Note μPD78C11A and 78C12A only

CONTENTS

1. PIN FUNCTIONS

1.1 Pin Function List

<table>
<tr><th>Pin name</th><th>I/O</th><th colspan="2">Function</th></tr>
<tr><td>PA7-0
(Port A)</td><td>I/O</td><td colspan="2">Port A is an 8-bit I/O port for which the input or output mode can be specified bit-wise.</td></tr>
<tr><td>PB7-0
(Port B)</td><td>I/O</td><td colspan="2">Port B is an 8-bit I/O port for which the input or output mode can be specified bit-wise.</td></tr>
<tr><td>PC0/TxD</td><td>I/O or O</td><td rowspan="7">Port C
When used as port C, it is an 8-bit I/O port for which the input or output mode can be specified bit-wise.</td><td>Transmit Data
When used for transmit data output, it is a serial data output pin.</td></tr>
<tr><td>PC1/RxD</td><td>I/O or I</td><td>Receive Data
When used for receive data input, it is a serial data input pin.</td></tr>
<tr><td>PC2/$\overline{SCK}$</td><td>I/O or I/O</td><td>Serial Clock
When used for serial clock I/O, it is an output pin for the internal clock or an input pin for an external clock.</td></tr>
<tr><td>PC3/$\overline{INT2}$/TI</td><td>I/O or I or I</td><td>Interrupt Request/Timer Input
When used for interrupt request or timer input, it is a falling-edge triggered maskable interrupt input pin, or a timer input pin for external clock input, or an AC-input, zero-cross detection pin.</td></tr>
<tr><td>PC4/TO</td><td>I/O or O</td><td>Timer Output
When used for timer output, it outputs a square wave having a count time of one-half cycle per internal clock cycle.</td></tr>
<tr><td>PC5/CI</td><td>I/O or I</td><td>Counter Input
When used for counter input, it is an input pin for external pulses to the timer/event counter.</td></tr>
<tr><td>PC6/CO0
PC7/CO1</td><td>I/O or O</td><td>Counter Output0, 1
When used for counter outputs 0 and 1, these pins output a programmable square wave from the timer/event counter.</td></tr>
<tr><td>PD7-0/AD7-0</td><td>I/O or I/O</td><td>Port D
When used as Port D, it is an 8-bit I/O port for which the input or output mode can be specified byte-wise (μPD78C11A(A)).</td><td>Address/Data Bus
When using external memory, it acts as a multiplexed address/data bus.</td></tr>
<tr><td>PF7-0/AB15-8</td><td>I/O or O</td><td>Port F
When used as Port F, it is an 8-bit I/O port for which the input or output mode can be specified bit-wise.</td><td>Address Bus
When using external memory, it acts as an address bus.</td></tr>
<tr><td>$\overline{WR}$
(Write Strobe)</td><td>O</td><td colspan="2">This is a strobe signal that is output for external memory write operations. It goes high except during the external memory's data write cycle. Output has high impedance when the $\overline{RESET}$ signal is low or during hardware STOP mode.</td></tr>
<tr><td>$\overline{RD}$
(Read Strobe)</td><td>O</td><td colspan="2">This is a strobe signal that is output for external memory read operations. It goes high except during the external memory's data read cycle. Output has high impedance when the $\overline{RESET}$ signal is low or during hardware STOP mode.</td></tr>
<tr><td>ALE
(Address Latch Enable)</td><td>O</td><td colspan="2">A strobe signal is used to externally latch the low-order address data output to PD0 to PD7 for external memory access. Output has high impedance when the $\overline{RESET}$ signal is low or during hardware STOP mode.</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th></tr>
<tr><td>MODE0
MODE1
(Mode)</td><td>I/O</td><td>In the μPD78C11A(A) and 78C12A(A), the MODE0 pin is set to “0” (low) and the MODE1 pin is set to “1” (high)(Note).
In the μPD78C10A(A), the MODE0 and MODE1 pins are used to select one of three external memory sizes: 4 Kbytes, 16 Kbytes, or 64 Kbytes.
<table>
<tr><th>MODE0</th><th>MODE1</th><th>External memory</th></tr>
<tr><td>0</td><td>0</td><td>4 Kbytes</td></tr>
<tr><td>1</td><td>0</td><td>16 Kbytes</td></tr>
<tr><td>1</td><td>1</td><td>64 Kbytes</td></tr>
</table>
If MODE0 and MODE1 are both set to “1”(Note), a control signal is output synchronously with ALE.</td></tr>
<tr><td>$\overline{\text{NMI}}$
(Non-Maskable Interrupt)</td><td>I</td><td>This is a falling edge-triggered nonmaskable interrupt input pin.</td></tr>
<tr><td>INT1
(Interrupt Request)</td><td>I</td><td>INT1 is a rising edge-triggered maskable interrupt input pin. It is also an AC-input, zero-cross detection pin.</td></tr>
<tr><td>AN7-0
(Analog Input)</td><td>I</td><td>These are eight analog inputs to the A/D converter. AN4 to AN7 can also be used as inputs for falling edge detection.</td></tr>
<tr><td>V_{AREF}
(Reference Voltage)</td><td>I</td><td>This pin can be used as a reference voltage input for the A/D converter or as a control pin for A/D converter operation.</td></tr>
<tr><td>AV_{DD}
(Analog V_{DD})</td><td></td><td>This is the power supply pin for the A/D converter.</td></tr>
<tr><td>AV_{SS}
(Analog V_{SS})</td><td></td><td>This is the ground pin for the A/D converter.</td></tr>
<tr><td>X1, X2
(Crystal)</td><td></td><td>These are the crystal pins for the system clock oscillator. X1 inputs an external clock. X2 inputs the inverted clock from X1. ★</td></tr>
<tr><td>$\overline{\text{RESET}}$
(Reset)</td><td>I</td><td>This is the system reset input pin (active low).</td></tr>
<tr><td>$\overline{\text{STOP}}$
(Stop)</td><td>I</td><td>This is the control signal input pin during hardware STOP mode. Low-level input stops the system clock oscillator.</td></tr>
<tr><td>V_{DD}</td><td></td><td>Positive power supply pin</td></tr>
<tr><td>V_{SS}</td><td></td><td>Ground pin</td></tr>
</table>

Note These must be pulled up using a pull-up resistance value (R) of 4 (kΩ) $\leq$ R $\leq$ 0.4 t_{CYC} (kΩ). (t_{CYC} is in ns units.)

Remark On-chip pull-up resistors for Ports A, B, and C are available as mask options on the μPD78C11A(A) or 78C12A(A).

1.2 Pin I/O Lines

Tables 1-1 and 1-2 list the I/O lines to the various pins, and (1) to (15) show partial diagrams of these lines.

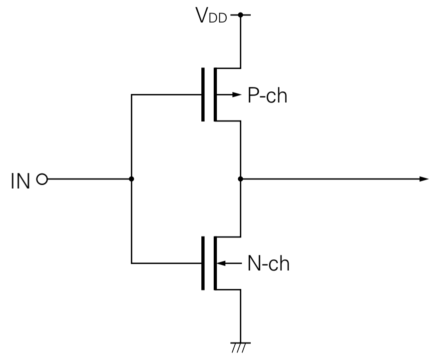
Table 1-1. Pin Type Numbers (μPD78C10A(A))

Pin name	Type No.	Pin name	Type No.
PA7-0	5	$\overline{RESET}$	2
PB7-0	5	$\overline{RD}$	4
PC1-0	5	$\overline{WR}$	4
PC2/$\overline{SCK}$	8	ALE	4
PC3/$\overline{INT2}$	10	$\overline{STOP}$	2
PC7-4	5	MODE0	11
PD7-0	5	MODE1	11
PF7-0	5	AN3-0	7
$\overline{NMI}$	2	AN7-4	12
INT1	9	V_{AREF}	13

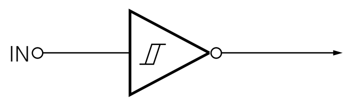
Table 1-2. Pin Type Numbers (μPD78C11A(A), 78C12A(A))

Pin name	Type No.	Pin name	Type No.
PA7-0	5-A	$\overline{RESET}$	2
PB7-0	5-A	$\overline{RD}$	4
PC1-0	5-A	$\overline{WR}$	4
PC2/$\overline{SCK}$	8-A	ALE	4
PC3/$\overline{INT2}$	10-A	$\overline{STOP}$	2
PC7-4	5-A	MODE0	11
PD7-0	5	MODE1	11
PF7-0	5	AN3-0	7
$\overline{NMI}$	2	AN7-4	12
INT1	9	V_{AREF}	13

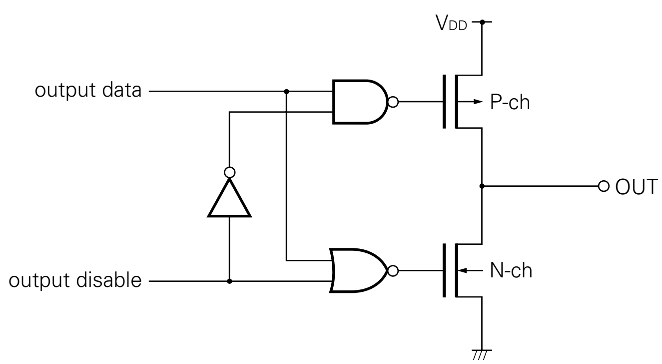
(1) Type1



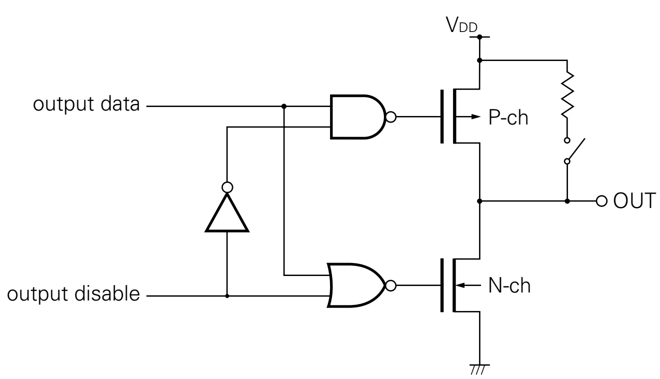
(2) Type2



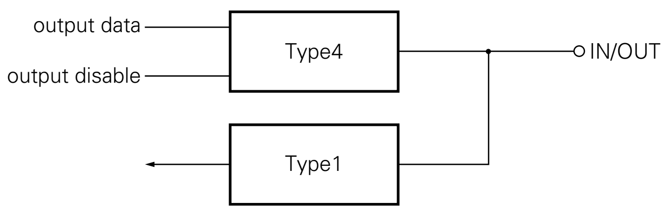
(3) Type4



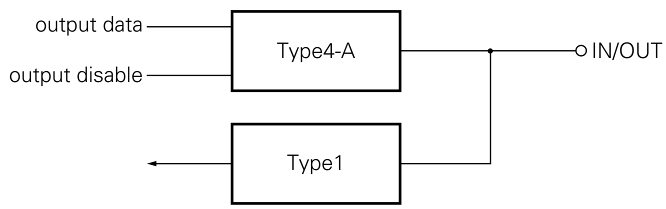
(4) Type4-A



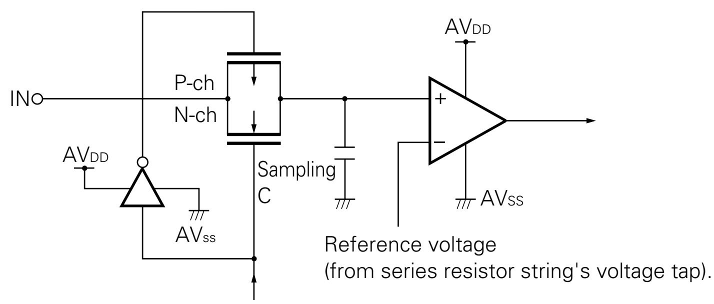
(5) Type5



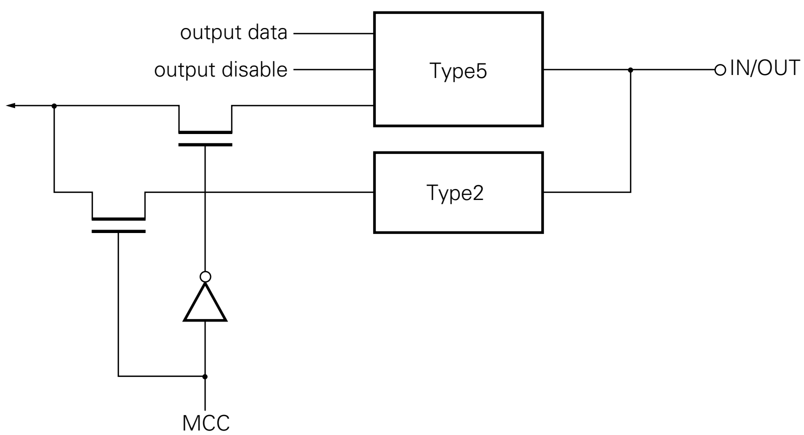
(6) Type5-A



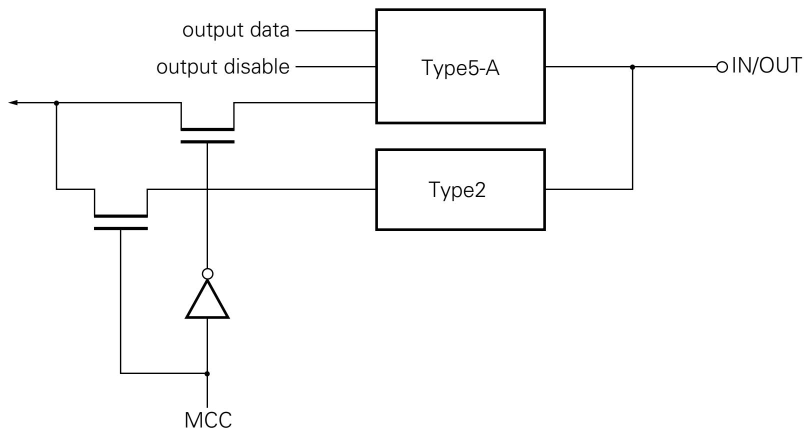
(7) Type7



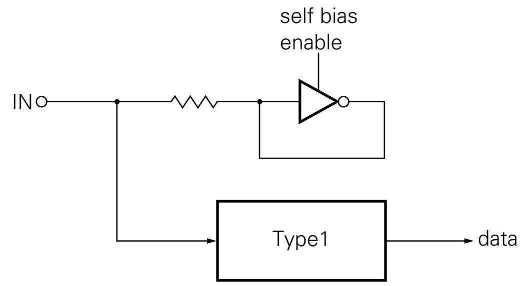
(8) Type8



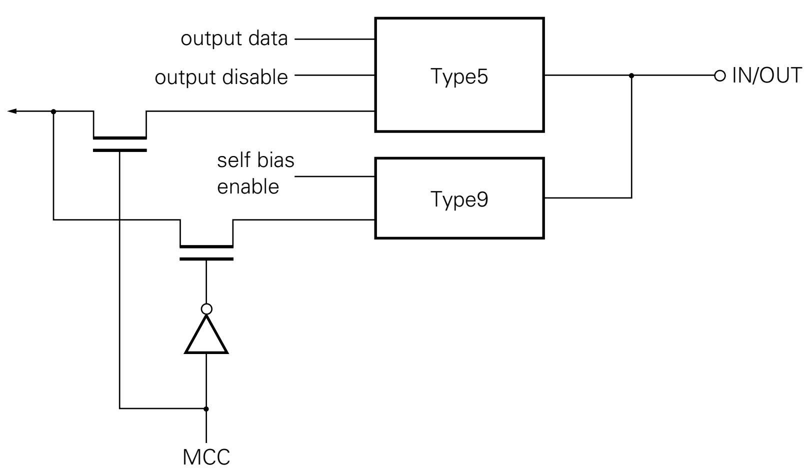
(9) Type8-A



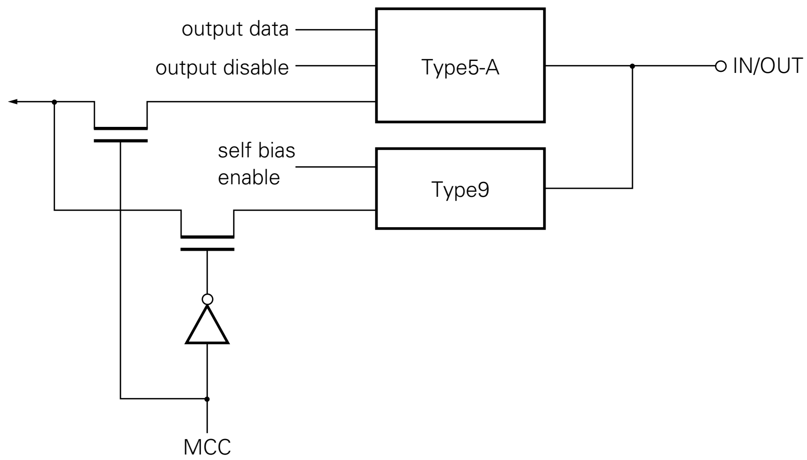
(10) Type9



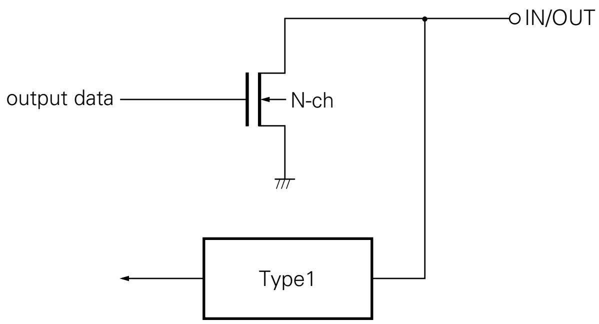
(11) Type10



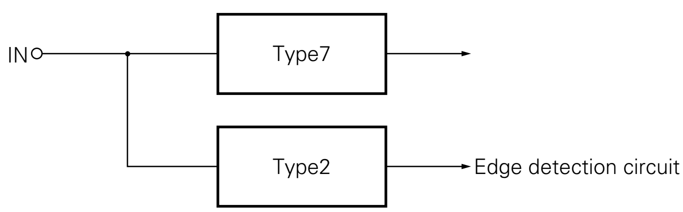
(12) Type10-A



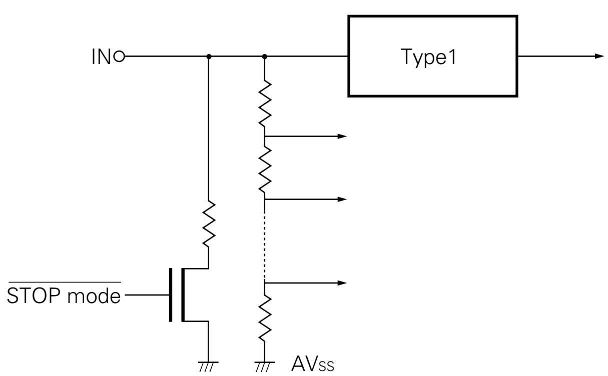
(13) Type11



(14) Type12



(15) Type13



1.3 Pin Mask Options

The following mask options are available for pins in the μPD78C11A(A) and 78C12A(A). They are selectable bit-wise according to the use objective.

Pin name	Mask option
PA7-0	(a) On-chip pull-up resistor (b) No on-chip pull-up resistor
PB7-0	
PC7-0	

Cautions 1. If there is an on-chip pull-up resistor for PC3, the zero-cross function will not operate normally.

2. The μPD78C10A(A) has no mask options.

1.4 Recommended Connections of Unused Pins

Pin	Recommended connection
PA7-0	Connect via a resistor to V_{SS} or V_{DD}.
PB7-0	
PC7-0	
PD7-0	
PF7-0	
$\overline{RD}$	No connection
$\overline{WR}$	
ALE	
$\overline{STOP}$	Connect to V_{DD}.
INT1, $\overline{NMI}$	Connect to V_{SS} or V_{DD}.
AV_{DD}	Connect to V_{DD}.
V_{AREF}	Connect to V_{SS}.
AV_{SS}	
AN7-0	Connect to AV_{SS} or AV_{DD}.

2. DIFFERENCES BETWEEN (1) μPD78C10A(A) AND (2) μPD78C11A(A) AND 78C12A(A)

The main difference between the μPD78C10A(A) and the μPD78C11A(A) and 78C12A(A) is that the μPD78C10A(A) does not have an on-chip mask programmable ROM. This results in the memory mapping differences described below.

(1) μPD78C10A(A)

Because the μPD78C10A(A) does not have on-chip ROM, all memory except for the on-chip RAM area (FF00H to FFFFH) are installed externally. The amount of externally installed memory can be set using the MODE0 and MODE1 pins. As shown in the following table and in Figure 2-1, there are three memory access options: 4 Kbytes (0000H to 0FFFH), 16 Kbytes (0000H to 3FFFH) and 64 Kbytes (0000H to FEFFH).

Operation mode	Control pins		External memory	On-chip RAM
	MODE1	MODE0		
4-Kbyte access	0	0	4 Kbytes (addresses 0000H to 0FFFH)	Addresses FF00H to FFFFH
16-Kbyte access	0	1	16 Kbytes (addresses 0000H to 3FFFH)	Addresses FF00H to FFFFH
64-Kbyte access	1	1	64 Kbytes (addresses 0000H to FEFFH)	Addresses FF00H to FFFFH

External memory can be accessed via PD0 to PD7 (multiplexed address/data buses), PF0 to PF7 (address buses), or the $\overline{\text{RD}}$, $\overline{\text{WR}}$, or ALE signals. When accessing 4 Kbytes or 16 Kbytes of external memory, address buses (PF0 to PF7) that are not being used as address lines can be used as an ordinary I/O port.

Use the MODE0 and MODE1 pins to select the amount of externally installed memory and set the memory mapping register's MM2, MM1, and MM0 bits to "0".

(2) μPD78C11A(A), 78C12A(A)

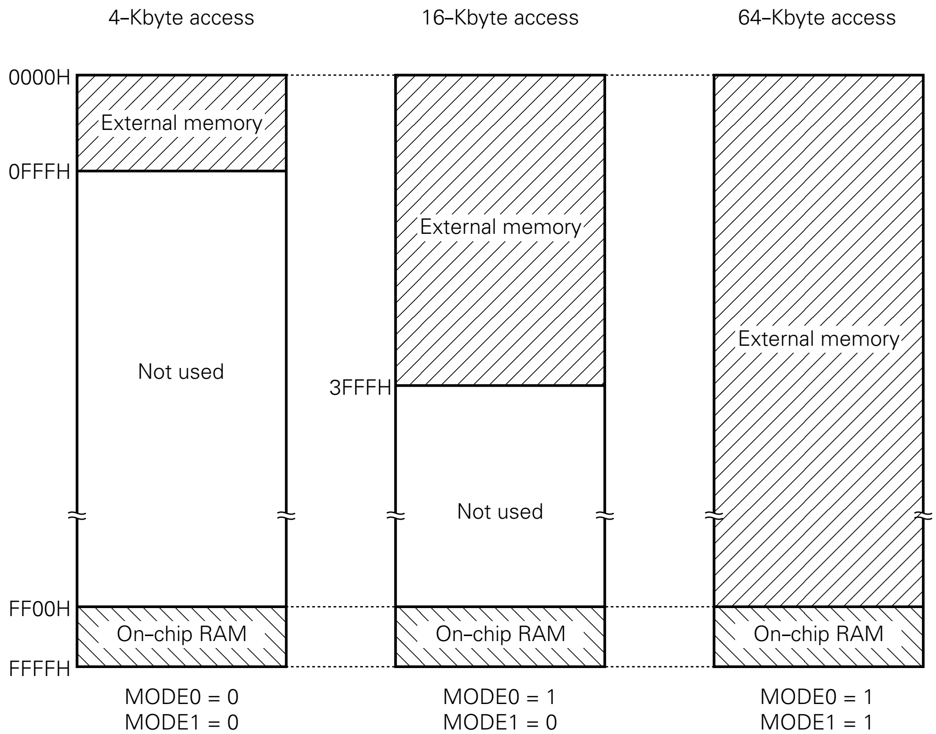
The μPD78C11A(A) has on-chip mask programmable ROM from addresses 0000H to 0FFFH and on-chip RAM from addresses FF00H to FFFFH. Up to 60 Kbytes (addresses 1000H to FEFFH) of external expansion memory can be added in steps. The μPD78C12A(A) has on-chip mask programmable ROM from addresses 0000H to 1FFFH and on-chip RAM from addresses FF00H to FFFFH. Up to 56 Kbytes (addresses 2000H to FEFFH) of external expansion memory can be added in steps.

Set the memory mapping register to select among five external expansion memory modes: no external memory, 256 bytes, 4 Kbytes, 16 Kbytes, and 56 or 60 Kbytes(Note). External memory can be accessed via PD0 to PD7 (multiplexed address/data buses), PF0 to PF7 (address buses), or using the $\overline{\text{RD}}$, $\overline{\text{WR}}$, or ALE signals. External memory can contain either programs or data. Some address buses (PF0 to PF7) are used as address lines, depending on the memory size, and any remaining address buses can be used as an ordinary I/O port.

PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	External memory
Port	Port	Port	Port	Port	Port	Port	Port	256 bytes max
Port	Port	Port	Port	AB11	AB10	AB9	AB8	4 Kbytes max
Port	Port	AB13	AB12	AB11	AB10	AB9	AB8	16 Kbytes max
AB15	AB14	AB13	AB12	AB11	AB10	AB9	AB8	56/60 Kbytes max(Note)

Note 56 Kbytes for the μPD78C12A(A) and 60 Kbytes for the μPD78C11A(A)

Figure 2-1. μPD78C10A(A) Memory Map



3. RESET OPERATION

Low-level input to the $\overline{\text{RESET}}$ input causes a system reset, after which the following states occur.

- INTERRUPT ENABLE F/F is reset and the interrupt disable state occurs.
- All interrupt mask registers are set (to "1") so that all interrupts are masked.
- The interrupt request flag is set (to "0") so that any pending interrupt is released.
- All PSWs are reset (to "0").
- 0000H is loaded into the program counter (PC).
- The MODE A register, MODE B register, MODE C register, and MODE F register are set to FFH and the MM0, MM1, and MM2 bits in the mode control C register and memory mapping register are reset (to "0"). Port A, Port B, Port C, Port D, and Port F all become input ports (high-impedance output).
- All test flags except the SB flag are reset (to "0").
- The timer mode register is set to FFH and the timer F/F is reset.
- The timer/event counter's mode registers (ETMM, EOM) are reset (to "0").
- The serial interface's serial mode high register (SMH) is reset (to "0") and the serial mode low register (SML) is set to 48H.
- The A/D converter's A/D channel mode register is reset (to "0").
- The $\overline{\text{WR}}$, $\overline{\text{RD}}$, and ALE signal are set for high impedance.
- Zero cross mode register (ZCM) bits ZC1 and ZC2 are set to "1".
- The internal timers are initialized.
- The data memory and the contents of the following registers are undefined.

  Stack pointer (SP)
  Expansion accumulators (EA, EA') and accumulators (A, A')
  General-purpose registers (B, C, D, E, H, L, B', C', D', E', H', L')
  Output latch for each port
  Timer REG0 and REG1 (TM0, TM1)
  Timer/event counter REG0 and REG1 (ETM0, ETM1)
  Memory mapping register's RAE bit
  Test flags' SB flag

When $\overline{\text{RESET}}$ input goes high, the reset state is canceled and program execution begins from address 0000H. At that point, initialize or reinitialize the various register contents as required by the program.

Table 3-1 lists various hardware states after reset and Table 3-2 lists various pin states after reset.

Table 3-1. Hardware States after Reset

Hardware				State after reset	
Internal data memory	During power-on reset			Previous contents are retained	
	$\overline{\text{RESET}}$ input during normal operation	During CPU write operation	Write address data	Undefined	
			Other address data	Previous contents are retained	
		Operation other than CPU write			
	$\overline{\text{RESET}}$ input during standby mode				
Expansion accumulators (EA, EA’)				Undefined	
Accumulators (A, A’)					
General-purpose registers (B, C, D, E, H, L, B′, C′, D′, E′, H′, L′)					
Working register’s vector registers (V, V’)					★
Program counter (PC)				0000H	
Stack pointer (SP)				Undefined	
Ports	Mode registers (MA, MB, MC, MF)			FFH	
	MCC register			00H	
	MM register (bits MM0 to MM2)			0	
Output latch for each port				Undefined	
Interrupt	INTERRUPT ENABLE F/F			0	
	Request flag			0	
	Mask register			FFH	
Test flags (except SB flag)				0	
Standby flag (SB)	During power-on reset			1	
	During standby mode			Previous contents are retained	
	$\overline{\text{RESET}}$ input during normal operation			Contents prior to $\overline{\text{RESET}}$ input are retained	★
Timer	Timer mode register (TMM)			FFH	
	Timer F/F			0	
	Timer registers (TM0, TM1)			Undefined	
Timer/event counter	Timer/event counter mode register (ETMM)			00H	
	Timer/event counter output mode register (EOM)				
	Timer/event counter registers (ETM0, ETM1)			Undefined	
	Timer/event counter capture register (ECPT)				
	Timer/event counter (ECNT)				★
Serial interface	Serial mode high register (SMH)			00H	
	Serial mode low register (SML)			48H	
A/D channel mode register (ANM)				00H	
MM register (MM3, RAE bit)				Undefined	
Zero-cross mode register (bits ZC1 and ZC2)				1	

Table 3-2. Pin States after Reset

Pin	State after reset
$\overline{WR}$	High impedance
$\overline{RD}$	
ALE	
All ports (PA, PB, PC, PD, PF)	

4. INSTRUCTION SET

4.1 Operand Symbols and Definitions

Symbol	Definition
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TXB, TM0, TM1, ZCM
sr1	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM, RXB, CR0, CR1, CR2, CR3
sr2	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM
sr3	ETM0, ETM1
sr4	ECNT, ECPT
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
rpa	B, D, H, D +, H +, D –, H –
rpa1	B, D, H
rpa2	B, D, H, D +, H +, D –, H –, D + byte, H + A, H + B, H + EA, H + byte
rpa3	D, H, D ++, H ++, D + byte, H + A, H + B, H + EA, H + byte
wa	8 bit immediate data
word	16 bit immediate data
byte	8 bit immediate data
bit	3 bit immediate data
f	CY, HC, Z
irf	NMI(Note), FT0, FT1, F1, F2, FE0, FE1, FEIN, FAD, FSR, FST, ER, OV, AN4, AN5, AN6, AN7, SB

Note "NMI" can also be written as "FNMI".

Remarks

1. sr to sr4 (special register)

PA	PORT A	ETMM	TIMER/EVENT COUNTER MODE
PB	PORT B	EOM	TIMER/EVENT COUNTER OUTPUT MODE
PC	PORT C	ANM	A/D CHANNEL MODE
PD	PORT D	CR0 to CR3	A/D CONVERSION RESULT 0 to 3
PF	PORT F	TXB	Tx BUFFER
MA	MODE A	RXB	Rx BUFFER
MB	MODE B	SMH	SERIAL MODE High
MC	MODE C	SML	SERIAL MODE Low
MCC	MODE CONTROL C	MKH	MASK High
MF	MODE F	MKL	MASK Low
MM	MEMORY MAPPING	ZCM	ZERO CROSS MODE
TM0	TIMER REG0		
TM1	TIMER REG1		
TMM	TIMER MODE		
ETM0	TIMER/EVENT COUNTER REG0		
ETM1	TIMER/EVENT COUNTER REG1		
ECNT	TIMER/EVENT COUNTER UPCOUNTER		
ECPT	TIMER/EVENT COUNTER CAPTURE		

2. rp to rp3 (register pair)

SP	STACK POINTER
B	BC
D	DE
H	HL
V	VA
EA	EXTENDED ACCUMULATOR

3. rpa to rpa3 (rp addressing)

B	(BC)
D	(DE)
H	(HL)
D +	$(DE)^+$
H +	$(HL)^+$
D –	$(DE)^-$
H –	$(HL)^-$
D ++	$(DE)^{++}$
H ++	$(HL)^{++}$
D + byte	(DE + byte)
H + A	(HL + A)
H + B	(HL + B)
H + EA	(HL + EA)
H + byte	(HL + byte)

4. f (flag)

CY	CARRY
HC	HALF CARRY
Z	ZERO

5. irf (interrupt flag)

NMI	NMI INPUT
FT0	INTFT0
FT1	INTFT1
F1	INTF1
F2	INTF2
FE0	INTFE0
FE1	INTFE1
FEIN	INTFEIN
FAD	INTFAD
FSR	INTFSR
FST	INTFST
ER	ERROR
OV	OVERFLOW
AN4 to AN7	ANALOG INPUT4 to 7
SB	STANDBY

4.2 Description of Instruction Code Symbols

r

R_2	R_1	R_0	reg
0	0	0	V
0	0	1	A
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

r2 r

r1

T_2	T_1	T_0	reg
0	0	0	EAH
0	0	1	EAL
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

rpa

A_3	A_2	A_1	A_0	addressing
0	0	0	0	——
0	0	0	1	(BC)
0	0	1	0	(DE)
0	0	1	1	(HL)
0	1	0	0	$(DE)^+$
0	1	0	1	$(HL)^+$
0	1	1	0	$(DE)^-$
0	1	1	1	$(HL)^-$
1	0	1	1	(DE + byte)
1	1	0	0	(HL + A)
1	1	0	1	(HL + B)
1	1	1	0	(HL + EA)
1	1	1	1	(HL + byte)

rpa rpa1 rpa2

sr

S_5	S_4	S_3	S_2	S_1	S_0	Special-reg
0	0	0	0	0	0	PA
0	0	0	0	0	1	PB
0	0	0	0	1	0	PC
0	0	0	0	1	1	PD
0	0	0	1	0	1	PF
0	0	0	1	1	0	MKH
0	0	0	1	1	1	MKL
0	0	1	0	0	0	ANM
0	0	1	0	0	1	SMH
0	0	1	0	1	0	SML
0	0	1	0	1	1	EOM
0	0	1	1	0	0	ETMM
0	0	1	1	0	1	TMM
0	1	0	0	0	0	MM
0	1	0	0	0	1	MCC
0	1	0	0	1	0	MA
0	1	0	0	1	1	MB
0	1	0	1	0	0	MC
0	1	0	1	1	1	MF
0	1	1	0	0	0	TXB
0	1	1	0	0	1	RXB
0	1	1	0	1	0	TM0
0	1	1	0	1	1	TM1
1	0	0	0	0	0	CR0
1	0	0	0	0	1	CR1
1	0	0	0	1	0	CR2
1	0	0	0	1	1	CR3
1	0	1	0	0	0	ZCM

sr sr1 sr2

rpa3

C_3	C_2	C_1	C_0	addressing
0	0	1	0	(DE)
0	0	1	1	(HL)
0	1	0	0	$(DE)^{++}$
0	1	0	1	$(HL)^{++}$
1	0	1	1	(DE + byte)
1	1	0	0	(HL + A)
1	1	0	1	(HL + B)
1	1	1	0	(HL + EA)
1	1	1	1	(HL + byte)

irf

I_4	I_3	I_2	I_1	I_0	INTF
0	0	0	0	0	NMI
0	0	0	0	1	FT0
0	0	0	1	0	FT1
0	0	0	1	1	F1
0	0	1	0	0	F2
0	0	1	0	1	FE0
0	0	1	1	0	FE1
0	0	1	1	1	FEIN
0	1	0	0	0	FAD
0	1	0	0	1	FSR
0	1	0	1	0	FST
0	1	0	1	1	ER
0	1	1	0	0	OV
1	0	0	0	0	AN4
1	0	0	0	1	AN5
1	0	0	1	0	AN6
1	0	0	1	1	AN7
1	0	1	0	0	SB

sr3

U_0	Special-reg
0	ETM0
1	ETM1

sr4

V_0	Special-reg
0	ECNT
1	ECPT

rp

P_2	P_1	P_0	reg-pair
0	0	0	SP
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA

rp rp2 rp3

rp1

Q_2	Q_1	Q_0	reg-pair
0	0	0	VA
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA

f

F_2	F_1	F_0	Flag
0	0	0	——
0	1	0	CY
0	1	1	HC
1	0	0	Z

4.3 Instruction Execution Times

Below, one state is equal to three clock cycles. When using a 15-MHz clock, one state is 200 ns (= 3 x 1/15 μs). In this case, the minimum execution time for a four-state instruction time is 0.8 μs.

Instruction group	Mnemonic		Operand	Instruction code B1	B2	B3	B4	States	Operation	Skip condition
8-bit data transfer instructions	MOV		r1, A	$00011T_2T_1T_0$				4	r1←A	
			A, r1	$00001T_2T_1T_0$				4	A←r1	
		*	sr, A	01001101	$11S_5S_4S_3S_2S_1S_0$			10	sr←A	
		*	A, sr1	01001100	$11S_5S_4S_3S_2S_1S_0$			10	A←sr1	
			r, word	01110000	$01101R_2R_1R_0$	Low Adrs	High Adrs	17	r←(word)	
			word, r	01110000	$01111R_2R_1R_0$	Low Adrs	High Adrs	17	(word)←r	
	MVI	*	r, byte	$01101R_2R_1R_0$	←Data→			7	r←byte	
			sr2, byte	01100100	$S_30000S_2S_1S_0$	Data		14	sr2←byte	
	MVIW	*	wa, byte	01110001	←Offset→	Data		13	(V.wa)←byte	
	MVIX	*	rpa1, byte	$010010A_1A_0$	←Data→			10	(rpa1)←byte	
	STAW	*	wa	01100011	←Offset→			10	(V.wa)←A	
	LDAW	*	wa	00000001	←Offset→			10	A←(V.wa)	
	STAX	*	rpa2	$A_30111A_2A_1A_0$	Data (Note 1)			7/13 (Note 3)	(rpa2)←A	
	LDAX	*	rpa2	$A_30101A_2A_1A_0$	Data (Note 1)			7/13 (Note 3)	A←(rpa2)	
	EXX			00010001				4	{B↔B', C↔C', D↔D' E↔E', H↔H', L↔L'	
	EXA			00010000				4	V,A↔V',A', EA↔EA'	
	EXH			01010000				4	H,L↔H',L'	
	BLOCK			00110001				13 (C+1)	$(DE)^+$←$(HL)^+$,C←C−1 End if borrow	
16-bit data transfer instructions	DMOV		rp3, EA	$101101P_1P_0$				4	$rp3_L$←EAL, $rp3_H$←EAH	
			EA, rp3	$101001P_1P_0$				4	EAL←$rp3_L$, EAH←$rp3_H$	

Instruction group	Mnemonic	Operand	Instruction code B1	B2	B3	B4	States	Operation	Skip condition
16-bit data transfer instructions	DMOV	sr3, EA	01001000	$1101001U_0$			14	sr3←EA	
		EA, sr4	↓ ↓	$1100000V_0$			14	EA←sr4	
	SBCD	word	01110000	00011110	Low Adrs	High Adrs	20	(word)←C, (word + 1)←B	
	SDED	word		00101110			20	(word)←E, (word + 1)←D	
	SHLD	word		00111110			20	(word)←L, (word + 1)←H	
	SSPD	word	↓ ↓	00001110	↓	↓	20	(word)←SP_L, (word + 1)←SP_H	
	STEAX	rpa3	01001000	$1001C_3C_2C_1C_0$	Data(Note 2)		14/20(Note 3)	(rpa3)←EAL, (rpa3 + 1)←EAH	
	LBCD	word	01110000	00011111	Low Adrs	High Adrs	20	C←(word), B←(word + 1)	
	LDED	word		00101111			20	E←(word), D←(word + 1)	
	LHLD	word		00111111			20	L←(word), H←(word + 1)	
	LSPD	word	↓ ↓	00001111	↓	↓	20	SP_L←(word), SP_H←(word + 1)	
	LDEAX	rpa3	01001000	$1000C_3C_2C_1C_0$	Data(Note 2)		14/20(Note 3)	EAL←(rpa3), EAH←(rpa3 + 1)	
	PUSH	rp1	$10110Q_2Q_1Q_0$				13	(SP – 1)←$rp1_H$, (SP – 2)←$rp1_L$ SP←SP – 2	
	POP	rp1	$10100Q_2Q_1Q_0$				10	$rp1_L$←(SP), $rp1_H$←(SP + 1) SP←SP + 2	
	LXI *	rp2, word	$0P_2P_1P_0 0100$	←Low Byte→	High Byte		10	rp2←word	
	TABLE		01001000	10101000			17	C←(PC + 3 + A) B←(PC + 3 + A + 1)	
8-bit arithmetic instructions (register)	ADD	A, r	01100000	$11000R_2R_1R_0$			8	A←A + r	
		r, A		0100			8	r←r + A	
	ADC	A, r		1101			8	A←A + r + CY	
		r, A	↓ ↓	0101 ↓			8	r←r + A + CY	

Instruction group	Mnemonic	Operand	Instruction code B1	Instruction code B2	Instruction code B3	Instruction code B4	States	Operation	Skip condition
8-bit arithmetic instructions (register)	ADDNC	A, r	01100000	10100R2R1R0			8	A←A + r	No Carry
		r, A		0010			8	r←r + A	No Carry
	SUB	A, r		1110			8	A←A – r	
		r, A		0110			8	r←r – A	
	SBB	A, r		1111			8	A←A – r – CY	
		r, A		0111			8	r←r – A – CY	
	SUBNB	A, r		1011			8	A←A – r	No Borrow
		r, A		0011			8	r←r – A	No Borrow
	ANA	A, r		10001R2R1R0			8	A←A ∧ r	
		r, A		0000			8	r←r ∧ A	
	ORA	A, r		1001			8	A←A ∨ r	
		r, A		0001			8	r←r ∨ A	
	XRA	A, r		10010R2R1R0			8	A←A ∀ r	
		r, A		0001			8	r←r ∀ A	
	GTA	A, r		10101R2R1R0			8	A – r – 1	No Borrow
		r, A		0010			8	r – A – 1	No Borrow
	LTA	A, r		1011			8	A – r	Borrow
		r, A		0011			8	r – A	Borrow
	NEA	A, r		1110			8	A – r	No Zero
		r, A		0110			8	r – A	No Zero

Instruction group	Mnemonic	Operand	Instruction code				States	Operation	Skip condition
			B1	B2	B3	B4			
8-bit arithmetic instructions (register)	EQA	A, r	01100000	$11111R_2R_1R_0$			8	A – r	Zero
		r, A		0111			8	r – A	Zero
	ONA	A, r		1100			8	A ∧ r	No Zero
	OFFA	A, r		1101			8	r∧ A	Zero
8-bit arithmetic instructions (memory)	ADDX	rpa	01110000	$11000A_2A_1A_0$			11	A←A + (rpa)	
	ADCX	rpa		1101			11	A←A + (rpa) + CY	
	ADDNCX	rpa		1010			11	A←A + (rpa)	No Carry
	SUBX	rpa		1110			11	A←A – (rpa)	
	SBBX	rpa		1111			11	A←A – (rpa) – CY	
	SUBNBX	rpa		1011			11	A←A – (rpa)	No Borrow
	ANAX	rpa		$10001A_2A_1A_0$			11	A←A ∧ (rpa)	
	ORAX	rpa		1001			11	A←A ∨ (rpa)	
	XRAX	rpa		$10010A_2A_1A_0$			11	A←A ∀ (rpa)	
	GTAX	rpa		$10101A_2A_1A_0$			11	A – (rpa) - 1	No Borrow
	LTAX	rpa		1011			11	A - (rpa)	Borrow
	NEAX	rpa		1110			11	A - (rpa)	No Zero
	EQAX	rpa		1111			11	A - (rpa)	Zero
	ONAX	rpa		1100			11	A ∧ (rpa)	No Zero
	OFFAX	rpa		1101			11	A ∧ (rpa)	Zero

Phase-out/Discontinued

Instruction group	Mnemonic	Operand	Instruction code B1	B2	B3	B4	States	Operation	Skip condition
Immediate data arithmetic instructions	ADI *	A, byte	01000110	←Data→			7	A←A + byte	
		r, byte	01110100	$01000R_2R_1R_0$	Data		11	r←r + byte	
		sr2, byte	0110 ↓	$S_31000S_2S_1S_0$	↓		20	sr2←sr2 + byte	
	ACI *	A, byte	01010110	←Data→			7	A←A + byte + CY	
		r, byte	01110100	$01010R_2R_1R_0$	Data		11	r←r + byte + CY	
		sr2, byte	0110 ↓	$S_31010S_2S_1S_0$	↓		20	sr2←sr2 + byte + CY	
	ADINC *	A, byte	00100110	←Data→			7	A←A + byte	No Carry
		r, byte	01110100	$00100R_2R_1R_0$	Data		11	r←r + byte	No Caryy
		sr2, byte	0110 ↓	$S_30100S_2S_1S_0$	↓		20	sr2←sr2 + byte	No Carry
	SUI *	A, byte	01100110	←Data→			7	A←A – byte	
		r, byte	01110100	$01100R_2R_1R_0$	Data		11	r←r – byte	
		sr2, byte	0110 ↓	$S_31100S_2S_1S_0$	↓		20	sr2←sr2 – byte	
	SBI *	A, byte	01110110	←Data→			7	A←A – byte – CY	
		r, byte	01110100	$01110R_2R_1R_0$	Data		11	r←r – byte – CY	
		sr2, byte	0110 ↓	$S_31110S_2S_1S_0$	↓		20	sr2←sr2 – byte – CY	
	SUINB *	A, byte	00110110	←Data→			7	A←A – byte	No Borrow
		r, byte	01110100	$00110R_2R_1R_0$	Data		11	r←r – byte	No Borrow
		sr2, byte	0110 ↓	$S_30110S_2S_1S_0$	↓		20	sr2←sr2 – byte	No Borrow
	ANI *	A, byte	00000111	←Data→			7	A←A ∧ byte	
		r, byte	01110100	$00001R_2R_1R_0$	Data		11	r←r∧ byte	

Instruction group	Mnemonic		Operand	Instruction code B1	B2	B3	B4	States	Operation	Skip condition
Immediate data arithmetic instructions	ANI		sr2, byte	01100100	$S_3 0001 S_2 S_1 S_0$	Data		20	sr2←sr2 ∧ byte	
	ORI	*	A, byte	00010111	←Data→			7	A←A ∨ byte	
			r, byte	01110100	$00011 R_2 R_1 R_0$	Data		11	r←r ∨ byte	
			sr2, byte	0110 ↓	$S_3 0011 S_2 S_1 S_0$	↓		20	sr2←sr2 ∨ byte	
	XRI	*	A, byte	00010110	←Data→			7	A←A ∀ byte	
			r, byte	01110100	$00010 R_2 R_1 R_0$	Data		11	r←r ∀ byte	
			sr2, byte	0110 ↓	$S_3 0010 S_2 S_1 S_0$	↓		20	sr2←sr2 ∀ byte	
	GTI	*	A, byte	00100111	←Data→			7	A – byte – 1	No Borrow
			r, byte	01110100	$00101 R_2 R_1 R_0$	Data		11	r – byte – 1	No Borrow
			sr2, byte	0110 ↓	$S_3 0101 S_2 S_1 S_0$	↓		14	sr2 – byte – 1	No Borrow
	LTI	*	A, byte	00110111	←Data→			7	A – byte	Borrow
			r, byte	01110100	$00111 R_2 R_1 R_0$	Data		11	r – byte	Borrow
			sr2, byte	0110 ↓	$S_3 0111 S_2 S1 S_0$	↓		14	sr2 – byte	Borrow
	NEI	*	A, byte	01100111	←Data→			7	A – byte	No Zero
			r, byte	01110100	$01101 R_2 R_1 R_0$	Data		11	r – byte	No Zero
			sr2, byte	0110 ↓	$S_3 1101 S_2 S_1 S_0$	↓		14	sr2 – byte	No Zero
	EQI	*	A, byte	01110111	←Data→			7	A – byte	Zero
			r, byte	01110100	$01111 R_2 R_1 R_0$	Data		11	r – byte	Zero
			sr2, byte	0110 ↓	$S_3 1111 S_2 S_1 S_0$	↓		14	sr2 – byte	Zero

Phase-out/Discontinued

Instruction group	Mnemonic	Operand	Instruction code B1	B2	B3	B4	States	Operation	Skip condition
Immediate data arithmetic instructions	ONI *	A, byte	01000111	Data			7	A ∧ byte	No Zero
		r, byte	01110100	01001$R_2R_1R_0$	Data		11	r ∧ byte	No Zero
		sr2, byte	0110	$S_3$1001$S_2S_1S_0$			14	sr2∧ byte	No Zero
	OFFI *	A, byte	01010111	Data			7	A ∧ byte	Zero
		r, byte	01110100	01011$R_2R_1R_0$	Data		11	r ∧ byte	Zero
		sr2, byte	0110	$S_3$1011$S_2S_1S_0$			14	sr2∧ byte	Zero
Working register arithmetic instructions	ADDW	wa	01110100	11000000	offset		14	A←A + (V.wa)	
	ADCW	wa		1101			14	A←A + (V.wa) + CY	
	ADDNCW	wa		1010			14	A←A + (V.wa)	No Carry
	SUBW	wa		1110			14	A←A – (V.wa)	
	SBBW	wa		1111			14	A←A – (V.wa) – CY	
	SUBNBW	wa		1011			14	A←A – (V.wa)	No Borrow
	ANAW	wa		10001000			14	A←A ∧ (V.wa)	
	ORAW	wa		1001			14	A←A ∨ (V.wa)	
	XRAW	wa		10010000			14	A←A ∀ (V.wa)	
	GTAW	wa		10101000			14	A – (V.wa) – 1	No Borrow
	LTAW	wa		1011			14	A – (V.wa)	Borrow
	NEAW	wa		1110			14	A – (V.wa)	No Zero
	EQAW	wa		1111			14	A – (V.wa)	Zero
	ONAW	wa		1100			14	A ∧ (V.wa)	No Zero

Instruction group	Mnemonic	Operand	Instruction code B1	B2	B3	B4	States	Operation	Skip condition
Working register arithmetic instructions	OFFAW	wa	01110100	11011000	Offset		14	A ∧ (V.wa)	Zero
	ANIW *	wa, byte	00000101	←Offset→	Data		19	(V.wa)←(V.wa) ∧ byte	
	ORIW *	wa, byte	0001				19	(V.wa)←(V.wa) ∨ byte	
	GTIW *	wa, byte	0010				13	(V.wa) – byte – 1	No Borrow
	LTIW *	wa, byte	0011				13	(V.wa) – byte	Borrow
	NEIW *	wa, byte	0110				13	(V.wa) – byte	No Zero
	EQIW *	wa, byte	0111				13	(V.wa) – byte	Zero
	ONIW *	wa, byte	0100				13	(V.wa) ∧ byte	No Zero
	OFFIW *	wa, byte	0101				13	(V.wa) ∧ byte	Zero
16-bit arithmetic instructions	EADD	EA, r2	01110000	$010000R_1R_0$			11	EA←EA + r2	
	DADD	EA, rp3	0100	$110001P_1P_0$			11	EA←EA + rp3	
	DADC	EA, rp3		1101			11	EA←EA + rp3 + CY	
	DADDNC	EA, rp3		1010			11	EA←EA + rp3	No Carry
	ESUB	EA, r2	0000	$011000R_1R_0$			11	EA←EA – r2	
	DSUB	EA, rp3	0100	$111001P_1P_0$			11	EA←EA – rp3	
	DSBB	EA, rp3		1111			11	EA←EA – rp3 – CY	
	DSUBNB	EA, rp3		1011			11	EA←EA – rp3	No Borrow
	DAN	EA, rp3		$100011P_1P_0$			11	EA←EA ∧ rp3	
	DOR	EA, rp3		1001			11	EA←EA ∨ rp3	
	DXR	EA, rp3		$100101P_1P_0$			11	EA←EA ∀ rp3	

Instruction group	Mnemonic	Operand	Instruction code B1	B2	B3	B4	States	Operation	Skip condition
16-bit arithmetic instructions	DGT	EA, rp3	01110100	101011P_1P_0			11	EA – rp3 – 1	No Borrow
	DLT	EA, rp3		1011			11	EA – rp3	Borrow
	DNE	EA, rp3		1110			11	EA – rp3	No Zero
	DEQ	EA, rp3		1111			11	EA – rp3	Zero
	DON	EA, rp3		1100			11	EA ∧ rp3	No Zero
	DOFF	EA, rp3		1101			11	EA ∧ rp3	Zero
Multiply /divide instructions	MUL	r2	01001000	001011R_1R_0			32	EA←A × r2	
	DIV	r2		0011			59	EA←EA ÷ r2, r2←remainder	
Increment/decrement instructions	INR	r2	010000R_1R_2				4	r2←r2 + 1	Carry
	INRW *	wa	00100000	←Offset→			16	(V.wa)←(V.wa) + 1	Carry
	INX	rp	00$P_1P_0$0010				7	rp←rp + 1	
		EA	10101000				7	EA←EA + 1	
	DCR	r2	010100R_1R_2				4	r2←r2 – 1	Borrow
	DCRW *	wa	00110000	←Offset→			16	(V.wa)←(V.wa) – 1	Borrow
	DCX	rp	00$P_1P_0$0011				7	rp←rp – 1	
		EA	10101001				7	EA←EA – 1	
Other arithmetic instructions	DAA		01100001				4	Decimal Adjust Accumulator	
	STC		01001000	00101011			8	CY←1	
	CLC			00101010			8	CY←0	
	NEGA			00111010			8	A←$\overline{A}$ + 1	

Instruction group	Mnemonic	Operand	Instruction code B1	Instruction code B2	Instruction code B3	Instruction code B4	States	Operation	Skip condition
Rotation/shift instructions	RLD		01001000	00111000			17	Rotate Left Digit	
	RRD			1001			17	Rotate Right Digit	
	RLL	r2		01R_1R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow CY$, $CY \leftarrow r2_7$	
	RLR	r2		00R_1R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow CY$, $CY \leftarrow r2_0$	
	SLL	r2		001001R_1R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	
	SLR	r2		00R_1R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	
	SLLC	r2		000001R_1R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	Carry
	SLRC	r2		00R_1R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	Carry
	DRLL	EA		10110100			8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow CY$, $CY \leftarrow EA_{15}$	
	DRLR	EA		0000			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow CY$, $CY \leftarrow EA_0$	
	DSLL	EA		10100100			8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow 0$, $CY \leftarrow EA_{15}$	
	DSLR	EA		0000			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow 0$, $CY \leftarrow EA_0$	
Jump instructions	JMP *	word	01010100	← Low Adrs →	High Adrs		10	PC←word	
	JB		00100001				4	$PC_H \leftarrow B$, $PC_L \leftarrow C$	
	JR	word	11 ← jdisp 1 →				10	PC←PC + 1 + jdisp1	
	JRE *	word	0100111 ←	jdisp →			10	PC←PC + 2 + jdisp	
	JEA		01001000	00101000			8	PC←EA	
Call instructions	CALL *	word	01000000	← Low Adrs →	High Adrs		16	$(SP - 1) \leftarrow (PC + 3)_H$, $(SP - 2) \leftarrow (PC + 3)_L$ PC←word, SP←SP − 2	
	CALB		01001000	00101001			17	$(SP - 1) \leftarrow (PC + 2)_H$, $(SP - 2) \leftarrow (PC + 2)_L$ $PC_H \leftarrow B$, $PC_L \leftarrow C$, SP←SP − 2	
	CALF *	word	01111 ←	fa →			13	$(SP - 1) \leftarrow (PC + 2)_H$, $(SP - 2) \leftarrow (PC + 2)_L$ $PC_{15-11} \leftarrow 00001$, $PC_{10-0} \leftarrow fa$, SP←SP − 2	

Instruction group	Mnemonic	Operand	Instruction code B1	B2	B3	B4	States	Operation	Skip condition
Call instructions	CALT	word	100←ta→				16	$(SP - 1) \leftarrow (PC + 1)_H$, $(SP - 2) \leftarrow (PC + 1)_L$ $PC_L \leftarrow (128 + 2ta)$, $PC_H \leftarrow (129 + 2ta)$, $SP \leftarrow SP - 2$	
	SOFTI		01110010				16	$(SP - 1) \leftarrow PSW$, $(SP - 2) \leftarrow (PC + 1)_H$, $(SP - 3) \leftarrow (PC + 1)_L$, $PC \leftarrow 0060H$, $SP \leftarrow SP - 3$	
Return instructions	RET		10111000				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP + 1)$ $SP \leftarrow SP + 2$	
	RETS		↓ 1001				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP + 1)$, $SP \leftarrow SP + 2$ $PC \leftarrow PC + n$	Unconditional skip
	RETI		01100010				13	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP + 1)$, $PSW \leftarrow (SP + 2)$, $SP \leftarrow SP + 3$	
Skip instructions	BIT *	bit, wa	$01011B_2B_1B_0$	←Offset→			10	Skip if (V.wa) bit = 1	(V.wa)bit = 1
	SK	f	01001000	$00001F_2F_1F_0$			8	Skip if f = 1	f = 1
	SKN	f	↓ ↓	0001 ↓			8	Skip if f = 0	f = 0
	SKIT	irf	↓ ↓	$010I_4I_3I_2I_1I_0$			8	Skip if irf = 1, then reset irf	irf = 1
	SKNIT	irf	↓ ↓	$011I_4I_3I_2I_1I_0$			8	Skip if irf = 0 Reset irf, if irf = 1	irf = 0
CPU control instructions	NOP		00000000				4	No Operation	
	EI		10101010				4	Enable Interrupt	
	DI		10111010				4	Disable Interrupt	
	HLT		01001000	00111011			12	Set Halt Mode	
	STOP		01001000	10111011			12	Set Stop Mode	

Notes 1. B2 (Data) indicates the case when rpa2 = D + byte or H + byte.

2. B3 (Data) indicates the case when rpa3 = D + byte or H + byte.

3. In the "States" column, the value on the right side of the slash indicates the case when rpa2 or rpa3 = D + byte, H + A, H + B, H + EA, or H + byte.

Remark For the skip condition, the idle states differ from the execution states and are as follows.

1-byte instructions	: 4 states	3-byte instructions with *	: 10 states
2-byte instructions with*	: 7 states	3-byte instructions	: 11 states
2-byte instructions	: 8 states	4-byte instructions	: 14 states

5. MODE REGISTER LIST

Mode register		Read/ Write	Function
MA	Mode A register	W	Bit-wise specification of input or output for Port A
MB	Mode B register	W	Bit-wise specification of input or output for Port B
MCC	Mode control C register	W	Bit-wise specification of port or control mode for Port C
MC	Mode C register	W	Bit-wise specification of input or output for Port C in port mode
MM	Memory mapping register	W	Specification of port or expansion mode for Port D and Port F
MF	Mode F register	W	Bit-wise specification of input or output for Port F in port mode
TMM	Timer mode register	R/W	Specification of timer operation mode
ETMM	Timer/event counter mode register	W	Specification of timer/event counter's operation mode
EOM	Timer/event counter output mode register	R/W	Control of output level for CO0 and CO1
SML	Serial mode register	W	Specification of serial interface's operation mode
SMH		R/W	
MKL	Interrupt mask register	R/W	Specification of interrupt request enable/ disable state
MKH			
ANM	A/D channel mode register	R/W	Specification of A/D converter's operation mode
ZCM	Zero-cross mode register	W	Specification of zero-cross detection circuit operation

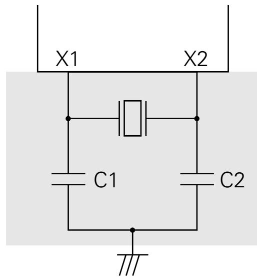
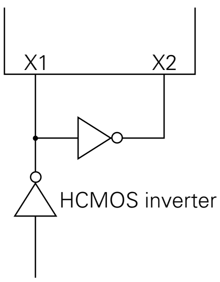
6. ELECTRICAL SPECIFICATIONS

Absolute maximum ratings (T_A = 25 °C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}		–0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD} + 0.5	V
	AV_{SS}		–0.5 to +0.5	V
Input voltage	V_I		–0.5 to V_{DD} + 0.5	V
Output voltage	V_O		–0.5 to V_{DD} + 0.5	V
Output current, low	I_{OL}	Each output pin	4.0	mA
		Total (all pins)	100	mA
Output current, high	I_{OH}	Each output pin	–2.0	mA
		Total (all pins)	–50	mA
A/D converter reference input voltage	V_{AREF}		–0.5 to AV_{DD} + 0.3	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

★ **Caution If the absolute maximum rating for any of the above parameters is exceeded even momentarily, it may adversely affect the quality of this product. In other words, these absolute maximum ratings have been set to prevent physical damage to the product. Do not use the product in such a way as to exceed any of these ratings.**

Oscillation characteristics (T_A = –40 to +85 °C, V_{DD} = AV_{DD} + 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V, V_{DD} – 0.8 V ≤ AV_{DD} ≤ V_{DD}, 3.4 V ≤ V_{AREF} ≤ AV_{DD})

Resonator	Recommended circuit	Parameter	Condition	MIN.	MAX.	Unit
Ceramic resonator or crystal resonator(Note)		Oscillation frequency (f_{XX})	A/D converter not used	4	15	MHz
			A/D converter used	5.8	15	MHz
External clock		X1 input frequency (f_X)	A/D converter not used	4	15	MHz
			A/D converter used	5.8	15	MHz
		X1 input rise, fall time (t_r, t_f)		0	20	ns
		X1 input low-level and high-level width ($t_{\varnothing L}$, $t_{\varnothing H}$)		20	250	ns

Cautions 1. The oscillation circuit should be placed as close to the X1 and X2 pins as possible.
2. Do not place other signal lines in the shaded area.

Note When using a crystal resonator, the following external capacitance values are recommended.
C1 = C2 = 10 pF

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V.			10	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

DC characteristics (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	All except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, and AN4 to AN7	0		0.8	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, and AN4 to AN7	0		$0.2V_{DD}$	V
Input voltage, high	V_{IH1}	All except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to AN7, X1, and X2	2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to AN7, X1, and X2	$0.8V_{DD}$		V_{DD}	V
Output voltage, low	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output voltage, high	V_{OH}	I_{OH} = –1.0 mA	V_{DD} - 1.0			V
		I_{OH} = –100 μA	V_{DD} - 0.5			V
Input current	I_I	INT1 **(Note 1)**, TI (PC3) **(Note 2)**; 0 V ≤ V_I ≤ V_{DD}			±200	μA
Input leakage current	I_{LI}	All except INT1, TI (PC3), and AN0 to AN7; 0 V ≤ V_I ≤ V_{DD}			±10	μA
		AN7-0; 0 V ≤ V_I ≤ V_{DD}			±1	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}			±10	μA
AV_{DD} supply current	AI_{DD1}	Operation mode; f_{XX} = 15 MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA
V_{DD} supply current	I_{DD1}	Operation mode; f_{XX} = 15 MHz		13	25	mA
	I_{DD2}	HALT mode; f_{XX} = 15 MHz		7	13	mA
Data retention voltage	V_{DDDR}	Hardware/software STOP mode	2.5			V
Data retention current	I_{DDDR}	Hardware/software STOP mode **(Note 3)**; V_{DDDR} = 2.5 V		1	15	μA
		Hardware/software STOP mode **(Note 3)**; V_{DDDR} = 5 V ± 10 %		10	50	μA
Pull-up resistor **(Note 4)**	R_L	Ports A, B, and C; 3.5 V ≤ V_{DD} ≤ 5.5 V, V_I = 0 V	17	27	75	kΩ

Caution For details of the hardware STOP mode, see the 87AD Series μPD78C18 User's Manual.

Notes
1. Assumes self-bias is set from the ZCM register
2. When control mode is set from the MCC register, assumes self-bias is set from the ZCM register
3. Assumes self-bias is not set
4. μPD78C11A(A) and 78C12A(A) only

AC characteristics (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ±10%, V_{SS} = AV_{SS} = 0 V)

Read/write operation:

Parameter	Symbol	Condition	MIN.	MAX.	Unit
X1 input cycle time	t_{CYC}		66	250	ns
Address setup time (to ALE ↓)	t_{AL}	f_{XX} = 15 MHz, C_L = 100 pF	30		ns
Address hold time (to ALE ↓)	t_{LA}		35		ns
Address to $\overline{RD}$ ↓ delay time	t_{AR}		100		ns
$\overline{RD}$ ↓ to address float time	t_{AFR}	C_L = 100 pF		20	ns
Address to data input time	t_{AD}	f_{XX} = 15 MHz, C_L = 100 pF		250	ns
ALE ↓ to data input time	t_{LDR}			135	ns
$\overline{RD}$ ↓ to data input time	t_{RD}			120	ns
ALE ↓ to $\overline{RD}$ ↓ delay time	t_{LR}		15		ns
Data hold time (to $\overline{RD}$ ↑)	t_{RDH}	C_L = 100 pF	0		ns
$\overline{RD}$ ↑ to ALE ↑ delay time	t_{RL}	f_{XX} = 15 MHz, C_L = 100 pF	80		ns
$\overline{RD}$ width low	t_{RR}	Data read f_{XX} = 15 MHz, C_L = 100 pF	215		ns
		Opcode fetch f_{XX} = 15 MHz, C_L = 100 pF	415		ns
ALE width high	t_{LL}	f_{XX} = 15 MHz, C_L = 100 pF	90		ns
$\overline{M1}$ setup time (to ALE ↓)	t_{ML}	f_{XX} = 15 MHz	30		ns
$\overline{M1}$ hold time (to ALE ↓)	t_{LM}		35		ns
$\overline{IO}$/M setup time (to ALE ↓)	t_{IL}		30		ns
$\overline{IO}$/M hold time (to ALE ↓)	t_{LI}		35		ns
Address to $\overline{WR}$ ↓ delay time	t_{AW}	f_{XX} = 15 MHz, C_L = 100 pF	100		ns
ALE ↓ to data output time	t_{LDW}			180	ns
$\overline{WR}$ ↓ to data output time	t_{WD}	C_L = 100 pF		100	ns
ALE ↓ to $\overline{WR}$ ↓ delay time	t_{LW}	f_{XX} = 15 MHz, C_L = 100 pF	15		ns
Data setup time (to $\overline{WR}$ ↑)	t_{DW}		165		ns
Data hold time (to $\overline{WR}$ ↑)	t_{WDH}		60		ns
$\overline{WR}$ ↑ to ALE ↑ delay time	t_{WL}		80		ns
$\overline{WR}$ width low	t_{WW}		215		ns

Serial operation:

Parameter	Symbol	Condition		MIN.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{CYK}	$\overline{SCK}$ input	Note 1	800		ns
			Note 2	400		ns
		$\overline{SCK}$ output		1.6		μs
$\overline{SCK}$ width low	t_{KKL}	$\overline{SCK}$ input	Note 1	335		ns
			Note 2	160		ns
		$\overline{SCK}$ output		700		ns
$\overline{SCK}$ width high	t_{KKH}	$\overline{SCK}$ input	Note 1	335		ns
			Note 2	160		ns
		$\overline{SCK}$ output		700		ns
RxD setup time (to $\overline{SCK}$ ↑)	t_{RXK}	Note 1		80		ns
RxD hold time (to $\overline{SCK}$ ↑)	t_{KRX}	Note 1		80		ns
$\overline{SCK}$ ↓ to TxD delay time	t_{KTX}	Note 1			210	ns

Notes 1. When in asynchronous mode with X1 clock rate, synchronous mode, or I/O interface mode

2. When in asynchronous mode with X16 or X64 clock rate

Remark The values shown in the above table are when f_{XX} = 15 MHz and C_L = 100 pF.

Zero-cross characteristics:

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Zero-cross detection input	V_{ZX}	AC-coupled 60-Hz sine wave	1	1.8	VAC_{P-P}
Zero-cross accuracy	A_{ZX}			±135	mV
Zero-cross detection input frequency	f_{ZX}		0.05	1	kHz

Other operation:

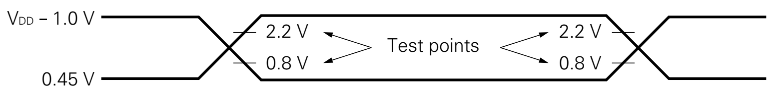
Parameter	Symbol	Condition	MIN.	MAX.	Unit
TI width high, low	t_{TIH}, t_{TIL}		6		t_{CYC}
CI width high, low	t_{CI1H}, t_{CI1L}	Event counter mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse-width measurement mode	48		t_{CYC}
$\overline{NMI}$ width high, low	t_{NIH}, t_{NIL}		10		μs
INT1 width high, low	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ width high, low	t_{I2H}, t_{I2L}		36		t_{CYC}
AN4 to AN7 width high, low	t_{ANH}, t_{ANL}		36		t_{CYC}
$\overline{RESET}$ width high, low	t_{RSH}, t_{RSL}		10		μs

A/D converter characteristics **(T_A = –40 to +85 °C, V_{DD} = +5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V, V_{DD} – 0.5 V ≤ AV_{DD} ≤ V_{DD}, 3.4 V ≤ V_{AREF} ≤ AV_{DD})**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution			8			Bits
Absolute accuracy (Note)		3.4 V ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 170 ns			±0.8 %	FSR
		4.0 ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 170 ns			±0.6 %	FSR
		T_A = –10 to +70 °C, 4.0 ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 170 ns			±0.4 %	FSR
Conversion time	t_{CONV}	66 ns ≤ t_{CYC} ≤ 110 ns	576			t_{CYC}
		110 ns ≤ t_{CYC} ≤ 170 ns	432			t_{CYC}
Sampling time	t_{SAMP}	66 ns ≤ t_{CYC} ≤ 110 ns	96			t_{CYC}
		110 ns ≤ t_{CYC} ≤ 170 ns	72			t_{CYC}
Analog input voltage	V_{IAN}	AN0 to AN7 (including unused pins)	–0.3		V_{AREF} + 0.3	V
Analog input impedance	R_{AN}			50		MΩ ★
Reference voltage	V_{AREF}		3.4		AV_{DD}	V
V_{AREF} current	I_{AREF1}	Operation mode		1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} supply current	AI_{DD1}	Operation mode; f_{XX} = 15 MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA

Note Quantizing error (±1/2 LSB) is not included.

AC timing test points



Calculation formulas for AC characteristics dependent on t_{CYC}

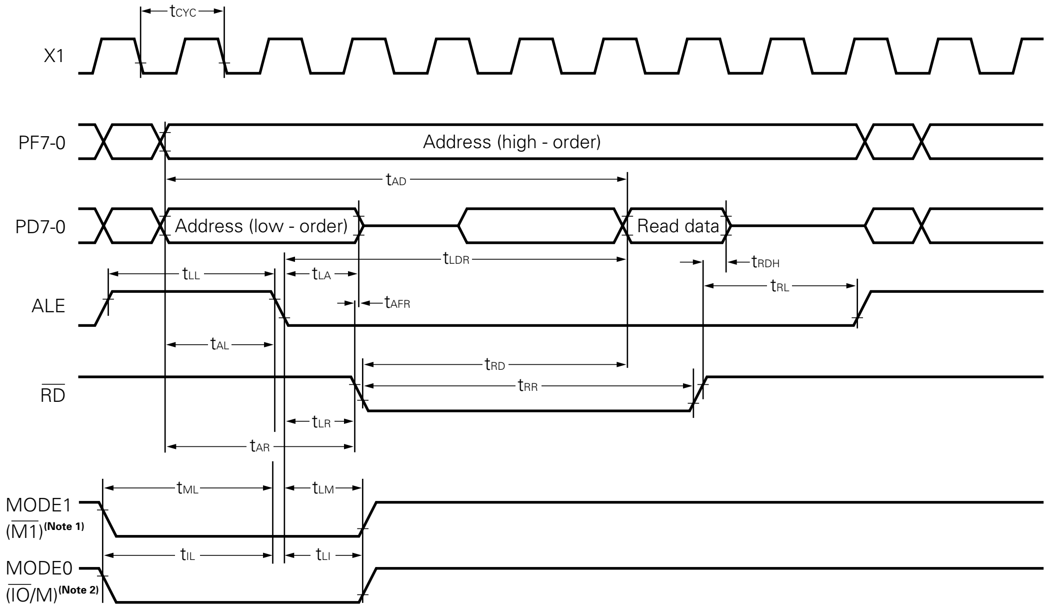
Symbol	Calculation formula	MIN/MAX.	Unit
t_{AL}	2T – 100	MIN.	ns
t_{LA}	T – 30	MIN.	ns
t_{AR}	3T – 100	MIN.	ns
t_{AD}	7T – 220	MAX.	ns
t_{LDR}	5T – 200	MAX.	ns
t_{RD}	4T – 150	MAX.	ns
t_{LR}	T – 50	MIN.	ns
t_{RL}	2T – 50	MIN.	ns
t_{RR}	4T – 50 (Data read)	MIN.	ns
	7 T – 50 (Opcode fetch)		
t_{LL}	2T – 40	MIN.	ns
t_{ML}	2T – 100	MIN.	ns
t_{LM}	T – 30	MIN.	ns
t_{IL}	2T – 100	MIN.	ns
t_{LI}	T – 30	MIN.	ns
t_{AW}	3T – 100	MIN.	ns
t_{LDW}	T + 110	MAX.	ns
t_{LW}	T – 50	MIN.	ns
t_{DW}	4T – 100	MIN.	ns
t_{WDH}	2T – 70	MIN.	ns
t_{WL}	2T – 50	MIN.	ns
t_{WW}	4T – 50	MIN.	ns
t_{CYK}	12T ($\overline{SCK}$ input)**(Note 1)** /6T ($\overline{SCK}$ input)**(Note 2)**	MIN.	ns
	24T ($\overline{SCK}$ output)		
t_{KKL}	5T + 5 ($\overline{SCK}$ input)**(Note 1)** /2.5T + 5 ($\overline{SCK}$ input)**(Note 2)**	MIN.	ns
	12T – 100 ($\overline{SCK}$ output)		
t_{KKH}	5T + 5 ($\overline{SCK}$ input)**(Note 1)** /2.5T + 5 ($\overline{SCK}$ input)**(Note 2)**	MIN.	ns
	12T – 100 ($\overline{SCK}$ output)		

Notes 1. When in asynchronous mode with X1 clock rate, synchronous mode, or I/O interface mode
2. When in asynchronous mode with X16 or X64 clock rate

Cautions 1. T = t_{CYC} = 1/f_{XX}
2. The items not included in this list are independent of oscillation frequency (f_{XX}).

Timing waveforms

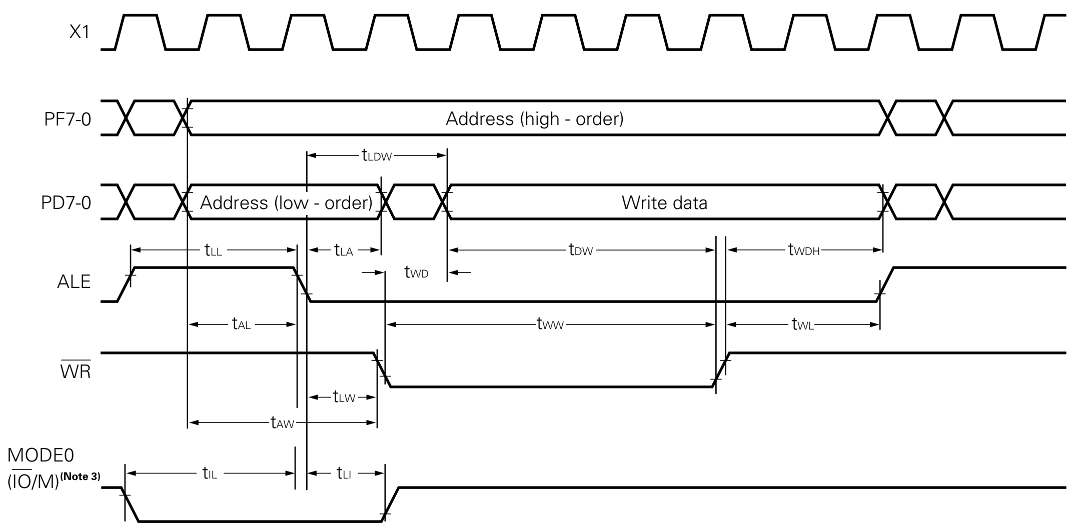
Read operation



Notes 1. The $\overline{\text{M1}}$ signal is output to the MODE1 pin during the first opcode fetch cycle when the MODE1 pin is pulled up.

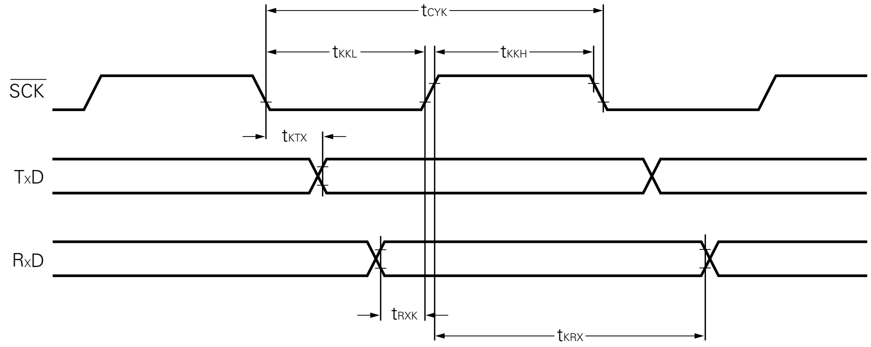
2. The $\overline{\text{IO}}$/M signal is output to the MODE0 pin during the sr to sr2 register read cycle when the MODE0 pin is pulled up.

Write operation

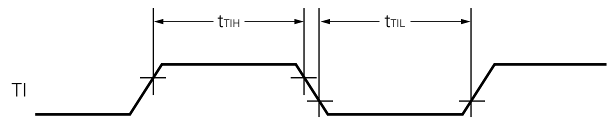


Notes 3. The $\overline{\text{IO}}$/M signal is output to the MODE0 pin during the sr to sr2 register write cycle when the MODE0 pin is pulled up.

Serial operation

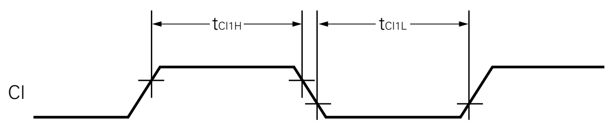


Timer input timing

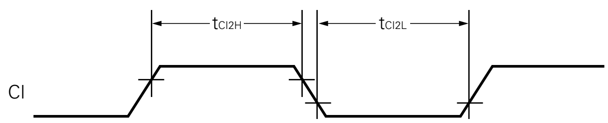


Timer/event counter input timing

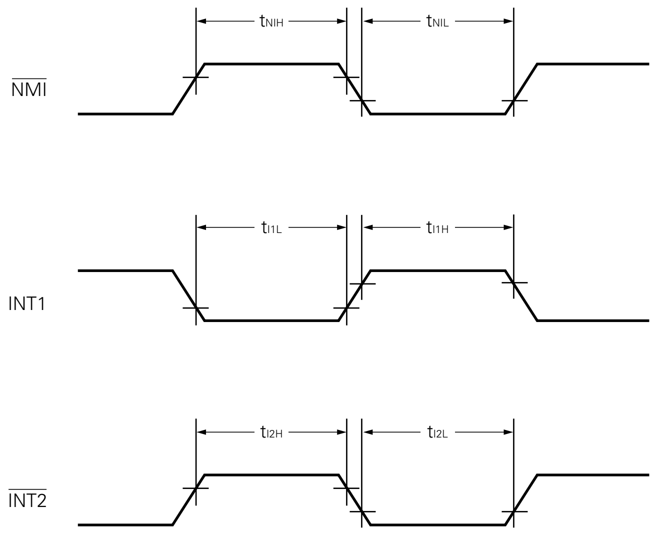
Event counter mode



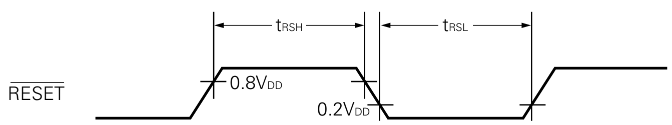
Pulse-width measurement mode



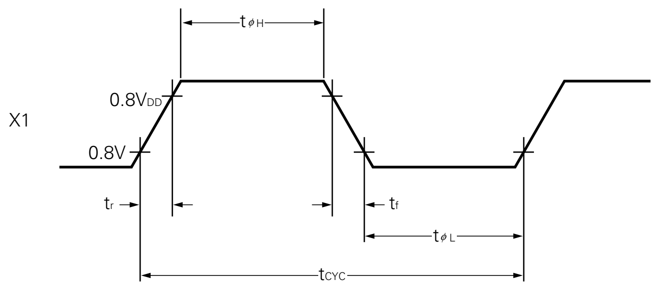
Interrupt input timing



Reset input timing



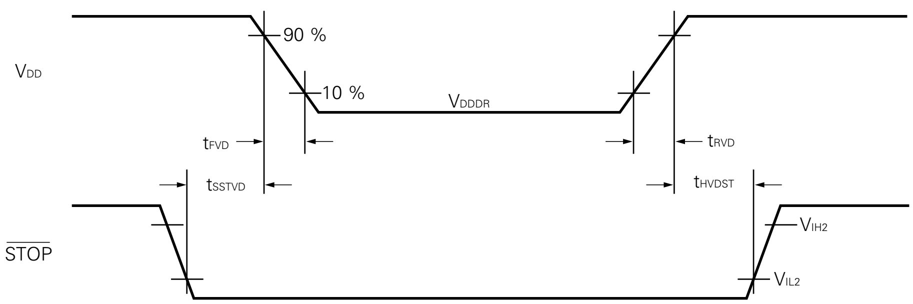
External clock timing



Data memory STOP mode low-voltage data retention characteristic (T_A = –40 to +85 °C)

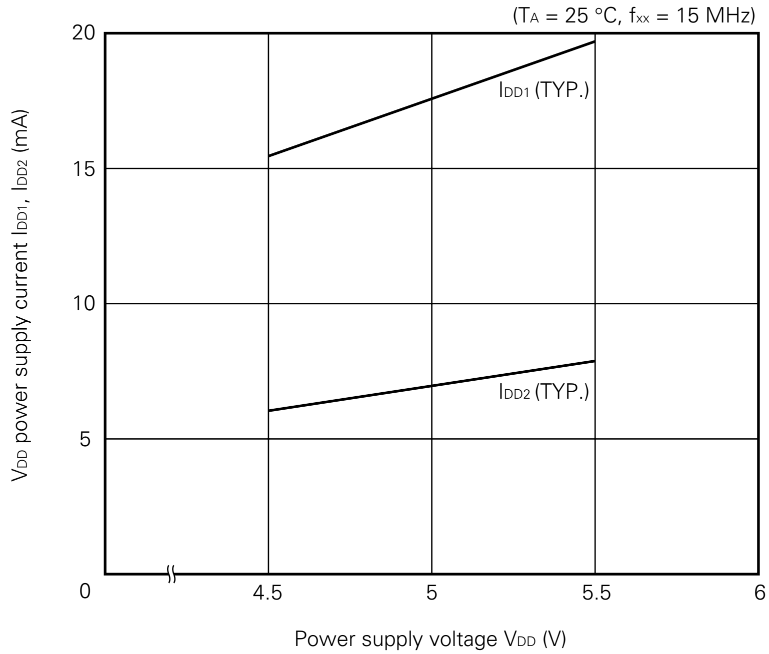
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		2.5		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.5 V		1	15	μA
★		V_{DDDR} = 5 V ± 10 %		10	50	μA
V_{DD} rise, fall time	t_{RVD}, t_{FVD}		200			μs
$\overline{\text{STOP}}$ setup time (to V_{DD})	t_{SSTVD}		12T + 0.5			μs
$\overline{\text{STOP}}$ hold time (from V_{DD})	t_{HVDST}		12T + 0.5			μs

Data retention timing

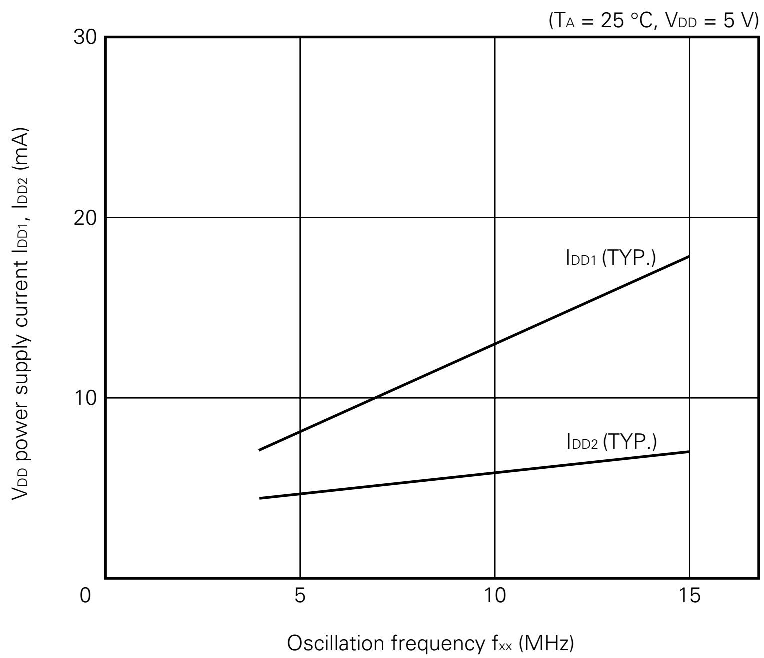


7. CHARACTERISTIC CURVES (REFERENCE VALUES)

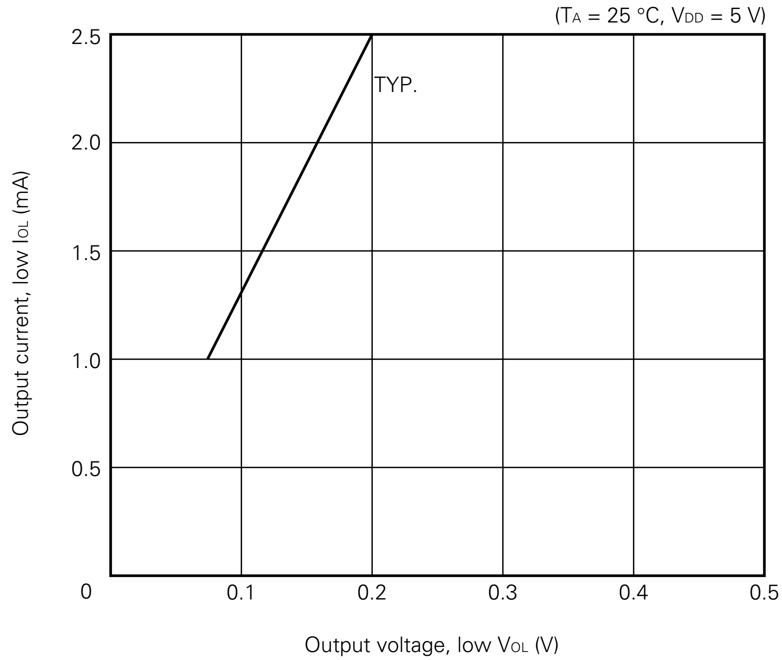
I_{DD1}, I_{DD2} vs V_{DD}



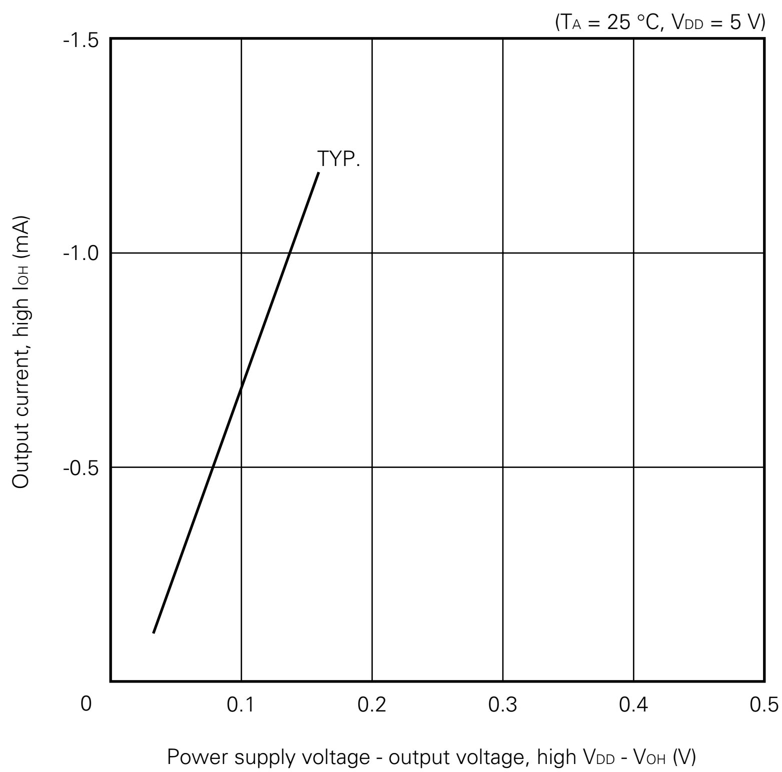
I_{DD1}, I_{DD2} vs f_{xx}



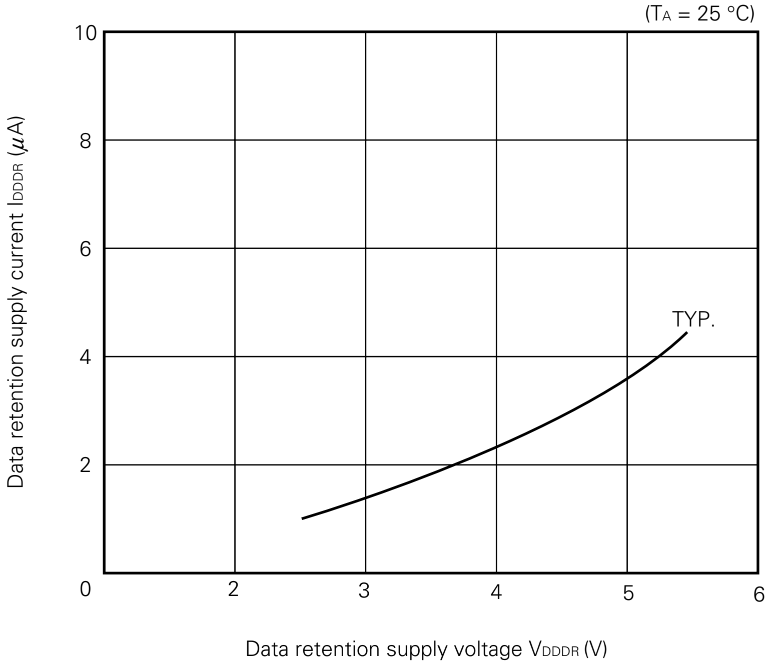
I_{OL} vs V_{OL}



I_{OH} vs V_{OH}

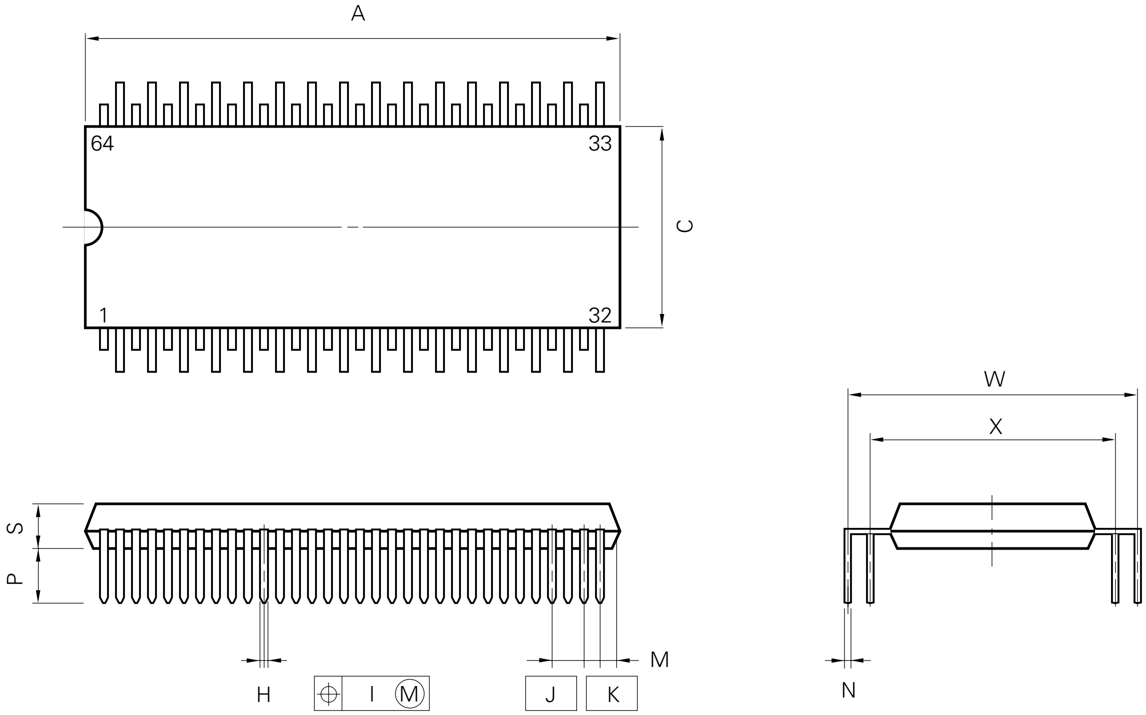


I_{DDDR} vs V_{DDDR}



8. PACKAGE DRAWINGS

64 PIN PLASTIC QUIP



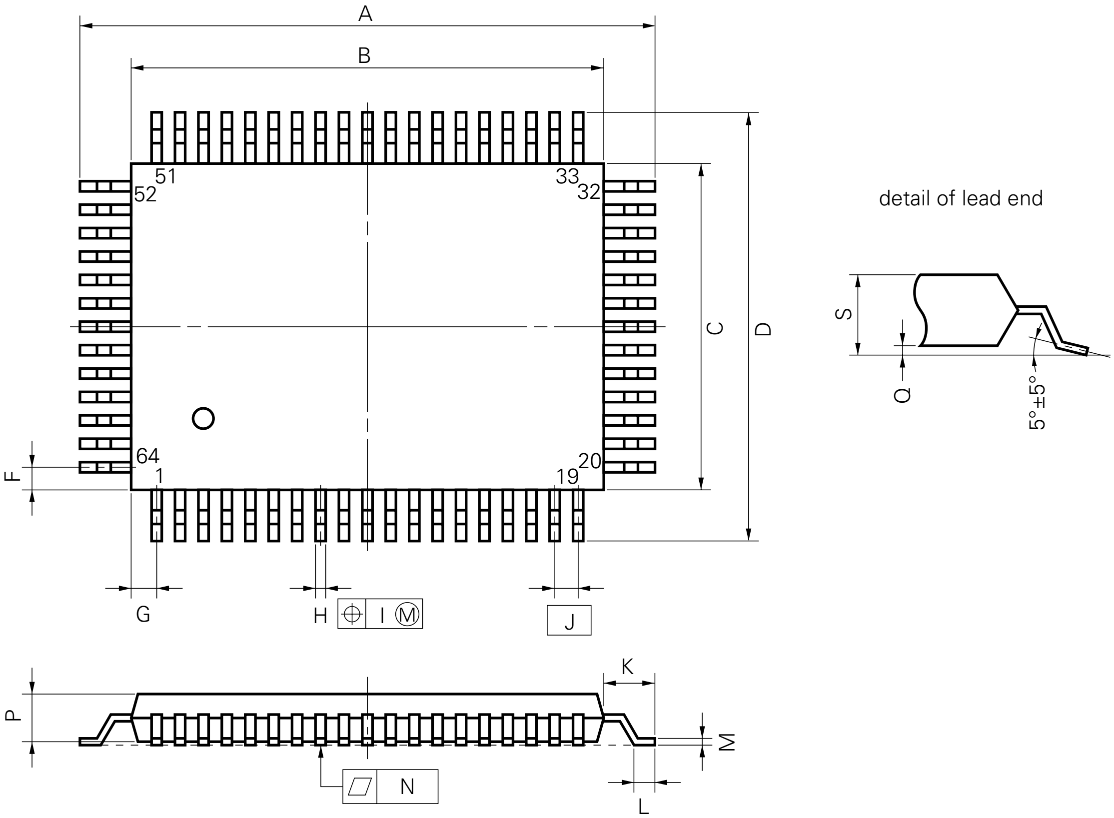
P64GQ-100-36

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$41.5^{+0.3}_{-0.2}$	$1.634^{+0.012}_{-0.008}$
C	16.5	0.650
H	$0.50^{\pm0.10}$	$0.020^{+0.004}_{-0.005}$
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0.050 (T.P.)
M	$1.1^{+0.25}_{-0.15}$	$0.043^{+0.011}_{-0.006}$
N	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
P	$4.0^{\pm0.3}$	$0.157^{+0.013}_{-0.012}$
S	$3.6^{\pm0.1}$	$0.142^{+0.004}_{-0.005}$
W	$24.13^{\pm1.05}$	$0.950^{\pm0.042}$
X	$19.05^{\pm1.05}$	$0.750^{\pm0.042}$

64 PIN PLASTIC QFP (14×20)



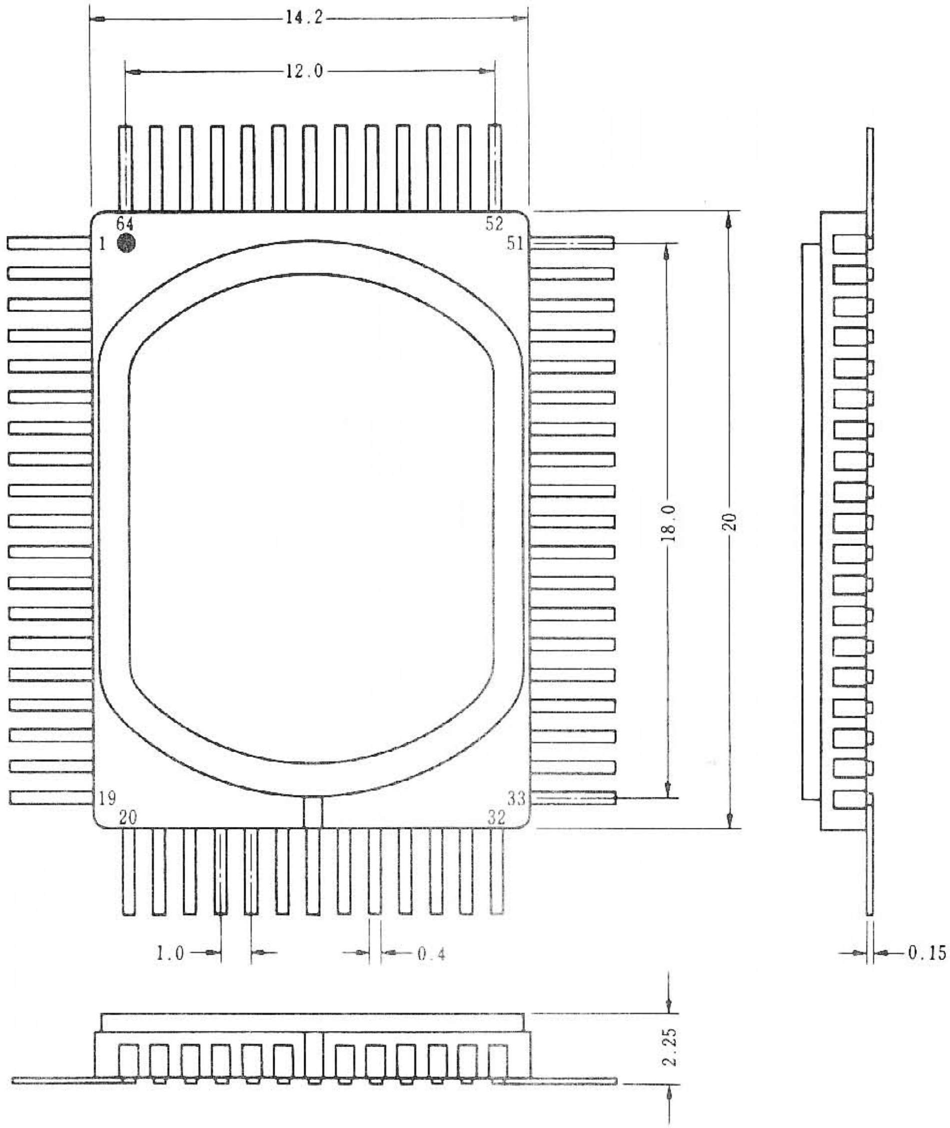
P64GF-100-3B8,3BE,3BR-1

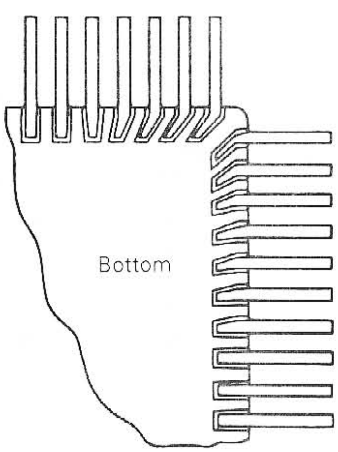
NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

64-pin ceramic QFP for engineering samples (Reference drawing) (unit: mm)

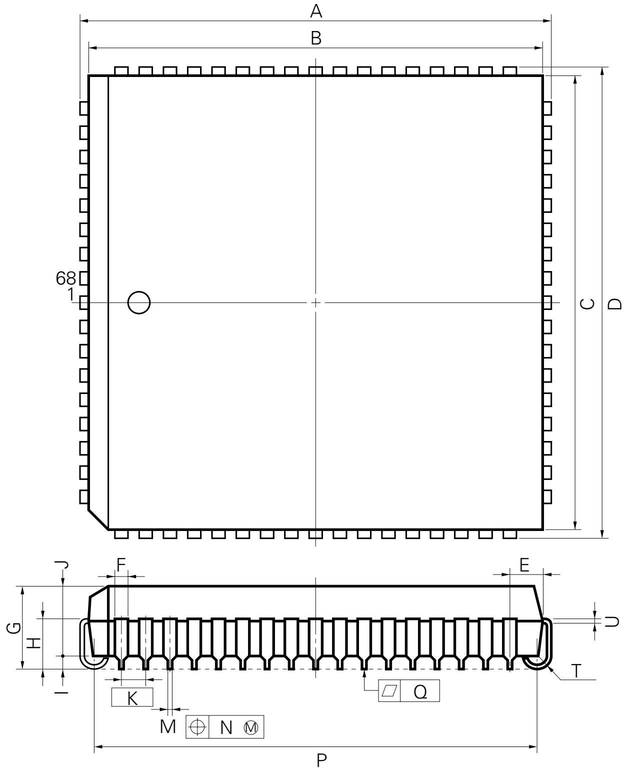




Cautions

1. The metal cover is connected to pin 26. Note that this is the Vss (GND) level.
2. The leads on the bottom surface are formed obliquely.
3. The length of the leads is not defined because the cutting of the lead tips is not controlled during the manufacturing process.

68 PIN PLASTIC QFJ (□950 mil)



P68L-50A1-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	25.2±0.2	0.992±0.008
B	24.20	0.953
C	24.20	0.953
D	25.2±0.2	0.992±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±1.0	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	23.12±0.20	$0.910^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

★ ## 9. RECOMMENDED SOLDERING CONDITIONS

Use the following recommended soldering conditions when solder-mounting the μPD78C10A(A), 78C11A(A), or 78C12A(A).

For details of recommended soldering conditions, see the **Semiconductor Device Mounting Technology Manual (IEI-1207)** in the information materials.

Consult your local NEC sales representative concerning soldering methods and conditions other than those recommended.

Table 9-1. Soldering Conditions for Surface Mounting Types

(1) μPD78C10AGF(A)-3BE : 64-pin plastic QFP (14 x 20 mm)
μPD78C11AGF(A)-xxx-3BE : 64-pin plastic QFP (14 x 20 mm)

Soldering method	Soldering conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Time: 30 seconds max. (210 °C min.), Number of operations: 2 max. **<Cautions>** (1) Do not start the second reflow until the device has cooled to normal temperature after the first reflow. (2) Do not use water for flux cleaning after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (200 °C min.), Number of operations: 2 max. **<Cautions>** (1) Do not start the second reflow until the device has cooled to normal temperature after the first reflow. (2) Do not use water for flux cleaning after the first reflow.	VP15-00-2
Wave soldering	Solder bath temperature: 260 °C max., Time: 10 seconds max., Number of operations: 1 Preheating temperature: 120 °C max. (package surface temperature)	WS60-00-1
Pin partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per device side)	–

Caution Do not use different soldering methods together (except when one method is pin partial heating).

(2) μPD78C12AGF(A)-xxx-3BE: 64-pin plastic QFP (14 x 20 mm)

Soldering method	Soldering conditions	Symbol
Infrared ray reflow	Package peak temperature: 230 °C, Time: 30 seconds max. (210 °C min.), Number of operations: 1	IR30-00-1
VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (200 °C min.), Number of operations: 1	VP15-00-1
Wave soldering	Solder bath temperature: 260 °C max., Time: 10 seconds max., Number of operations: 1 Preheating temperature: 120 °C max. (package surface temperature)	WS60-00-1
Pin partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per device side)	–

Caution Do not use different soldering methods together (except when one method is pin partial heating).

(3) μPD78C10AL(A) : 68-pin plastic QFJ (950 x 950 mil)
μPD78C11AL(A)-xxx : 68-pin plastic QFJ (950 x 950 mil)
μPD78C12AL(A)-xxx : 68-pin plastic QFJ (950 x 950 mil)

Soldering method	Soldering conditions	Symbol
Infrared ray reflow	Package peak temperature: 230 °C, Time: 3 seconds max. (210 °C min.), Number of operations: 1	IR30-00-1
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200 °C min.), Number of operations: 1	VP15-00-1
Pin partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per device side)	—

Caution Do not use different soldering methods together (except when one method is pin partial heating).

Table 9-2. Soldering Conditions for Through Hole Types

μPD78C10AGQ(A)-36 : 64-pin plastic QUIP
μPD78C11AGQ(A)-xxx-36 : 64-pin plastic QUIP
μPD78C12AGQ(A)-xxx-36 : 64-pin plastic QUIP

Soldering method	Soldering conditions
Wave soldering (pins only)	Solder bath temperature: 260 °C max., Time: 10 seconds max.
Pin partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per one pin)

Caution Perform wave soldering on pins only and do not allow the solder to make direct contact with the body.

★ **APPENDIX DEVELOPMENT TOOLS**

The following development tools are available for system development using the μPD78C10A(A), 78C11A(A), and 78C12A(A).

Language processor

87AD Series relocatable assembler (RA87)	This program converts symbolic (mnemonic) programs into object code that is executable by microcomputers. In addition, it includes functions for automatic generation of symbol tables and optimum processing of branch instructions.			
	Host machine	Operating System	Medium	Ordering code (product name)
	PC-9800 Series	MS-DOS™ Ver.2.11 to Ver.5.00A (Note)	3.5-inch 2HD	μS5A13RA87
			5-inch 2HD	μS5A10RA87
	IBM PC/AT™	PC DOS™ (Ver.3.1)	3.5-inch 2HC	μS7B13RA87
			5-inch 2HC	μS7B10RA87

PROM programming tools

Hard-ware	PG-1500		This is a PROM programmer that, when connected to an auxiliary board and a (separately sold) programmer adapter, can be operated as a stand-alone device or from a host machine for PROM programming of single-chip microcomputers that have on-chip PROM. It can also be used to program PROM devices in sizes ranging from 256 Kbits to 4 Mbits.			
	PA-78CP14GQ		This is the PROM programmer adapter for the μPD78CP14(A), which is connected to the PG-1500.			
		PA-78CP14GQ	μPD78CP14G(A)-36,			
Soft-ware	PG-1500 controller		This controller controls the PG-1500 from a host machine that is connected to the PG-1500 via a serial or parallel interface.			
			Host machine	Operating System	Medium	Ordering code (product name)
			PC-9800 Series	MS-DOS Ver.2.11 to Ver.5.00A (Note)	3.5-inch 2HD	μS5A13PG1500
					5-inch 2HD	μS5A10PG1500
			IBM PC/AT	PC DOS (Ver.3.1)	5-inch 2HC	μS7B10PG1500

Note This software does not include a task swapping function, although a task swapping function is provided in Ver.5.00/5.00A.

Remark Operation of the assembler and PG-1500 controller is guaranteed only on the host machines and operating systems described above.

Debugging tools

An in-circuit emulator (IE-78C11-M) is available as a program debugging tool for the μPD78C10A(A), 78C11A(A), and 78C12A(A). The system configuration is shown below.

<table>
<tr><td>Hard-
ware</td><td>IE-78C11-M</td><td colspan="4">The IE-78C11-M is an in-circuit emulator that supports the 87AD Series. It enables efficient debugging when connected to a host machine.</td></tr>
<tr><td rowspan="5">Soft-
ware</td><td rowspan="5">IE-78C11-M control program
(IE controller)</td><td colspan="4">This controller controls the IE-78C11-M from a host machine that is connected to the IE-78C11-M via the RS-232-C.</td></tr>
<tr><td>Host machine</td><td>Operating System</td><td>Medium</td><td>Ordering code
(product name)</td></tr>
<tr><td rowspan="2">PC-9800
Series</td><td rowspan="2">MS-DOS
[Ver.2.11
to
Ver.3.30D]</td><td>3.5-inch 2HD</td><td>μS5A13IE78C11</td></tr>
<tr><td>5-inch 2HD</td><td>μS5A10IE78C11</td></tr>
<tr><td>IBM PC/AT</td><td>PC DOS
(Ver.3.1)</td><td>5-inch 2HC</td><td>μS7B10IE78C11</td></tr>
</table>

Remark Operation of the IE controller is guaranteed only on the host machines and operating systems described above.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

MS-DOS is a trademark of Microsoft Corporation.

PC/AT and PC DOS are trademarks of IBM Corporation.

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License not needed :	μPD78C10AGF(A)-3BE, 78C10AGQ(A)-36, 78C10AL(A)
The customer must judge the need for license :	μPD78C11AGF(A)-xxx-3BE, 78C11AGQ(A)-xxx-36, 78C11AL(A)-xxx, μPD78C12AGF(A)-xxx-3BE, 78C12AGQ(A)-xxx-36, 78C12AL(A)-xxx