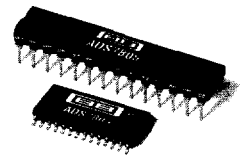
BURR-BROWN®



ADS7805

DEMO BOARD AVAILABLE
See Appendix A

www.burr-brown.com/databook/ADS7805.html

16-Bit 10µs Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

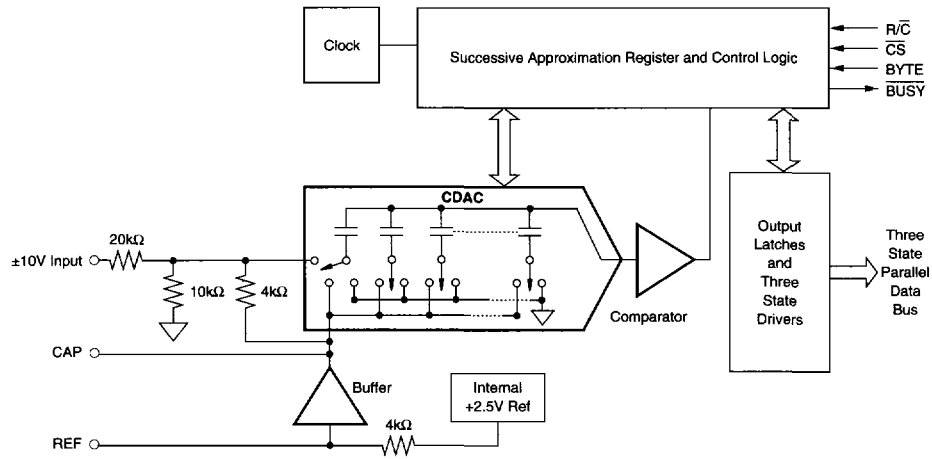
- 100kHz min SAMPLING RATE
- STANDARD ±10V INPUT RANGE
- 86dB min SINAD WITH 20kHz INPUT
- ±3.0 LSB max INL
- DNL: 16-bits "No Missing Codes"
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7804
- USES INTERNAL OR EXTERNAL REFERENCE
- FULL PARALLEL DATA OUTPUT
- 100mW max POWER DISSIPATION
- 28-PIN 0.3" PLASTIC DIP AND SOIC

DESCRIPTION

The ADS7805 is a complete 16-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7805 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide an industry-standard ±10V input range, while the innovative design allows operation from a single +5V supply, with power dissipation under 100mW.

The 28-pin ADS7805 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –25°C to +85°C range.



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SPECIFICATIONS

ELECTRICAL

T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7805P, U			ADS7805PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Ranges			±10V			*		V
Impedance			23			*		kΩ
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Cycle	Acquire and Convert			10			*	µs
Throughput Rate		100			*			kHz
DC ACCURACY								
Integral Linearity Error				±4			±3	LSB[1]
No Missing Codes		15			16			Bits
Transition Noise[2]			1.3			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]				±10			*	mV
Bipolar Zero Error Drift			±2			*		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±8			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 20kHz	90			94			dB[5]
Total Harmonic Distortion	f_{IN} = 20kHz			–90			–94	dB
Signal-to-(Noise+Distortion)	f_{IN} = 20kHz	83			86			dB
	–60dB Input		30			32		dB
Signal-to-Noise	f_{IN} = 20kHz	83			86			dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Transient Response	FS Step			2			*	µs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer.)			1			*		µA
Internal Reference Drift			8			*		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS				Parallel 16-bits				
Data Format				Binary Two's Complement				
Data Coding								
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				83			*	ns
Bus Relinquish Time				83			*	ns

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7805P, U			ADS7805PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.3			*		mA
I_{ANA}			16			*		mA
Power Dissipation	f_S = 100kHz			100			*	mW
TEMPERATURE RANGE								
Specified Performance		–25		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

* Specifications same as ADS7805P, U.

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±10V input ADS7805, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN} ..... ±25V
CAP ..... $+V_{ANA}$ +0.3V to AGND2 –0.3V
REF ..... Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, AGND2 ..... ±0.3V
V_{ANA} 7V
V_{DIG} to V_{ANA} ..... +0.3V
V_{DIG} 7V
Digital Inputs ..... –0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature ..... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) ..... +300°C

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADS7805P	Plastic DIP	246
ADS7805PB	Plastic DIP	246
ADS7805U	SOIC	217
ADS7805UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ORDERING INFORMATION

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7805P	±4	83	–25°C to +85°C	Plastic DIP
ADS7805PB	±3	86	–25°C to +85°C	Plastic DIP
ADS7805U	±4	83	–25°C to +85°C	SOIC
ADS7805UB	±3	86	–25°C to +85°C	SOIC

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog Input. See Figure 7.
2	AGND1		Analog Ground. Used internally as ground reference point.
3	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
4	CAP		Reference Buffer Capacitor. 2.2µF tantalum capacitor to ground.
5	AGND2		Analog Ground.
6	D15 (MSB)	O	Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
7	D14	O	Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
8	D13	O	Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D12	O	Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D11	O	Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D10	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D9	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D8	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D7	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D6	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D5	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D4	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	D3	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	D2	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	D1	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	O	Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	BYTE	I	Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH).
24	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
25	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion.
26	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
27	V_{ANA}		Analog Supply Input. Nominally +5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}		Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ V_{ANA}.

TABLE I. Pin Assignments.

PIN CONFIGURATION