Rockwell

RC9696/14 V.32 bis 14400 bps 2-Wire Modem

INTRODUCTION

The Rockwell RC9696/14 is a 14400 bps 2-wire, full-duplex, synchronous/asynchronous, V.32 bis modem data pump module. It operates over the public switched telephone network (PSTN) through the appropriate line termination.

The modem satisfies the requirements specified in CCITT recommendations V.32 bis, V.32, V.17/V.33, V.29, V.27 ter, V.22 bis, V.22, V.23, and V.21; is compatible with Bell 212A and Bell 103 modems; and supports Group 3 facsimile (fax).

The RC9696/14 can operate at 14400, 12000, 9600, 7200, 4800, 2400, 1200, 600, or 300 bps depending upon the selected configuration.

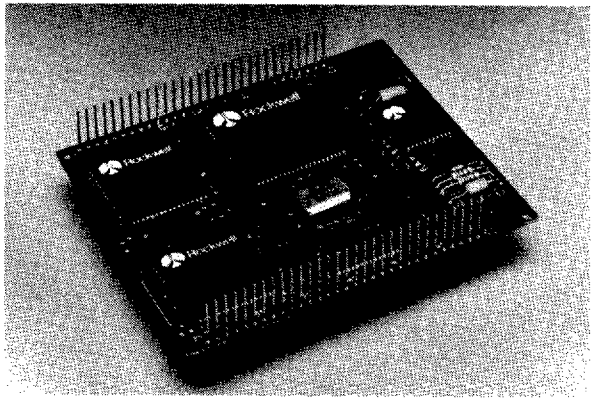
The RC9696/14 is designed for use in high speed data applications. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements.

The dual-in-line pin (DIP) connection allows direct installation onto a host module. The modem's small size (less than 13 square inches), low power consumption, serial/parallel host interface, and DIP connection simplify system development and reduce system production cost.

Detailed hardware and software interface information is described in the RC9696/14 and RC1496/14 Modem Designer's Guide (Order No. 856).

FEATURES

- 2-wire full-duplex compatibilities
  - —CCITT V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21
  - —Bell 212A and 103
- 2-wire half-duplex compatibilities
  - —CCITT V.17/V.33, V.29, V.27 ter, and V.21 channel 2
- Group 3 (G3) facsimile send/receive compatible
- Parallel synchronous
- Serial synchronous
- Serial asynchronous up to 9600 bps
- Trellis-coded modulation (TCM) at 14400, 12000, 9600, and 7200 bps
- Programmable near and far end echo cancellation
- Bulk delay for satellite transmission
- Auto-dial and auto-answer capability
- TTL and CMOS compatible DTE interface
  - —CCITT V.24 (RS-232-C) (data/control)
  - —Microprocessor bus (data/configuration/control)
- Dynamic Range: –43 dBm to 0 dBm
- Programmable compromise equalizer in transmitter
- Automatic adaptive equalizer in receiver
- Diagnostic capability
- V.13 signalling
- V.54 Inter-DCE signalling
- V.54 local analog and remote digital loopback
- Small Size: 82 mm x 100 mm (3.23 in. x 3.94 in.)
- Low power consumption: 1.9 W (typical)



RC9696/14 Modem

Document No. 29200N71 | **Data Sheet (Preliminary)** | **Order No. MD71 Rev. 2, October 1991**

TECHNICAL SPECIFICATIONS

CONFIGURATIONS, SIGNALING RATES AND DATA RATES

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

TONE GENERATION

Under control of the host processor, the modem can generate single or dual voice-band tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of ±0.01%. Tones over 3000 Hz are attenuated. DTMF tone generation allows the modem to operate as a programmable DTMF dialer.

DATA ENCODING

The data encoding conforms to CCITT recommendations V.32 bis, V.32, V.17/V.33, V.29, V.27 ter, V.22 bis, V.22, V.23, and V.21; and to Bell 212A and 103.

EQUALIZERS

Equalization functions are provided that improve performance when operating over low quality lines.

Compromise Equalizer: A 40-tap digital finite impulse response (FIR) filter in the transmitter provides compromise equalization. The filter taps can be changed in DSP RAM for varying line conditions. The default equalizer tap coefficients compensate for half the amplitude distortion of a 3002 unconditioned line and for half the group delay distortion of a 3002 unconditioned line. The filter can be enabled or disabled using the CEQ bit in the Chip 0 interface memory.

A 40-tap digital FIR filter in the receiver provides compromise equalization for V.23 1200 and 600 configurations only. The filter is identical to the transmitter compromise filter and can be programmed via the DSP RAM. This feature is enabled and disabled using the CEQ23 bit in the Chip 1 interface memory.

Automatic Adaptive Equalizer: A 64-tap automatic adaptive equalizer is provided in the receiver. The equalizer can be configured as either a T or a T/2 equalizer using the EQT2 bit in the Chip 2 interface memory.

TRANSMITTED DATA SPECTRUM

When the compromise equalizer is disabled, the transmitter spectrum is shaped by raised cosine filter functions:

Configuration	Raised Cosine Filter Function
V.32 bis/V.32, V.17/V.33, V.29	Square root of 12.5%
V.27 ter	Square root of 50%
V.22 bis/V.22, Bell 212A	Square root of 75%

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Baud (Symbols/Sec.)	Bits per Symbol		Constellation Points
					Data	TCM	
V.32 bis 14400 TCM	TCM	1800	14400	2400	6	1	128
V.32 bis 12000 TCM	TCM	1800	12000	2400	5	1	64
V.32 bis 7200 TCM	TCM	1800	7200	2400	3	1	16
V.32 9600 TCM	TCM	1800	9600	2400	4	1	32
V.32 9600	QAM	1800	9600	2400	4	0	16
V.32 4800	QAM	1800	4800	2400	2	0	4
V.17/V.33 14400 TCM	TCM	1700 or 1800	14400	2400	6	1	128
V.17/V.33 12000 TCM	TCM	1700 or 1800	12000	2400	5	1	64
V.17/V.33 9600 TCM	TCM	1700 or 1800	9600	2400	4	1	32
V.17/V.33 7200 TCM	TCM	1700 or 1800	7200	2400	3	1	16
V.29 9600	QAM	1700	9600	2400	4	0	16
V.29 7200	QAM	1700	7200	2400	3	0	8
V.29 4800	QAM	1700	4800	2400	2	0	4
V.27 4800	DPSK	1800	4800	1600	3	0	8
V.27 2400	DPSK	1800	2400	1200	2	0	4
V.22 bis 2400	QAM	1200/2400	2400	600	4	0	16
V.22 bis 1200	QAM	1200/2400	1200	600	2	0	4
V.22 1200	QAM	1200/2400	1200	600	2	0	4
V.22 600	QAM	1200/2400	600	600	1	0	2
Bell 212A	QAM	1200/2400	1200	600	2	0	4
Bell 103	FSK	1170/2125	0–300	300	1	0	–
V.23 1200	FSK	1700/420	1200/75	1200	1	0	–
V.23 600	FSK	1500/420	600/75	600	1	0	–
V.21	FSK	1080/1750	0–300	300	1	0	–
V.21 channel 2 Tone Transmit	FSK	1750	300	300	1	0	–

Notes: 1. Modulation legend: TCM: Trellis-Coded Modulation
QAM: Quadrature Amplitude Modulation
FSK: Frequency Shift Keying
DPSK: Differential Phase Shift Keying

RTS – CTS RESPONSE TIME

The response times of CTS relative to a corresponding transition of RTS are listed in Table 2.

TRANSMIT LEVEL

The transmitter output level is selectable from –0.5 dBm to –15.5 dBm in 1 dB steps and is accurate to ±0.5 dB. The output level can also be fine tuned to a value within a 1 dB step by changing a gain constant in RAM.

TRANSMITTER TIMING

Transmitter timing is selectable between internal (±0.01%), external or loopback.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with the applicable CCITT recommendation.

ANSWER TONE

The transmitter generates a 2100 Hz answer tone for 3.6 seconds at the beginning of the answer handshake when the NV25 bit is a zero. This is applicable to V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21. The V.32 bis/V.32 answer tone has 180° phase reversals every 0.45 seconds to disable network echo cancellers.

RECEIVE LEVEL

The receiver satisfies performance requirements for received line signal levels from 0 dBm to –43 dBm. The received line signal level is measured at the Receiver Analog (RXA) input.

Table 2. RTS-CTS Response Time

Configuration	RTS-CTS Response[1]		Turn-Off Sequence[3]
	Constant Carrier	Controlled Carrier	
V.32 bis, V.32	≤ 2 ms	N/A	N/A
V.17/V.33 Long	N/A	1393 ms[2]	15 ms[4]
V.17/V.33 Short	N/A	142 ms[2]	15 ms[4]
V.29	N/A	253 ms[2]	12 ms
V.27 4800 Long	N/A	708 ms[2]	7 ms[4]
V.27 4800 Short	N/A	50 ms[2]	7 ms[4]
V.27 2400 Long	N/A	943 ms[2]	10 ms[4]
V.27 2400 Short	N/A	67 ms[2]	10 ms[4]
V.22 bis, V.22, Bell 212A	≤ 2 ms	270 ms	N/A
V.21	500 ms	500 ms	N/A
V.23, Bell 103	210 ms	210 ms	N/A

Notes:

1. Times listed are CTS turn-on. The CTS OFF-to-ON response time is host programmable in DSP RAM.
2. Add echo protector tone duration plus 20 ms when echo protector tone is used during turn-on.
3. Turn-off sequence consists of transmission of remaining data and scrambled ones for controlled carrier operation. CTS turn-off is less than 2 ms for all configurations.
4. Plus 20 ms of no transmitted energy.
5. N/A = not applicable.

RECEIVER TIMING

The timing recovery circuit can track a ±0.035% (V.22 bis) or ±0.01% (other than V.22 bis) frequency error in the associated transmit timing source.

CARRIER RECOVERY

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier with less than a 0.2 dB degradation in bit error rate (BER).

CLAMPING

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector (RLSD) is off. RLSD can be clamped off by a bit in the receiver sample rate device interface memory (RLSDE).

ECHO CANCELLER

A data echo canceller with near-end and far-end echo cancellation is included for 2-wire full-duplex V.32 operation. The combined echo span of near and far cancellers is host programmable with a default value of 53.3 ms (53.3 ms is also the maximum programmable value). The proportion allotted to each end is host programmable with default values of 23.3 ms for near-end and 30 ms for far-end. The delay between near-end and far-end echoes can be up to 1.7 seconds. The canceller can compensate for ±7 Hz frequency offset in the far-end echo. The echo canceller error signal may be monitored through the transmitter DSP interface memory.

ASYNC/SYNC, SYNC/ASYNC CONVERSION

An asynchronous-to-synchronous converter is provided in the transmitter and a synchronous-to-asynchronous converter is provided in the receiver. The converter operates in serial mode only. The asynchronous character format is 1 start bit, 5 to 8 data bits, an optional parity bit, and 1 or 2 stop bits. Valid character size, including all bits, is 7, 8, 9, 10, or 11 bits per character. Two ranges of signaling rates are provided:

- Basic: +1% to –2.5%
- Extended overspeed: +2.3% to –2.5%

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters. Break is handled in the transmitter and receiver as described in V.14.

Asynchronous characters are accepted by the transmitter on the TXD serial input and issued by the receiver on the RXD serial output. To configure the converters, the host must set up interface memory bits EXOS0, PEN0, STB0 and WDSZ0 bits before setting ASYN0 for the transmitter and EXOS1, PEN1, STB1 and WDSZ1 bits before setting ASYN1 for the receiver. The converter is not used in V.21, V.23, or Bell 103 mode.

V.54 INTER-DCE SIGNALLING

The modem supports V.54 inter-DCE signalling procedures in synchronous and asynchronous configurations. Transmission and detection of the preparatory, acknowledgement, and termination phases as defined in V.54 are provided. Three control bits in the transmitter allow the host to send the appropriate bit patterns (V54T, V54A, and V54P). Three control bits in the receiver are used to enable one of three bit pattern detectors (V54TE, V54AE, and V54PE). A status bit in the receiver indicates when the selected pattern detector has found the corresponding bit pattern (V54DT).

V.13 REMOTE RTS SIGNALLING

The modem supports V.13 remote RTS signalling procedures. Transmission and detection of signalling bit patterns in response to a change of state in the RTS bit or the RTS input signal are provided. A control bit in the transmitter enables V.13 signalling (RRTSE). A control bit in the receiver enables detection of V.13 patterns (RTSDE). A status bit in the receiver is used to indicate the state of the remote RTS signal (RTSDT). This feature may be used to clamp/unclamp the local RLSD and RXD signals in response to a change in the remote RTS signal in order to simulate controlled carrier operation in a constant carrier environment.

AUTO-DIALING AND AUTO-ANSWERING CONTROL

General Description

The host can perform auto-dialing and auto-answering. These functions include DTMF or pulse dialing, ringing detection and a comprehensive supervisory tone detection scheme. The major parameters of these functions are host programmable, enabling the host to customize the modem to work on the PSTN.

Supervisory Tone Detection

Three parallel tone detectors (A, B, and C) are provided for supervisory tone detection. The signal path to these detectors is separate from the main received signal path. Therefore, the tone detect signal does not pass through the highpass section of the analog receive bandpass filter, enabling the tone detection to be largely independent of the receiver status.

The tone detection bandwidth depends on the configuration:

Receiver Configuration	Tone Detection Bandwidth
V.32 bis, V.32, V.17/V.33, V.29, V.27 ter, V.23	0–3400 Hz
V.22 bis, V.22, Bell 212A, Bell 103 Originate	0–2800 Hz
V.22 bis, V.22, Bell 212A, Bell 103 Answer	0–1700 Hz
V.21 Originate	0–2200 Hz
V.21 Answer	0–1300 Hz

There are, however, some restrictions depending on the receiver configuration and status:

1. When DATA1 bit (see Table 8) is a 0, all three tone detectors are enabled.
2. When DATA1 bit is a 1 and the receiver is in synchronous mode (except V.32 bis 14400 or 12000), tone detectors A and B are enabled and tone detector C is disabled.
3. When DATA1 bit is a 1, the receiver is in asynchronous mode, V.32 bis 14400 or 12000, and the TDAE bit is a 1, tone detector A is enabled and tone detectors B and C are disabled.
4. All three tone detectors are disabled during a V.32 bis/V.32 handshake.

Each tone detector consists of two cascaded second order IIR biquad filters. The coefficients are host programmable. Each fourth order filter is followed by a level detector which has host programmable turn-on and turn-off thresholds allowing hysteresis. Tone detector C is preceded by a prefilter and squarer. This circuit is useful for detecting a tone with frequency equal to the difference between two tones that may be simultaneously present on the line. The squarer may be disabled by the SQDIS bit in interface memory causing tone detector C to be an eighth order filter.

Supervisory Tone Detectors, Default Characteristics

The default bandwidths and thresholds of the tone detectors are as follows:

Tone Detector	Bandwidth	Turn-On Threshold	Threshold Turn-Off
A	245 – 650 Hz	–25 dBm	–31 dBm
B	360 – 440 Hz	–25 dBm	–31 dBm
C Prefilter	0 – 500 Hz	N/A	N/A
C	50 – 110 Hz	*	*

*Tone Detector C will detect a difference tone within its bandwidth when the two tones present are in the range –1 dBm to –26 dBm.

GENERAL SPECIFICATIONS

The power requirements and environmental requirements are listed in Tables 3 and 4, respectively. The module dimensions are listed in Table 5.

Table 3. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Maximum) @ 0°C
+5 VDC	±5%	300 mA	585 mA
+12 VDC	±5%	3 mA	6 mA
−12 VDC	±5%	30 mA	36 mA

Note 1. Input voltage ripple ± 0.1 volts peak-to-peak. The amplitude of any frequency between 20 kHz and 150 kHz must be less than 500 microvolts peak.

Table 4. Modem Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to +70°C (32°F to 158°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Table 5. Modem Mechanical Dimensions

Parameter	Specification
Board Structure:	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions:	
Width	3.228 in. (82 mm)
Length	3.937 in. (100 mm)
Component Height	
Top (max.)	0.300 in. (7.62 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max.):	3.6 oz. (100 g)
Pin Length (max.)	0.535 ±0.015 in. (13.6 ± 0.4 mm), gold plated. 0.433 ±0.015 in. (11.0 ± 0.4 mm), gold plated. 0.315 ±0.015 in. (8.0 ± 0.4 mm), gold plated.

HARDWARE INTERFACE SIGNALS

The functional interconnect diagram (Figure 1) shows the typical modem connection in a system. In this diagram, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., $\overline{IRQ}$). Active low signals are overscored (e.g., $\overline{POR}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., $\overline{RDCLK}$), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high, (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The hardware interconnect signals shown in Figure 1 are organized into six functional groups: overhead, microprocessor interface, V.24 interface, ancillary, analog, and diagnostic. These signals, along with their connector pin numbers and interface circuit types, are listed in Table 6. The digital interface characteristics are defined in Tables 7 and 8, respectively. The hardware interface signals are described in Table 9.

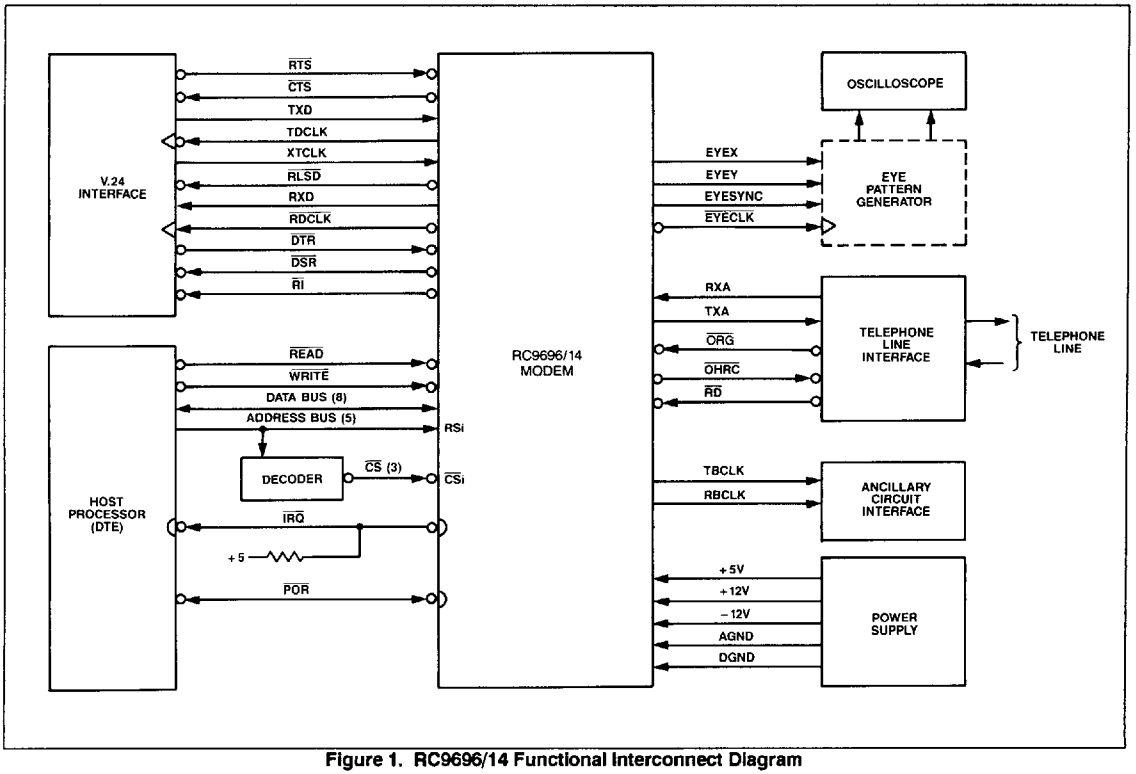


Figure 1. RC9696/14 Functional Interconnect Diagram

Table 6. Hardware Interface Signals

Name	Type	Pin No.	Description
OVERHEAD			
$\overline{POR}$	IB/OB	2	Power-On-Reset
+5V	PWR	1, 45, 61	+5 Volt Supply
+12V	PWR	32	+12 Volt Supply
−12V	PWR	36	−12 Volt Supply
DGND	GND	29, 37, 53	Digital Ground
AGND	GND	30, 31	Analog Ground
MICROPROCESSOR INTERFACE			
D7	IA/OB	3	Data Bus Line 7
D6	IA/OB	4	Data Bus Line 6
D5	IA/OB	5	Data Bus Line 5
D4	IA/OB	6	Data Bus Line 4
D3	IA/OB	7	Data Bus Line 3
D2	IA/OB	8	Data Bus Line 2
D1	IA/OB	9	Data Bus Line 1
D0	IA/OB	10	Data Bus Line 0
RS4	IA	15	Register Select Line 4
RS3	IA	16	Register Select Line 3
RS2	IA	17	Register Select Line 2
RS1	IA	18	Register Select Line 1
$\overline{RS0}$	IA	19	Register Select Line 0
$\overline{CS0}$	IA	20	Chip Select Transmitter Device
$\overline{CS1}$	IA	21	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	13	Chip Select Receiver Baud Rate Device
$\overline{READ}$	IA	14	Read Enable
$\overline{WRITE}$	IA	12	Write Enable
$\overline{IRQ}$	OC	11	Interrupt Request
V.24 INTERFACE			
$\overline{RDCLK}$	OA	23	Receive Data Clock
TDCLK	OA	46	Transmit Data Clock
$\overline{XTCLK}$	IA	51	External Transmit Clock
$\overline{RTS}$	IA	50	Request-to-Send
$\overline{CTS}$	OA	49	Clear-to-Send
TXD	IA	48	Transmitter Data
$\overline{RXD}$	OA	26	Receiver Data
$\overline{RLSD}$	OA	27	Received Line Signal Detector
$\overline{DTR}$	IA	40	Data Terminal Ready
$\overline{DSR}$	OA	41	Data Set Ready
$\overline{RI}$	OA	25	Ring Indicator

Table 6. Hardware Interface Signals (Cont'd)

Name	Type	Pin No.	Description
ANCILLARY CIRCUITS			
RBCLK	OA	22	Receiver Baud Clock
TBCLK	OA	47	Transmitter Baud Clock
LINE INTERFACE			
TXA	AA	34	Transmitter Analog Output
$\overline{RXA}$	AB	33	Receiver Analog Input
$\overline{OHRC}$	OD	35	Off-Hook Relay Control
$\overline{RD}$	IA	24	Ring Detect
$\overline{ORG}$	IA	42	Originate
DIAGNOSTIC			
EYEX	OA	56	Eye Pattern Data–X Axis
$\overline{EYEY}$	OA	55	Eye Pattern Data–Y Axis
$\overline{EYECLK}$	OA	57	Eye Pattern Clock
EYESYNC	OA	58	Eye Pattern Synchronizing Signal

Notes:

1. Refer to Table 7 for digital circuit interface characteristics and Table 8 for analog circuit interface characteristics.
2. The following pins should be left open: 28, 39, 43, 44, 52, 59, and 60.
3. The following pins are not used but should be connected to DGND through individual 10 KΩ series resistors: 38 and 54.
4. Unused inputs tied to +5V or ground require individual 10 KΩ series resistors.

Table 7. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type					
			IA	IB	OA	OB	OC	OD
V_{IH}	Input Voltage, High	V	2.0 min	4.0 min.				
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.				
V_{OH}	Output Voltage, High	V			3.5 min.[1]	3.5min.[1]		
V_{OL}	Output Voltage, Low	V			0.4 max.[2]	0.4 max.[3]	0.4 max.[2]	0.75 max[5]
I_{IN}	Input Current, Leakage	µA	±2.5 max.	±2.5 max.				
I_{OH}	Output Current, High	µA			−100 max.	−100 max		0[4]
I_{OL}	Output Current, Low	mA			1.6 max.	0.8 max.	1.6 max.	15.0 max.[5]
I_L	Output Current, Leakage	µA			±10 max.	±10 max.		
C_L	Capacitive Load	pF	5	5				
C_D	Capacitive Drive	pF			50	50	50	
	Circuit Type		TTL	TTL	TTL 3-state	TTL 3-state	Open-Drain	Open-Drain

Notes:

1. I Load = −100 µA
2. I Load = 1.6 mA
3. I Load = 0.8 mA
4. µA leakage
5. Can drive a +5V relay with coil resistance greater than 360Ω.

Table 8. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output impedance is 604 Ω ±1%.
RXA	AB	The receiver input impedance is 71.5K Ω ±14%.

Table 9. Hardware Interface Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
$\overline{POR}$	IB/OB	**Power-On-Reset.** When power is applied to the modem, the modem pulses Power-On-Reset ($\overline{POR}$) low to begin the POR sequence. The modem is ready to use 350 ms after the low-to-high transition of $\overline{POR}$. The POR sequence is reinitiated any time the +5V supply drops below +3.5V for more than 30 ms, or an external device drives $\overline{POR}$ low for at least 3 µs.
+5V	PWR	**+ 5V Digital Supply.** +5V must be connected to +5V ± 5%.
+12V	PWR	**+ 12V Analog Supply.** +12V must be connected to +12V ± 5%.
–12V	PWR	**–12V Analog Supply.** –12VA must be connected to –12V ± 5%.
DGND	GND	**Digital Ground.** DGND must be connected to digital ground.
AGND	GND	**Analog Ground.** AGND must be connected to analog ground.
		MICROPROCESSOR BUS
		Data, control, and interrupt hardware interface signals are provided to allow modem connection to an 8086 compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 6502, 8086 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits.
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable and Write Enable signals.
RS0 - RS4	IA	**Register Select Lines.** The five active high register select lines (RS0–RS4) address interface memory registers within the selected DSP interface memory. These lines are typically connected to the five least significant lines (A0-A4) of the host address bus. The selected DSP decodes RS0 through RS4 to address one of 32 internal interface memory registers (00–1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from or written into via the 8-bit parallel data bus (D0–D7). The most significant data bit is D7 while the least significant data bit is D0.
$\overline{CS0}$-$\overline{CS2}$	IA	**Chip Selects.** Each active low chip select input selects one of three modem DSP devices. $\overline{CS0}$-$\overline{CS2}$ are typically generated by decoding the host address bus lines.
$\overline{READ}$ $\overline{WRITE}$	IA IA	**Read Enable and Write Enable.** During a read cycle, data from the selected DSP interface memory register is gated onto the data bus by means of three-state drivers in each DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state. During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
$\overline{IRQ}$	OC	**Interrupt Request.** The modem ($\overline{IRQ}$) output may be optionally connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in the DSP interface memory to indicate immediate change of conditions in any of the three modem DSP devices. The DSP $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). Each of the individual DSP $\overline{IRQ}$ output lines is wire-ORed to form the modem $\overline{IRQ}$ output signal. The modem $\overline{IRQ}$ output can also be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high).

Table 9. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		V.24 SERIAL INTERFACE
		Timing, data, control, and status signals provide a V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to RS-232-C voltage levels.
TXD	IA	**Transmitted Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input.
RXD	OA	**Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output.
$\overline{RTS}$	IA	**Request to Send.** Activating ($\overline{RTS}$) causes the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The $\overline{RTS}$ pin is logically ORed with the RTS bit.
$\overline{CTS}$	OA	**Clear To Send.** $\overline{CTS}$ active indicates to the local DTE that the modem will transmit any data present on TXD. CTS response times from an active condition of RTS are shown in Table 2.
$\overline{RLSD}$	OA	**Received Line Signal Detector.** $\overline{RLSD}$ active indicates to the local DTE that energy above the receive level threshold is present on the receiver input, and that the energy is not a training sequence. One of four $\overline{RLSD}$ receive level threshold options can be selected (Table 10). A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with a modulated signal applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than –43 dBm. The $\overline{RLSD}$ on and off thresholds are host programmable in DSP RAM.
$\overline{DTR}$	IA	**Data Terminal Ready.** In V.32, V.32 bis, V.22, V.22 bis, and Bell 212A configurations, activating $\overline{DTR}$ initiates the handshake sequence, provided that the DATA0 bit is a 1. If in answer mode, the transmitter will immediately send answer tone. In V.21, V.23, and Bell 103 configurations, activating $\overline{DTR}$ causes the modem to enter the data state provided that the DATA0 bit is a 1. If in answer mode, the transmitter will immediately send answer tone. In these modes, if controlled carrier is enabled, carrier is controlled by $\overline{RTS}$. During the data mode, deactivating $\overline{DTR}$ causes the transmitter and receiver to turn off and return to the idle state. The $\overline{DTR}$ input and the DTR control bit in chip 0 are logically ORed.
$\overline{DSR}$	OA	**Data Set Ready.** $\overline{DSR}$ ON indicates that the modem is in the data transfer state. $\overline{DSR}$ OFF indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator (RI). DSR is OFF when the modem is in a test mode (i.e., local analog or remote digital loopback). The DSR status bit in chip 0 reflects the state of the $\overline{DSR}$ output.
$\overline{RI}$	OA	**Ring Indicator.** $\overline{RI}$ output follows the ringing signal present on the line with a low level (0V) during the ON time, and a high level (+5V) during the OFF time coincident with the ringing signal. The RI status bit in chip 2 reflects the state of the $\overline{RI}$ output.
TDCLK	OA	**Transmit Data Clock.** The modem outputs a synchronous Transmit Data Clock (TDCLK) for USRT timing. The TDCLK frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The TDCLK source can be internal, external (input on XTCLK) or slave (to $\overline{RDCLK}$) as selected by bits in the transmitter interface memory.
XTCLK	IA	**External Transmit Clock.** In synchronous communication, an external transmit data clock can be connected to the modem XTCLK input. The clock supplied at XTCLK must exhibit the same characteristics as TDCLK. The XTCLK input is then reflected at the TDCLK output.
$\overline{RDCLK}$	OA	**Receive Data Clock.** The modem outputs a synchronous Receive Data Clock ($\overline{RDCLK}$) for USRT timing. The $\overline{RDCLK}$ frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The $\overline{RDCLK}$ low-to-high transitions coincide with the center of the received data bits.

Table 9. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		ANCILLARY SIGNALS
TBCLK RBCLK	OA OA	**Transmitter Baud Clock and Receiver Baud Clock.** TBCLK and RBCLK active high outputs mark the baud interval rather than the data rate for the transmitter and receiver, respectively. These baud clocks are useful in identifying the order of data bits in a baud (e.g., for multiplexing data). The first bit in each baud begins with the falling edge of the corresponding baud clock. In asynchronous mode, the baud clocks are character clocks.
		LINE INTERFACE
		The Transmitter Analog (TXA) output and Receiver Analog (RXA) input allow modem connection to either a leased line or the PSTN through an audio transformer or a data access arrangement.
TXA	AA	**Transmitter Analog.** The TXA output can drive an audio transformer or data access arrangement. TXA is a low impedance amplifier output in series with an internal 604 ohm ±1% resistor to match a standard telephone load of 600 ohms.
RXA	AB	**Receiver Analog.** The RXA input can originate from an audio transformer or data access arrangement. The input impedance is nominally 66.5K ohms. The RXA input must be shunted by an external 604 ohm ±1% resistor in order to match a 600 ohm source. The maximum received signal at RXA is 0 dBm. The maximum near-end echo at RXA that the modem can cancel in V.32 mode is –5 dBm. Transient protection for TXA and RXA is recommended when interfacing directly to a transformer. This protection can be back-to-back zener diodes or a varistor across the transformer.
$\overline{\text{OHRC}}$	OD	**Off-Hook Relay Control.** $\overline{\text{OHRC}}$ is an output designed to drive directly a +5V reed relay coil with a worst case resistance of 360 ohms having a must-operate voltage no greater than 4.0 Vdc. A clamp diode, such as a 1N4004, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). $\overline{\text{OHCR}}$ is controlled by the host setting the RA bit.
$\overline{\text{RD}}$	IA	**Ring Detect.** The $\overline{\text{RD}}$ input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving $\overline{\text{RD}}$ should be a 4N35 optoisolator or equivalent. The circuit driving $\overline{\text{RD}}$ should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. DATA2 bit must be set to a 0 to enable ring detection. Detected ring signals are reflected on the RI output signal as well as the RI bit.
$\overline{\text{ORG}}$	IA	**Originate.** The $\overline{\text{ORG}}$ input pin determines the mode the modem will enter upon completion of a power-on-reset (POR) sequence (low = originate; high = answer). After the POR sequence is completed, the host may configure the modem for originate or answer using the ORG bit. If unused, the $\overline{\text{ORG}}$ pin must be connected to DGND through a 10K Ω resistor.
		DIAGNOSTIC SIGNALS
		Four signals provide the timing and data needed to create an oscilloscope quadrature eye pattern. The eye pattern is a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified. The EYEX and EYEY outputs are two serial bit streams containing data for display on the X axis and Y axis, respectively. This serial digital data must be converted to parallel digital form and then to analog form.
EYEX, EYEY	OA OA	**Serial Eye Pattern X and Y Output.** EYEX and EYEY outputs are 15-bit words, each with 8-bits of significance. The 15-bit data words are shifted out most significant bit first with the seven most significant bits equal to zero. EYEX and EYEY are clocked by the rising edge of EYECLK.
$\overline{\text{EYECLK}}$	OA	**Serial Eye Pattern Clock.** $\overline{\text{EYECLK}}$ is a clock for use by the serial-to-parallel converters. The EYECLK output is a 288 kHz clock which is internally divided down to create the Receiver Baud Clock (RBCLK). $\overline{\text{EYECLK}}$ is also a common multiple of all the possible receiver data clocks.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a strobe for loading the D/A converters.

SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in three DSPs: transmitter device, receiver sample rate device, and receiver baud rate device.

INTERFACE MEMORY

Each DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in each DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus shared between the three DSPs.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

INTERFACE MEMORY MAPS

Memory maps of the 96 addressable registers in the modem transmitter (chip 0), receiver sample rate (chip 1), and receiver baud rate (chip 2) devices are shown in Figure 2. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or a group of bits in a register, the host processor must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory.

INTERFACE MEMORY BIT DEFINITIONS

Table 10 defines the individual bits in the interface memory. In the Table 8 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0,1 or 2), the register number by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = LSB).

DSP RAM ACCESS

Each DSP contains a 16-bit wide random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can access (read or write) the X RAM only, the Y RAM only, or both the X RAM and the Y RAM simultaneously.

Interface Memory Access to DSP RAM

The interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The address stored in DSP interface memory RAM Access registers by the host, in conjunction with the data or coefficient RAM bit (e.g., XCR0) determines the DSP RAM address for data access.

One or two 16-bit words are transferred between DSP RAM and DSP interface memory once each device cycle. The transmitter device and the receiver sample rate device operate at the 9600 Hz sample rate. The receiver baud rate device operates at the baud rate of the selected data rate.

Two RAM access bits in each DSP interface memory tell the DSP to access the X RAM and/or Y RAM. For example, the transfer is initiated in the transmitter by the host setting the XACC0 and/or the YACC0 bit(s). The transmitter tests these bits each sample period. The receiver tests XACC1 and YACC1 each sample period and XACC2 and YACC2 each baud period.

The parameters available in DSP RAM are listed in Table 11 along with the respective addressing information, i.e., chip number, address code, and CR bit value.

RC9696/14 DSP Interface Memory (Chip 0)

Register	Bit 7	6	5	4	3	2	1	0
1F	NSIA0	NCIA0	—	NSIE0	NEWS0	NCIE0	—	NEWC0
1E	—	DBIA0	—	—	—	DBIE0	—	DBA0
1D	XACC0	—	—	—	—	XCRD0	XWT0	XCR0
1C	X RAM ADDRESS (XADD0)							
1B	YACC0	—	—	—	—	YCRD0	YWT0	YCR0
1A	Y RAM ADDRESS (YADD0)							
19	X RAM DATA MSB (XDAM0)							
18	X RAM DATA LSB (XDAL0)							
17	Y RAM DATA MSB (YDAM0)							
16	Y RAM DATA LSB (YDAL0)							
15	—	—	—	—	—	RREN	EXL3	EARC0
14	—	—	—	—	—	—	—	—
13	TLVL				—	—	TXCLK	
12	TRANSMITTER CONFIGURATION (TCONF)							
11	—	—	—	—	—	V23HDX	ECMOD	—
10	—	—	—	—	—	—	—	—
0F	—	—	CTS	DSR	—	TM	—	—
0E	—	—	—	—	—	—	—	—
0D	—	—	—	—	—	—	—	HKAB0
0C	—	—	—	—	—	—	—	—
0B	—	—	—	—	—	—	—	—
0A	—	—	—	—	—	—	—	—
09	NV25	CC	DTMF	ORG	LL0	DATA0	RRTSE	DTR
08	ASYN0	TPDM	V21S0	V54T	V54A	V54P	RTRN	RTS
07	—	RDL	L2ACT	—	L3ACT	L4ACT	RA	MHLD
06	—	EXOS0	CF170	SHAP0	PEN0	STB0	WDSZ0	
05	ECFZ	ECSQ	FECSQ	TXSQ	CEQ	TTDIS	STOFF	TSPA
04	—	—	V32BS0	—	—	—	—	STRN0
03	EPT	SEPT	—	—	ARC0	SDIS	GTE	GTS
02	—	—	—	—	—	—	—	—
01	TSPY							
00	TBUFFER/TSPX							

RC9696/14 DSP Interface Memory (Chip 1)

Register	Bit 7	6	5	4	3	2	1	0
1F	NSIA1	NCIA1	—	NSIE1	NEWS1	NCIE1	—	NEWC1
1E	—	DBIA1	—	—	—	DBIE1	—	DBA1
1D	XACC1	—	—	—	—	XCRD1	XWT1	XCR1
1C	X RAM ADDRESS (XADD1)							
1B	YACC1	—	—	—	—	YCRD1	YWT1	YCR1
1A	Y RAM ADDRESS (YADD1)							
19	X RAM DATA MSB (XDAM1)							
18	X RAM DATA LSB (XDAL1)							
17	Y RAM DATA MSB (YDAM1)							
16	Y RAM DATA LSB (YDAL1)							
15	—	—	—	—	—	—	—	EARC1
14	ABCODE							
13	—	—	—	—	RTH		—	
12	RECEIVER CONFIGURATION (RCONF)							
11	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—
0F	RLSD	FED	—	—	—	—	—	—
0E	RTDET	—	—	—	SPEED			
0D	P2DET	PNDET	S1DET	SCR1	U1DET	—	—	HKAB1
0C	AADET	ACDET	CADET	CCDET	SDET	SNDET	—	RSEQ
0B	TONEA	TONEB	TONEC	ATV25	ATBEL	V21	—	—
0A	—	—	—	—	—	—	—	—
09	—	—	—	—	LL1	DATA1	—	—
08	ASYN1	—	V21S1	—	—	—	—	—
07	RDLE	—	—	—	—	—	—	—
06	RTDIS	EXOS1	CF171	SHAP1	PEN1	STB1	WDSZ1	
05	—	—	—	—	—	—	—	—
04	—	—	V32BS1	—	—	—	—	STRN1
03	—	—	CEQ23	RLSDE	ARC1	—	—	—
02	TDAE	SQDIS	—	—	—	—	—	—
01	RSEQM							
00	RBUFFER/RSEQL							

NOTE: (—) Indicated reserved for modem use only.

RC9696/14 DSP Interface Memory (Chip 2)

Register	Bit 7	6	5	4	3	2	1	0
1F	NSIA2	—	—	NSIE2	NEWS2	—	—	—
1E	—	DBIA2	—	—	—	DBIE2	—	DBA2
1D	XACC2	—	—	—	—	XCRD2	XWT2	XCR2
1C	X RAM ADDRESS (XADD2)							
1B	YACC2	—	—	—	—	YCRD2	YWT2	YCR2
1A	Y RAM ADDRESS (YADD2)							
19	X RAM DATA MSB (XDAM2)							
18	X RAM DATA LSB (XDAL2)							
17	Y RAM DATA MSB (YDAM2)							
16	Y RAM DATA LSB (YDAL2)							
15	—	—	—	—	—	—	—	—
14	—	—	—	—	—	—	—	—
13	—	—	—	—	—	—	—	—
12	—	—	—	—	—	—	—	—
11	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—
0F	—	—	—	—	RI	—	RTSDT	V54DT
0E	—	—	RREDT	V32BDT	—	—	—	—
0D	—	—	—	—	—	—	—	—
0C	—	—	—	—	—	—	—	—
0B	—	—	—	—	—	—	—	—
0A	—	—	—	—	—	—	—	—
09	—	—	—	—	—	DATA2	—	—
08	—	—	—	—	—	—	—	—
07	—	—	—	DDIS	—	—	—	—
06	—	—	—	—	—	—	—	—
05	—	—	—	—	—	—	—	—
04	EQRES	EQT2	—	RSPA	EQFZ	IFIX	TOD	STRN2
03	—	—	—	—	—	—	—	—
02	—	—	AMTD	—	RTSDE	V54TE	V54AE	V54PE
01	RSPY							
00	RSPX							

NOTE: (—) Indicated reserved for modem use only.

Figure 2. RC9696/14 DSP Interface Memory Map

Table 10. Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
AADET	1:C:7	–	**AA Detector.** Status bit AADET is used to indicate a V.32 bis/V.32 AA sequence has been detected. (V.32 bis, V.32)
ABCODE	1:14:0–7	00	**Abort Code.** If the V.32/V.32 bis handshake fails, status bit HKAB1 is set to a 1 and an abort code is written into ABCODE to indicate the point in the handshake where the failure occurred. (V.32 bis, V.32)
ACDET	1:C:6	–	**AC Detector.** Status bit ACDET is used to indicate a V.32 bis/V.32 AC sequence has been detected. (V.32 bis, V.32)
AMTD	2:2:5	1	**Amplitude Modulation Tracker Disable.** Control bit AMTD disables or enables the adaptive amplitude modulation tracker in the receiver. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
ARC0	0:3:3	1	**Automatic Rate Change Enable Chip 0.** When control bits ARC0 and ARC1 are both 1, the modem automatically conditions itself to transmit data at the highest common rate negotiated during the V.32 bis/V.32 handshake. The host may specify the undefined bits in the rate sequence in DSP RAM. When ARC0 and ARC1 are both 0, the modem cannot change from the rate it is configured to before beginning the handshake. However, it is possible for the host to interact with the rate sequences during the handshake and then set the transmitter configuration as desired. (See EARC0.) (V.32 bis, V.32) When control bit ARC0 and ARC1 are 1, then setting the RTRN bit will cause the modem to send a rate change sequence rather than the normal retrain sequence. (V.22 bis) (See RTRN.)
ARC1	1:3:3	1	**Automatic Rate Change Enable Chip 1.** See ARC0 and EARC0.
ASYN0	0:8:7	0	**Asynchronous/Synchronous.** Control bit ASYN0 selects either asynchronous or synchronous mode in the transmitter. ASYN0 may be used to switch between synchronous and asynchronous modes at any time in idle or data mode. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
ASYN1	1:8:7	0	**Asynchronous/Synchronous.** Control bit ASYN1 selects either asynchronous or synchronous mode in the receiver. ASYN1 may be used to switch between synchronous and asynchronous modes at any time in idle or data mode. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
ATBEL	1:B:3	–	**Bell Answer Tone Detector.** Status bit ATBEL is used to indicate the modem receiver has detected a 2225 Hz answer tone. ATBEL is active only when the DATA1 bit is a 0 and the modem is in originate mode. (Bell 212A, Bell 103)
ATV25	1:B:4	–	**V25 Answer Tone Detector.** Status bit ATV25 is used to indicate the modem receiver has detected a 2100 Hz answer tone. ATV25 is only active when the DATA1 bit is a 0 and the modem is in originate mode. (V.32 bis, V.32, V.22 bis, V.22, V.23, V.21)
CADET	1:C:5	–	**CA Detector.** Status bit CADET is used to indicate a V.32 bis/V.32 CA sequence has been detected. (V.32 bis, V.32)
CC	0:9:6	0	**Controlled Carrier.** Control bit CC selects controlled (by RTS) or constant carrier operation. (V.22 bis, V.22, V.23, Bell 212A)
CCDET	1:C:4	–	**CC Detector.** Status bit CCDET is used to indicate a V.32 bis/V.32 CC sequence has been detected. (V.32 bis, V.32)
CEQ	0:5:3	1	**Compromise Equalizer Enable.** Control bit CEQ enables or disables insertion of the transmitter's digital compromise equalizer into the transmit path. This bandpass equalizer has host programmable taps in DSP RAM.
CEQ23	1:3:5	0	**V.23 Compromise Equalizer Enable.** Control bit CEQ23 enables or disables insertion of the receiver's digital compromise equalizer into the receive path. This bandpass equalizer has host programmable taps in DSP RAM. (V.23)
CF170	0:6:5	0	**Carrier Frequency 1700 Hz Chip 0.** Control bit CF170 selects either the 1700 or 1800 Hz transmitter carrier frequency. The non-standard 1700 Hz option is provided for use with a secondary channel which is added at the high end of the band. (V.17/V.33)
CF171	1:6:5	0	**Carrier Frequency 1700 Hz Chip 1.** Control bit CF171 selects either the 1700 or 1800 Hz transmitter carrier frequency. The non-standard 1700 Hz option is provided for use with a secondary channel which is added at the high end of the band. (V.17/V.33)
CTS	0:F:5	–	**Clear To Send.** Status bit CTS is used to indicate the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted (see TPDM). CTS response times from an RTS ON or OFF transition after the modem has completed a handshake are shown in Table 2. The CTS OFF-to-ON response time is programmable in DSP RAM.

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
DATA0	0:9:2	1	**Data Chip 0.** Control bit DATA0 is used to prevent the transmitter from entering and proceeding with the handshake (start-up) sequence and to ignore all V.24 interface signals.
DATA1	1:9:2	1	**Data Chip 1.** Control bit DATA1 is used to prevent the receiver from entering and proceeding with the handshake (start-up) sequence.
DATA2	2:9:2	1	**Data Chip 2.** Control bit DATA2 enables or disables the ring detector.
DBA0	0:1E:0	–	**Data Buffer Available Chip 0.** Status bit DBA0 is used to indicate the transmitter has read register 0:0 (TBUFFER), or registers 0:1 (TSPY) and 0:0 (TSPX), and the host can write new data into register 0:0 or into registers 0:1 and 0:0. (See DBIE0 and DBIA0.)
DBA1	1:1E:0	–	**Data Buffer Available Chip 1.** Status bit DBA1 is used to indicate the receiver wrote valid data into register 1:0 (RBUFFER) or into registers 1:1 (RSEQM) and 1:0 (RSEQL). (See DBIE1 and DBIA1.)
DBA2	2:1E:0	–	**Data Buffer Available Chip 2.** Status bit DBA1 is used to indicate the receiver wrote valid data into registers 2:1 (RSPY) and 2:0 (RSPX). (See DBIE2 and DBIA2.)
DBIA0	0:1E:6	–	**Data Buffer Interrupt Active Chip 0.** Status bit DBIA0 is used to indicate DBA0 caused $\overline{IRQ}$ to be asserted when enabled by the DBIE0 bit. (See DBIE0 and DBA0.)
DBIA1	1:1E:6	–	**Data Buffer Interrupt Active Chip 1.** Status bit DBIA1 is used to indicate DBA1 caused $\overline{IRQ}$ to be asserted when enabled by the DBIE1 bit. (See DBIE1 and DBA1.)
DBIA2	2:1E:6	–	**Data Buffer Interrupt Active Chip 2.** Status bit DBIA2 is used to indicate DBA2 caused $\overline{IRQ}$ to be asserted when enabled by the DBIE2 bit. (See DBIE2 and DBA2.)
DBIE0	0:1E:2	0	**Data Buffer Interrupt Enable Chip 0.** Control bit DBIE0 enables or disables assertion of $\overline{IRQ}$ and the setting of DBIA0 when DBA0 is set to a 1 by the modem. (See DBA0 and DBIA0.)
DBIE1	1:1E:2	0	**Data Buffer Interrupt Enable Chip 1.** Control bit DBIE1 enables or disables assertion of $\overline{IRQ}$ and the setting of DBIA1 when DBA1 is set to a 1 by the modem. (See DBA1 and DBIA1.)
DBIE2	2:1E:2	0	**Data Buffer Interrupt Enable Chip 2.** Control bit DBIE2 enables or disables assertion of $\overline{IRQ}$ and the setting of DBIA2 when DBA2 is set to a 1 by the modem. (See DBA2 and DBIA2.)
DDIS	2:7:4	0	**Descrambler Disable.** Control bit DDIS disables or enables the receiver's descrambler circuit.
DSR	0:F:4	–	**Data Set Ready.** Status bit DSR is used to indicate the modem is in the data transfer state. The DTE is to disregard all signals appearing on the interchange circuits except $\overline{RI}$ when DTR is OFF. DSR will switch to the OFF state when the modem is in a test mode.
DTMF	0:9:5	0	**DTMF Select.** Control bit DTMF selects either DTMF or pulse dialing when the modem is in dialing mode.
DTR	0:9:0	0	**Data Terminal Ready.** In modes V.32 bis/V.32, V.22 bis/V.22, and Bell 212A, control bit DTR is used to initiate a handshake sequence in originate mode (providing DATA0 bit is a 1) or to immediately send answer tone in answer mode. In modes V.21, V.23, and Bell 103, control bit DTR must be a 1 for the modem to enter data state providing DATA0 bit is a 1. If in answer mode, the transmitter will send answer tone. In these configurations, if controlled carrier is selected, the carrier is controlled by the $\overline{RTS}$ pin or RTS bit. During the data mode, setting DTR to a 0 will cause the transmitter to turn off. The DTR bit parallels the operation of the hardware $\overline{DTR}$ control input. These inputs are ORed by the modem.
EARC0	0:15:0	0	**Extended Automatic Rate Change 0.** Control bits EARC0 and EARC1 enable automatic rate change for the transmitter in either proprietary/standard or standard configuration during the V.32 bis/V.32 handshake. (See ARC0 and ARC1) (V.32 bis, V.32).
EARC1	1:15:0	0	**Extended Automatic Rate Change Chip 1.** See EARC0. (V.32 bis, V.32)
ECFZ	0:5:7	0	**Echo Canceller Freeze.** Control bit ECFZ inhibits or enables updating of the echo canceller taps. (V.32 bis, V.32)
ECMOD	0:14:0	0	**Echo Canceller Mode.** Control bit ECMOD is used to allow the echo canceller dividing point to automatically adjust in order to compensate for short round trip delays or to remain fixed. (V.32 bis, V.32)
ECSQ	0:5:6	0	**Echo Canceller Squelch.** Control bit ECSQ is used to force the echo canceller output to zero. (V.32 bis, V.32)
EPT	0:3:7	0	**Echo Protector Tone Enable.** When control bit EPT is a 1, an unmodulated carrier is transmitted for 185 ms (SEPT bit = 0) or 30 ms (SEPT bit = 1) followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is a 0, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence. (V.17/V.33, V.29, V.27 ter)

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
EQFZ	2:4:3	0	**Equalizer Freeze.** Control bit EQFZ inhibits or enables updating of the receiver's adaptive equalizer taps.
EQRES	2:4:7	0	**Equalizer Reset.** Control bit EQRES is used to allow the receiver to either reset all of the adaptive equalizer's taps to zero or to update the equalizer taps normally. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A, V.33/V.17, V.29, V.27)
EQT2	2:4:6	0	**Equalizer T/2 Spacing Select.** Control bit EQT2 selects the receiver's adaptive equalizer spacing to be either T/2 fractionally spaced or T spaced (T = 1 baud time).
EXL3	0:15:1	0	**External Loop 3 Selector.** Control bit EXL3 selects either external or internal path during local analog test (loop 3). (See L3ACT.)
EXOS0	0:6:6	0	**Extended Overspeed Chip 0.** Control bit EXOS0 selects Extended or Normal Overspeed mode in the transmitter async-to-sync converter. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
EXOS1	1:6:6	0	**Extended Overspeed Chip 1.** Control bit EXOS0 selects Extended or Normal Overspeed mode in the receiver sync-to-async converter. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
FECSQ	0:5:5	0	**Far Echo Canceller Squelch.** Control bit FECSQ is used to force the output of the far-end echo canceller to zero. (V.32 bis, V.32)
FED	1:F:6	–	**Fast Energy Detector.** Status bit FED is used to indicate energy in the passband above the selected receiver threshold has been detected (see RTH).
GTE	0:3:1	0	**Guard Tone Enable.** Control bit GTE enables or disables transmission of guard tone by the answering modem as selected by the GTS bit in a CCITT configuration. (V.22 bis)
GTS	0:3:0	0	**Guard Tone Select.** Control bit GTS selects the 550 Hz or 1800 Hz guard tone (see GTE). (V.22 bis)
HKAB0	0:D:0	–	**Handshake Abort Chip 0.** Status bit HKAB0 is used to indicate the V.32 bis/V.32 handshake has failed. The transmitter remains in an abort state for 1 second after which HKAB0 is reset to 0 and the transmitter returns to idle mode. While in the abort state the transmitter output is silent.
HKAB1	1:D:0	–	**Handshake Abort Chip 1.** Status bit HKAB1 is set to indicate the V.32 bis/V.32 handshake has failed. At the same time an abort code is written into ABCODE (see ABCODE). (V.32 bis, V.32)
IFIX	2:4:2	1	**Eye Fix.** Control bit IFIX enables the serial diagnostic data on EYEX and EYEY to either reflect the Rotated Equalizer Output or to selected by the addresses in X RAM ADDRESS and Y RAM ADDRESS registers in chip 2, respectively.
L2ACT	0:7:5	0	**Loop 2 Activate.** Control bit L2ACT is used to cause the receiver's digital output to be connected to the transmitter's digital input (locally activated remote digital loopback) in accordance with V.54. (Not valid in FSK modes.)
L3ACT	0:7:3	0	**Loop 3 Activate.** Control bit L3ACT is used to cause the transmitter's analog output to be coupled internally to the receiver's analog input through an attenuator (local analog loopback) in accordance with V.54. Optionally, the signal path for loop 3 can also be established externally to the modem (see EXL3).
L4ACT	0:7:2	0	**Loop 4 Activate.** Control bit L4ACT is used to cause the receiver's analog input to be connected to the transmitter's output (remote analog loopback) in a manner similar to V.54. (V.17/V.33, V.29)
LL0	0:9:3	0	**Leased Line Chip 0.** Control bit LL0 selects leased or switched line transmitter operation. (V.22 bis, V.22)
LL1	1:9:3	0	**Leased Line Chip 1.** Control bit LL1 selects leased or switched line receiver operation. (V.22 bis, V.22)
MHLD	0:7:0	0	**Mark Hold.** Control bit MHLD is used to enable the transmitter to either clamp the digital input data to a mark or to take the input from TXD or TBUFFER (see TPDM).
NCIA0	0:1F:6	–	**NEWC0 Interrupt Active Chip 0.** Status bit NCIA0 is used to indicate NEWC0 caused $\overline{IRQ}$ to be asserted when enabled by the NCIE0 bit. (See NEWC0 and NCIE0.)
NCIA1	1:1F:6	–	**NEWC1 Interrupt Active Chip 0.** Status bit NCIA1 is used to indicate NEWC1 caused $\overline{IRQ}$ to be asserted when enabled by the NCIE1 bit. (See NEWC1 and NCIE1.)
NCIE0	0:1F:2	0	**NEWC0 Interrupt Enable Chip 0.** Control bit NCIE0 enables or disables assertion of $\overline{IRQ}$ and setting of NCIA0 when NCIA0 is set to a 1 by the modem. (See NEWC0 and NCIA0.)
NCIE1	1:1F:2	0	**NEWC1 Interrupt Enable Chip 1.** Control bit NCIE1 enables or disables assertion of $\overline{IRQ}$ and setting of NCIA1 when NCIA1 is set to a 1 by the modem. (See NEWC1 and NCIA1.)

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
NEWC0	0:1F:0	0	**New Configuration Chip 0.** Control bit NEWC0 must be set by the host after the host changes the configuration code in TCONF, the L3ACT bit, the ORG bit, the GTS bit, or the V21S0 bit. This informs the transmitter to implement the new transmitter configuration. The DSP resets the NEWC0 bit to a 0 when the configuration change is implemented. (See NCIE0 and NCIA0.)
NEWC1	1:1F:0	0	**New Configuration Chip 1.** Control bit NEWC1 must be set by the host after the host changes the configuration code in RCONF, the L3ACT bit, the RTH bit, the ORG bit, or the V21S1 bit. The DSP resets the NEWC1 bit to a 0 when the change is implemented. (See NCIE1 and NCIA1.)
NEWS0	0:1F:3	–	**New Status Chip 0.** Status bit NEWS0 is used to indicate one or more status bits located in registers 0E or 0F have changed state, or a DSP RAM read or write has been completed, in chip 0. The host may mask the effect of individual status bits upon NEWS0 by writing a mask value to DSP RAM. (See NSIE0 and NSIA0.)
NEWS1	1:1F:3	–	**New Status Chip 1.** Status bit NEWS0 is used to indicate one or more status bits located in registers 0A to 0F have changed state, or a DSP RAM read or write has been completed, in chip 1. The host may mask the effect of individual status bits upon NEWS1 by writing a mask value to DSP RAM. (See NSIE1 and NSIA1.)
NEWS2	2:1F:3	–	**New Status Chip 2.** Status bit NEWS0 is used to indicate the RI status bit in register 0F has changed state, or a DSP RAM read or write has been completed, in chip 2. The host may mask the effect of RI status bit upon NEWS2 by writing a mask value to DSP RAM. (See NSIE2 and NSIA2.)
NSIA0	0:1F:7	–	**NEWS0 Interrupt Active Chip 0.** Status bit NSIA0 is used to indicate NEWS0 bit caused $\overline{IRQ}$ to be asserted when enabled by the NSIE0 bit. (See NEWS0 and NSIE0.)
NSIA1	1:1F:7	–	**NEWS1 Interrupt Active Chip 1.** Status bit NSIA1 is used to indicate NEWS1 bit caused $\overline{IRQ}$ to be asserted when enabled by the NSIE1 bit. (See NEWS1 and NSIE1.)
NSIA2	2:1F:7	–	**NEWS2 Interrupt Active Chip 2.** Status bit NSIA2 is used to indicate NEWS2 bit caused $\overline{IRQ}$ to be asserted when enabled by the NSIE2 bit. (See NEWS2 and NSIE2.)
NSIE0	0:1F:4	0	**NEWS0 Interrupt Enable Chip 0.** Control bit NSIE0 enables or disables assertion of $\overline{IRQ}$ when NEWS0 is set to a 1 by the modem. (See NEWS0 and NSIA0.)
NSIE1	1:1F:4	0	**NEWS1 Interrupt Enable Chip 1.** Control bit NSIE1 enables or disables assertion of $\overline{IRQ}$ when NEWS1 is set to a 1 by the modem. (See NEWS1 and NSIA1.)
NSIE2	2:1F:4	0	**NEWS2 Interrupt Enable Chip 2.** Control bit NSIE2 enables or disables assertion of $\overline{IRQ}$ and the setting of NSIA2 when NEWS2 is set to a 1 by the modem. (See NEWS2 and NSIA2.)
NV25	0:9:7	0	**No V.25 Answer Tone.** Control bit NV25 is used to disable transmission of the 2100 Hz CCITT answer tone when a handshake sequence is initiated. (V.32 bis, V.32, V.22 bis, V.22, V.23, V.21)
ORG	0:9:4	1	**Originate.** Control bit ORG selects either originate or answer mode.
P2DET	1:D:7	–	**P2 Sequence Detected.** Status bit P2DET is used to indicate the receiver is detecting the P2 portion of the training sequence. (V.17/V.33, V.29, V.27 ter)
PEN0	0:6:3	0	**Parity Enable Chip 0.** Control bit PEN0 enables or disables parity in asynchronous mode in the transmitter. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
PEN1	1:6:3	0	**Parity Enable Chip 1.** Control bit PEN1 enables or disables parity in asynchronous mode in the receiver. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
PNDET	1:D:6	–	**PN Sequence Detected.** Status bit PNDET is used to indicate the receiver is detecting the PN portion of the training sequence. (V.17/V.33, V.29, V.27 ter)
RA	0:7:1	0	**Relay Activate.** Control bit RA activates or turns off the $\overline{OHRC}$ output.
RBUFFER	1:0:0–7	–	**Receive Buffer.** The host obtains channel data from the modem receiver in the parallel data mode by reading a data byte from the RBUFFER. The data is divided on the baud boundaries shown under TBUFFER. The RBUFFER reflects the received data when the RSEQ bit is a 0.
RCONF	1:12:0–7	74	**Receiver Configuration.** The RCONF control bits select the receiver configuration.
RDL	0:7:6	0	**Remote Digital Loopback.** Control bit RDL is used to cause the modem to initiate a V.22 bis request for the remote modem to go into digital loopback. (V.22 bis, Bell 212A/1200)
RDLE	1:7:7	1	**Remote Digital Loopback Response Enable.** Control bit RDLE is used to enable the modem to respond to another modem's V.22 bis remote digital loopback request, thus going into loopback. (V.22 bis, V.22, Bell 212A/1200)
RI	2:F:3	–	**Ring Indicator.** Status bit $\overline{RI}$ is used to indicate a ranging signal is being detected. Ringing is detected if pulses are present on the $\overline{RD}$ input in the 15 Hz–68 Hz frequency range. The $\overline{RI}$ bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time coincident with $\overline{RI}$ output signal. The decision bounds are host programmable in DSP RAM.

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
RLSD	1:F:7	–	**Received Line Signal Detector.** Status bit RLSD is used to indicate the receiver has finished receiving the training sequence, or has turned on due to detected energy above threshold, and is receiving data.
RLSDE	1:3:4	1	**RLSD Enable.** Control bit RLSDE enables the $\overline{\text{RLSD}}$ pin to either reflect the RLSD bit or to be clamped to a 1 (OFF condition) regardless of the state of the RLSD bit.
RREDT	2:E:5	–	**Rate Renegotiation Detected.** Status bit RREDT indicates V.32 bis rate renegotiation sequence detection status. (V.32 bis)
RREN	0:15:2	0	**Rate Renegotiation.** When the modem is in V.32 bis data mode and control bit RREN is set to a 1, a rate negotiation sequence is initiated. RREN resets to a 0 as soon as the initiation is acknowledged. (V.32 bis)
RRTSE	0:9:1	0	**Remote RTS Signalling Enable.** Control bit RRTSE is used to enable remote RTS signalling by sending either a pattern (idle pattern) produced by scrambling a binary 1 with the polynomial $1+x^{-3}+x^{-7}$ (RTS OFF) or a pattern of 8 bits (turn-on pattern) produced by scrambling a binary 0 with the polynomial $1+x^{-3}+x^{-7}$ (RTS ON) followed by the user data.
RSEQ	1:C:0	0	**Rate Sequence Received.** Status bit RSEQ is used to indicate the 16-bit rate sequence included in the V.32 bis/V.32 start-up procedure has been received and the 16-bit rate sequence word is available in RSEQM (1:1) and RSEQL (1:0). (V.32 bis, V.32)
RSEQL	1:0:0–7	–	**Rate Sequence LSB.** When the RSEQ bit is a 1, register 1:0 holds the least significant byte of the 16-bit V.32 bis/V.32 rate sequence word (RSEQL) received by the modem. When the RSEQ bit is a 0, register 1:0 holds the received data (see RBUFFER). (V.32 bis, V.32)
RSEQM	1:1:0–7	–	**Rate Sequence MSB.** When the RSEQ bit is a 1, register 1:1 holds the most significant byte of the 16-bit V.32 bis/V.32 rate sequence word (RSEQM) received by the modem. When the RSEQ bit is a 0, register 1:1 is not used. (V.32 bis, V.32)
RSPA	2:4:4	1	**Receiver Signal Point Activate.** Control bit RSPA is used to enable writing of the received signal point coordinates into registers RSPY (2:1) and RSPX (2:0). (V.32 bis, V.32, V.17/V.33, V.29, V.27 ter, V.22 bis, V.22, Bell 212A)
RSPX	2:0:0–7	–	**Receiver Signal Point X.** RSPX holds the X (in-phase) coordinate of the received signal point. RSPX is valid only when RSPA is a 1. (See RSPA.) (V.32 bis, V.32, V.17/V.33, V.29, V.27 ter, V.22 bis, V.22, Bell 212A)
RSPY	2:1:0–7	–	**Receiver Signal Point Y.** RSPY holds the Y (quadrature) coordinate of the received signal point. RSPY is valid only when RSPA is a 1. (See RSPA.) (V.32 bis, V.32, V.17/V.33, V.29, V.27 ter, V.22 bis, V.22, Bell 212A)
RTDET	1:E:7	–	**Retrain Detector.** Status bit RTDET is used to indicate a training sequence has been detected (V.32 bis, V.32 or V.22 bis). This bit parallels the operation of AADET (V.32 Answer) or S1DET (V.22 bis).
RTDIS	1:6:7	0	**Receiver Training Disable.** Control bit RTDIS is used to prevent the receiver from recognizing a training sequence and entering the training state. (V.17/V.33, V.29)
RTH	1:13:2,3	0	**Receiver Threshold.** The RTH control bits select the receiver energy detector threshold according to the following codes: RTH / RLSD ON / RLSD OFF 0 / – 43 dBm / – 48 dBm 1 / – 33 dBm / – 38 dBm 2 / – 26 dBm / – 31 dBm 3 / – 16 dBm / – 21 dBm
RTRN	0:8:1	0	**Retrain.** Control bit RTRN is used to initiate a retrain sequence. (V.32 or V.22 bis)
RTS	0:8:0	0	**Request to Send.** Control bit RTS enables the modem to transmit any data on TXD when CTS becomes active. In V.22 bis, V.22, V.23, V.21, and Bell 103 constant carrier and in V.32 bis/V.32 modes, RTS controls data transmission and DTR controls the carrier. For ease of use, RTS can be turned ON at the same time as DTR. In V.22 bis controlled carrier mode, RTS independently controls the carrier when DTR is ON. When RTS is turned ON, the modem then transmits 270 ms of scrambled 1s before turning CTS ON. In V.21, V.23 and Bell 103 controlled carrier modes, RTS independently controls the carrier when DTR is ON. When RTS is turned ON, CTS is turned ON per Table 2. The RTS bit parallels the operation of the $\overline{\text{RTS}}$ hardware control input. These inputs are ORed by the modem. (See descriptions of CTS and DTR bits.)

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
RTSDE	2:2:3	0	**Remote RTS Pattern Detector Enable.** Control bit RTSDE enables or disables the remote RTS pattern detector in the receiver. (See RTSDT).
RTSDT	2:F:1	–	**Remote RTS Pattern Detected.** Status bit RTSDT indicates the remote RTS signal is either ON or OFF. This status bit is valid only when RTSDE is a 1.
S1DET	1:D:5	–	**S1 Detector.** Status bit S1DET is used to indicate a V.22 bis S1 sequence has been detected. (V.22 bis)
SCR1	1:D:4	–	**Scrambled Ones Detector.** Status bit SCR1 is used to indicate V.22 bis scrambled 1s have been detected during handshake. (V.22 bis)
SDET	1:C:3	–	**S Detector.** Status bit SDET is used to indicate a V.32 bis/V.32 S sequence has been detected. (V.32 bis, V.32)
SDIS	0:3:2	0	**Scrambler Disable.** Control bit SDIS disables or enables the transmitter scrambler circuit. (V.32 bis, V.32, V.22 bis)
SEPT	0:3:6	0	**Short Echo Protector Tone.** Control bit selects an echo protector tone duration of 30 ms or 185 ms (see EPT). (V.17/V.33, V.29)
SHAP0	0:6:4	0	**Transmitter Shaping Filter Select.** Control bit SHAP0 enables the transmit spectrum to be shaped by either a square root of 12.5% raised cosine filter or a square root of 20% raised cosine filter. (V.32 bis, V.32, V.17/V.33, V.29)
SHAP1	1:6:4	0	**Receiver Shaping Filter Select.** Control bit SHAP1 enables the receiver low pass filter to be either a square root of 12.5% raised cosine filter or a square root of 20% raised cosine filter. (V.32 bis, V.32, V.17/V.33, V.29)
SNDET	1:C:2	–	**S Negative Detector.** Status bit SNDET is used to indicate the V.32 bis/V.32 $\overline{S}$ sequence has been detected. (V.32 bis, V.32)
SPEED	1:E:0–3	–	**Speed Indication.** The SPEED status bits indicate the receiver's data rate at the completion of a handshake.
SQDIS	1:2:6	0	**Squarer Disable (Tone Detector C).** Control bit SQDIS disables or enables the squarer in front of tone detector C.
STB0	0:6:2	0	**Stop Bit Number Chip 0.** Control bit STB0 selects either one or two stop bits in asynchronous mode in the transmitter. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
STB1	1:6:2	0	**Stop Bit Number Chip 1.** Control bit STB1 selects either one or two stop bits in asynchronous mode in the receiver. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
STOFF	0:5:1	0	**Soft Turn Off.** Control bit STOFF is used to enable to the transmitter to send a tone at the end of a transmission in V.23, V.21, and Bell 103 configurations. This tone is detected as a mark frequency at the receiver. The soft turn off tone frequencies and durations are as follows: Configuration / Frequency (Hz) / Duration (ms) V.23/1200 / 900 / 7 V.21 Originate / 880 / 30 V.21 Answer / 1550 / 30 Bell 103 Originate / 1370 / 30 Bell 103 Answer / 2325 / 30
STRN0	0:4:0	0	**Short Train Select Chip 0.** Control bit STRN0 selects short or long train mode. STRN0, STRN1, and STRN2 must be the same state. (V.17/V.33)
STRN1	1:4:0	0	**Short Train Select Chip 1.** Control bit STRN1 selects short or long train mode. (V.17/V.33)
STRN2	2:4:0	0	**Short Train Select Chip 2.** Control bit STRN2 selects short or long train mode. (V.17/V.33)
TBUFFER	0:0:0–7	00	**Transmitter Buffer.** The host conveys output data to the transmitter in the parallel mode by writing a data byte to the TBUFFER. Parallel data mode is available only in synchronous mode. The data is transmitted bit 0 first.
TCONF	0:12:0–7	74	**Transmitter Configuration.** The TCONF control bits select the transmitter configuration.
TDAE	1:2:7	1	**Tone Detector A Enable.** Control bit TDAE enables or disables tone detector A. This bit only has an effect when DATA1 bit is a 1 and the receiver is in asynchronous mode or V.32 12000 bps.
TLVL	0:13:4–7	0	**Transmit Level.** The TLVL code selects one of 16 transmitter analog output levels at the TXA pin between –0.5 dBm and –15.5 dBm ±0.5 dB. The host can fine tune the transmit level to a value lying within a 1 dB step by changing a value in DSP RAM.

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
TM	0:F:2	–	**Test Mode.** Status bit TM is used to indicate the modem has completed the handshake and is in RDL test mode. (V.22 bis)
TOD	2:4:1	0	**Train On Data.** Control bit TOD is used to enable the train-on-data algorithm to converge the equalizer if the signal quality degrades. (V.32 bis, V.32, V.17/V.33, V.29, V.27 ter)
TONEA	1:B:7	–	**Tone A Detected.** Status bit TONEA is used to indicate energy is present on the line within the tone detector A passband and above its threshold.
TONEB	1:B:6	–	**Tone B Detected.** Status bit TONEB is used to indicate energy is present on the line within the tone detector B passband and above its threshold.
TONEC	1:B:5	–	**Tone C Detected.** Status bit TONEC is used to indicate energy is present on the line within the tone detector C passband and above its threshold.
TPDM	0:8:6	0	**Transmitter Parallel Data Mode.** Control bit TPDM selects either parallel data mode (the transmitter accepts data for transmission from the TBUFFER, register 0:0) or serial data mode (the transmitter accepts data for transmission from the TXD pin).
TSPA	0:5:0	0	**Transmitter Signal Point Activate.** When control bit TSPA is a 1, the transmitter uses the signal points X and Y directly from registers TSPX (0:0) and TSPY (0:1). The transmitter data input, TBUFFER and TXD, are ignored. When TSPA is a 0, the transmitter accepts data for transmission from the TBUFFER or the TXD input.
TSPX	0:0:0–7	00	**Transmitter Signal Point X.** When TSPA is a 1, register 0:0 is used to transmit the in-phase (X) coordinate of the transmitted signal point (TSPX). (V.32 bis, V.32, V.17/V.33, V.29, V.27 ter, V.22 bis, V.22, Bell 212A)
TSPY	0:1:0–7	00	**Transmitter Signal Point Y.** When TSPA is a 1, register 0:1 is used to transmit the quadrature (Y) coordinate of the transmitted signal point (TSPY). (V.32 bis, V.32, V.17/V.33, V.29, V.27 ter, V.22 bis, V.22, Bell 212A)
TTDIS	0:5:2	0	**Transmitter Training Disable.** Control bit TTDIS enables or disables the generation of the training sequence at the start of transmission. With training disabled, the RTS/CTS delay is less than two baud times. (V.17/V.33, V.29)
TXCLK	0:13:0,1	0	**Transmit Clock Select.** Control bits TXCLK select the origin of the transmitter data clock, i.e., Internal, External (XTCLK), or Slave ($\overline{\text{RDCLK}}$). When the external clock option is chosen, an external clock must be supplied to the XTCLK input pin. The external clock signal must have a duty cycle of 50% and must be within ± 0.01% of the nominal TDCLK frequency (the actual frequency of TDCLK as measured when internal clock is selected). TDCLK will be phase locked to XTCLK when the external clock option is selected. When the slave clock is chosen, the transmitter clock (TDCLK) is phase locked to the receiver clock ($\overline{\text{RDCLK}}$).
TXSQ	0:5:4	0	**Transmitter Squelch.** Control bit TXSQ enables the transmitter analog output to be squelched or to function normally.
U1DET	1:D:3	–	**Unscrambled 1s Detector.** Status bit U1DET is used to indicate V.22 bis unscrambled 1s sequence has been detected. (V.22 bis)
V21	1:B:2	–	**V.21 Mark Detector.** Status bit V21 is used to indicate a V.21 mark frequency was detected during a handshake. (V.21)
V21S0	0:8:5	0	**V21 Synchronous Chip 0.** Control bit V21S0 selects synchronous or asynchronous mode in the transmitter. (V.21)
V21S1	1:8:5	0	**V21 Synchronous Chip 1.** Control bit V21S1 selects synchronous or asynchronous mode in the receiver chip 1. Synchronous data is output in both serial or parallel form. (V.21)
V32BDT	2:E:4	–	**V.32 bis Rate Sequence Detected.** Status bit V32BDT indicates V.32 bis rate sequence detection status. (V.32 bis, V.32)
V32BS0	0:4:5	0	**V.32 bis Select Chip 0.** Control bit V32BS0 selects the V.32 bis or V.32 operating mode. The EARC0 bit is valid only when V32BS0 is a 0. (V.32 bis, V.32)
V32BS1	1:4:5	0	**V.32 bis Select Chip 1.** Control bit V32BS1 selects the V.32 bis or V.32 operating mode. The EARC1 bit is valid only when V32BS1 is a 0. (V.32 bis, V.32)
V54A	0:8:3	0	**V.54 Acknowledgement Signalling.** Control bit V54A is used to enable sending of a pattern of 1948 bits produced by scrambling a binary 1 with the polynomial $1+x^{-4}+x^{-7}$ per V.54 at the modem data signalling rate. (Not valid in FSK modes.)

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
V54AE	2:2:1	0	**V.54 Acknowledgement Phase Detector Enable.** Control bit V54AE enables or disables the V.54 acknowledgement phase detector in the receiver. (See V54DT). (Not valid in FSK modes.)
V54DT	2:F:0	0	**V.54 Pattern Detected.** Status bit V54DT is used to indicate one of the three V.54 patterns is being detected. (Not valid in FSK modes.)
V54P	0:8:2	0	**V.54 Preparatory Signalling.** Control bit V54P is used to enable the sending of a pattern of 2048 bits produced by scrambling a binary 0 with the polynomial $1+x^{-4}+x^{-7}$ per V.54 at the modem data signalling rate. (Not valid in FSK modes.)
V54PE	2:2:0	0	**V.54 Preparatory Phase Detector Enable.** Control bit V54PE enables or disables the V.54 preparatory phase detector in the receiver. (Not valid in FSK modes.)
V54T	0:8:4	0	**V.54 Termination Signalling.** Control bit V54T is used to enable the sending of a pattern of 8192 bits produced by scrambling a binary 1 with the polynomial $1+x^{-4}+x^{-7}$ followed by 64 binary 1s per V.54 at the modem signalling rate. (Not valid in FSK modes.)
V54TE	2:2:2	0	**V.54 Termination Phase Detector Enable.** Control bit V54TE enables or disables the V.54 termination phase detector in the receiver. (See V54DT). (Not valid in FSK modes.)
WDSZ0	0:6:0,1	0	**Data Word Size Chip 0.** The WDSZ0 field selects a word size of 5, 6, 7, or 8 data bits per character in asynchronous mode in the transmitter. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
WDSZ1	1:6:0,1	0	**Data Word Size Chip 1.** The WDSZ1 field selects a word size of 5, 6, 7, or 8 data bits per character in asynchronous mode in the receiver. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
XACC0	0:1D:7	0	**X RAM Access Enable Chip 0.** Control bit XACC0 is used to enable the modem to access the X RAM associated with the address in the XADD0 and XCR0 bits. XWT0 controls read or write.
XACC1	1:1D:7	0	**X RAM Access Enable Chip 1.** Control bit XACC1 is used to enable the modem to access the X RAM associated with the address in the XADD1 and XCR1 bits. XWT1 controls read or write.
XACC2	2:1D:7	0	**X RAM Access Enable Chip 2.** Control bit XACC2 is used to enable the modem to access the X RAM associated with the address in the XADD2 and XCR2 bits. XWT2 controls read or write.
XADD0	0:1C:0–7	00	**X RAM Address Chip 0.** XADD0 contains the X RAM address for accessing X Data RAM or X Coefficient RAM in chip 0 via the X RAM Data LSB and MSB registers (0:18 and 0:19, respectively)
XADD1	1:1C:0–7	00	**X RAM Address Chip 1.** XADD1 contains the X RAM address for accessing X Data RAM or X Coefficient RAM in chip 1 via the X RAM Data LSB and MSB registers (1:18 and 1:19, respectively)
XADD2	2:1C:0–7	00	**X RAM Address Chip 2.** XADD2 contains the X RAM address for accessing X Data RAM or X Coefficient RAM in chip 2 via the X RAM Data LSB and MSB registers (2:18 and 2:19, respectively)
XCR0	0:1D:0	0	**X Coefficient RAM Select Chip 0.** Control bit XCR0 enables or disables the XADD0 address to access X Coefficient RAM or X Data RAM in chip 0.
XCR1	1:1D:0	0	**X Coefficient RAM Select Chip 1.** Control bit XCR1 enables or disables the XADD1 address to access X Coefficient RAM or X Data RAM in chip 1.
XCR2	2:1D:0	0	**X Coefficient RAM Select Chip 2.** Control bit XCR2 enables or disables the XADD2 address to access X Coefficient RAM or X Data RAM in chip 2.
XCRD0	0:1D:2	0	**X RAM Continuous Read Chip 0.** Control bit XCRD0 enables or disables continuous X RAM read from chip 0.
XCRD1	1:1D:2	0	**X RAM Continuous Read Chip 1.** Control bit XCRD1 enables or disables continuous X RAM read from chip 1.
XCRD2	2:1D:2	0	**X RAM Continuous Read Chip 2.** Control bit XCRD2 enables or disables continuous X RAM read from chip 2.
XDAL0	0:18:0–7	00	**X RAM Data LSB Chip 0.** XDAL0 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 0.
XDAL1	1:18:0–7	00	**X RAM Data LSB Chip 1.** XDAL1 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 1.
XDAL2	2:18:0–7	00	**X RAM Data LSB Chip 2.** XDAL2 is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 2.
XDAM0	0:19:0–7	00	**X RAM Data MSB Chip 0.** XDAM0 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 0.
XDAM1	1:19:0–7	00	**X RAM Data MSB Chip 1.** XDAM1 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 1.
XDAM2	2:19:0–7	00	**X RAM Data MSB Chip 2.** XDAM2 is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in DSP chip 2.

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
XWT0	0:1D:1	0	**X RAM Write Chip 0.** Control bit XWT0 enables the modem to write data from the X RAM Data registers (0:18 and 0:19) into an X RAM location, or to read data from an X RAM location and store it into the X RAM Data registers (0:18 and 0:19). The X RAM is addressed by XADD0 and XCR0.
XWT1	1:1D:1	0	**X RAM Write Chip 1.** Control bit XWT1 enables the modem to write data from the X RAM Data registers (1:18 and 1:19) into an X RAM location, or to read data from an X RAM location and store it into the X RAM Data registers (1:18 and 1:19). The X RAM is addressed by XADD1 and XCR1.
XWT2	2:1D:1	0	**X RAM Write Chip 2.** Control bit XWT2 enables the modem to write data from the X RAM Data registers (2:18 and 2:19) into an X RAM location, or to read data from an X RAM location and store it into the X RAM Data registers (2:18 and 2:19). The X RAM is addressed by XADD2 and XCR2.
YACC0	0:1B:7	0	**Y RAM Access Enable Chip 0.** Control bit YACC0 enables or disables the modem to access the Y RAM associated with the address in the YADD0 and YCR0 bits. YWT0 controls read or write.
YACC1	1:1B:7	0	**Y RAM Access Enable Chip 1.** Control bit YACC1 enables or disables the modem to access the Y RAM associated with the address in the YADD1 and YCR1 bits. YWT1 controls read or write.
YACC2	2:1B:7	0	**Y RAM Access Enable Chip 2.** Control bit YACC2 enables or disables the modem to access the Y RAM associated with the address in the YADD2 and YCR2 bits. YWT2 controls read or write.
YADD0	0:1A:0–7	00	**Y RAM Address Chip 0.** YADD0 contains the Y RAM address for accessing Y Data RAM or Y Coefficient RAM in chip 0 via the Y RAM Data LSB and MSB registers (0:16 and 0:17, respectively).
YADD1	1:1A:0–7	00	**Y RAM Address Chip 1.** YADD1 contains the Y RAM address for accessing Y Data RAM or Y Coefficient RAM in chip 1 via the Y RAM Data LSB and MSB registers (1:16 and 1:17, respectively).
YADD2	2:1A:0–7	00	**Y RAM Address Chip 2.** YADD2 contains the Y RAM address used to access Y Data RAM or Y Coefficient RAM in chip 2 via the Y RAM Data LSB and MSB registers (2:16 and 2:17, respectively).
YCR0	0:1B:0	0	**Y Coefficient RAM Select Chip 0.** Control bit YCR0 is used to enable the YADD0 address to access Y Coefficient RAM or Y Data RAM.
YCR1	1:1B:0	0	**Y Coefficient RAM Select Chip 1.** Control bit YCR1 is used to enable the YADD1 address to access Y Coefficient RAM or Y Data RAM.
YCR2	2:1B:0	0	**Y Coefficient RAM Select Chip 2.** Control bit YCR2 is used to enable the YADD2 address to access Y Coefficient RAM or Y Data RAM.
YCRD0	0:1B:2	0	**Y RAM Continuous Read Chip 0.** Control bit YCRD0 enables continuous Y RAM read from chip 0.
YCRD1	1:1B:2	0	**Y RAM Continuous Read Chip 1.** Control bit YCRD1 enables continuous Y RAM read from chip 1.
YCRD2	2:1B:2	0	**Y RAM Continuous Read Chip 2.** Control bit YCRD2 enables continuous Y RAM read from chip 2.
YDAL0	0:16:0–7	00	**Y RAM Data LSB Chip 0.** YDAL0 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 0.
YDAL1	1:16:0–7	00	**Y RAM Data LSB Chip 1.** YDAL1 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 1.
YDAL2	2:16:0–7	00	**Y RAM Data LSB Chip 2.** YDAL2 is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM location in DSP chip 2.
YDAM0	0:17:0–7	00	**Y RAM Data MSB Chip 0.** YDAM0 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 0.
YDAM1	1:17:0–7	00	**Y RAM Data MSB Chip 1.** YDAM1 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 1.
YDAM2	2:17:0–7	00	**Y RAM Data MSB Chip 2.** YDAM2 is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in DSP chip 2.
YWT0	0:1B:1	0	**Y RAM Write Chip 0.** Control bit YWT0 enables the modem to write data from the Y RAM Data registers (0:16 and 0:17) into an Y RAM location, or to read data from an Y RAM location and store it into the Y RAM Data registers (0:16 and 0:17). The Y RAM is addressed by YADD0 and YCR0.
YWT1	1:1B:1	0	**Y RAM Write Chip 1.** Control bit YWT1 enables the modem to write data from the Y RAM Data registers (1:16 and 1:17) into an Y RAM location, or to read data from an Y RAM location and store it into the Y RAM Data registers (1:16 and 1:17). The Y RAM is addressed by YADD1 and YCR1.
YWT2	2:1B:1	0	**Y RAM Write Chip 2.** Control bit YWT2 enables the modem to write data from the Y RAM Data registers (2:16 and 2:17) into an Y RAM location, or to read data from an Y RAM location and store it into the Y RAM Data registers (2:16 and 2:17). The Y RAM is addressed by YADD2 and YCR2.

Table 11. Interface Memory RAM Addresses

No.	Function	Chip No.	Address Code: Real Part (X)	Address Code: Imag. Part (Y)	CR Bit[1]	No.	Function	Chip No.	Address Code: Real Part (X)	Address Code: Imag. Part (Y)	CR Bit[1]
1	Transmitter Compromise Equalizer Coefficients:					29	V.23 Receiver Compromise Equalizer Coefficients				
	First Tap	0	5B	--	1		Tap 1	1	76	--	1
	Last Tap	0	34	--	1		Tap 20	1	63	--	1
	Number of Taps	0	35	--	0		Tap 21	1	F6	--	1
2	Rate Sequence	0	93	--	1		Tap 40	1	E3	--	1
3	DTMF Tone Duration	0	9A	--	1	30	RLSD Threshold	1	01	--	0
4	DTMF Interdigit Delay	0	1A	--	1	31	Receiver Chip 1 New Status Bit (NEWS1)				
5	DTMF Low Band Power Level	0	19	--	1		Masking Register for 1:A and 1:B	1	9B	--	1
6	DTMF High Band Power Level	0	99	--	1		Masking Register for 1:C and 1:D	1	9C	--	1
7	Pulse Relay Make Time	0	9C	--	1		Masking Register for 1:E and 1:F	1	9D	--	1
8	Pulse Relay Break Time	0	1C	--	1	32	Received Signal Samples	1	03	--	0
9	Pulse Interdigit Delay	0	1B	--	1	33	Demodulator Output	1	04	84	0
10	Transmitter Output Level Gain Constant	0	99	--	0	34	Low Pass Filter Output	1	00	80	0
11	Dual Tone 1 Frequency	0	87	--	0	35	Average Energy	1	02	--	0
12	Dual Tone 2 Frequency	0	8A	--	1	36	AGC Gain Word	1	01	--	1
13	Dual Tone 1 Power Level	0	02	--	0	37	Timing Recovery Update	1	25	--	0
14	Dual Tone 2 Power Level	0	82	--	0	38	Round Trip Far Echo Delay	1	15	--	1
15	Transmitter New Status Bit (NEWS0)					39	Equalizer Input	2	18	98	0
	Masking Register for 0:E and 0:F	0	11	--	1	40	Equalizer Tap Coefficients:				
16	Total Span of Echo Canceller	0	9D	--	0		First Tap	2	18	98	1
17	Echo Canceller Dividing Point	0	A0	--	0		Last Tap	2	47	C7	1
18	Far End Echo Canceller Center Tap Position	0	24	--	0	41	Unrotated Equalizer Output	2	01	81	0
						42	Rotated Equalizer Output (Received Points)	2	02	82	1
19	Echo Canceller Update Coefficient (Training Mode)	0	24	--	1	43	Decision Points (Ideal Points)	2	02	82	0
20	Echo Canceller Update Coefficient (Data Mode)	0	A4	--	1	44	Equalizer Error	2	03	83	0
						45	Equalizer Rotation Angle	2	87	--	1
21	CTS OFF-to-ON Response Time (RTS–CTS Delay)	0	10	--	1	46	Equalizer Frequency Correction	2	0A	--	1
						47	Eye Quality Monitor (EQM)	2	07	--	1
22	Bulk Delay	0	9E	--	0	48	Maximum Period of Valid Ring Signal	2	17	--	0
23	Echo Canceller Error	0	20	--	0	49	Minimum Period of Valid Ring Signal	2	97	--	0
24	Far End Echo Frequency Offset	0	20	--	1	50	Receiver Chip 2 New Status Bit (NEWS2)				
25	Far End Echo Level	0	25	--	0		Masking Register for 2:E and 2:F	2	75	--	0
26	Tone Detector A Bandpass Filter Coefficients	1	26	--	1						
27	Tone Detector B Bandpass Filter Coefficients	1	2C	--	1						
28	Tone Detector C Bandpass Filter Coefficients	1	32	--	1						

Note: 1. CR corresponds to XCR0, YCR0, XCR1, YCR1, XCR2, or YCR2 depending on the chip number and address code.