P54/74FCT640T/AT/CT—P54/74FCT643T/AT/CT OCTAL BIDIRECTIONAL TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES

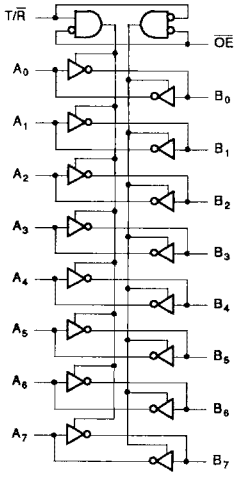
- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 4.4ns max. (Com'l) FCT-A speed at 5.0ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **ESD protection exceeds 2000V**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **3-State Outputs**
- **Manufactured in 0.7 micron PACE Technology™**

DESCRIPTION

The 'FCT640T, 'FCT643T contain eight bidirectional buffers with 3-state outputs and is intended for bus oriented applications. Current sinking capability is 64 mA at the A & B ports. The 'FCT640T and 'FCT643T are identical except for the non-inversion on the B port for the 'FCT643T.

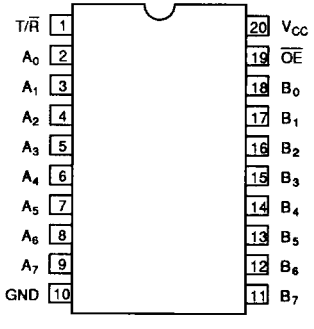
The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (Active HIGH) enables data from A ports to B ports; receive (Active LOW) enables data from B ports to A ports. The output enable input, when HIGH, disables both the A and B ports by putting them in a high Z condition.

LOGIC BLOCK DIAGRAM

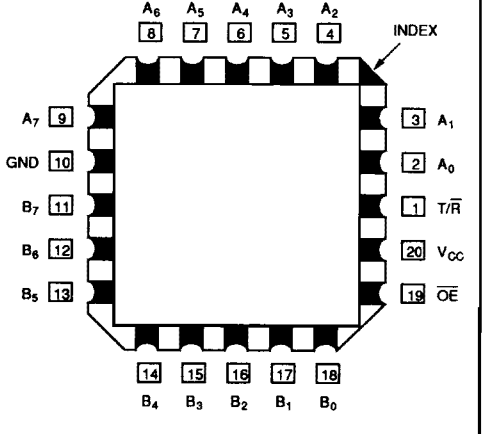


PIN CONFIGURATIONS

'FCT640T



DIP (D2, P2), SOIC (S2)



LCC (L2)

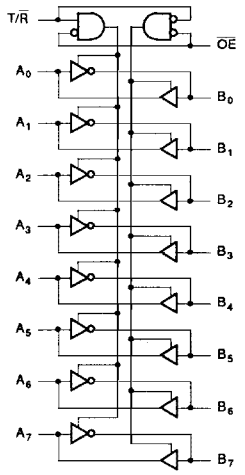
1726 01

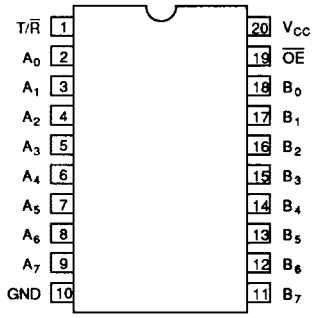
7

LOGIC BLOCK DIAGRAM

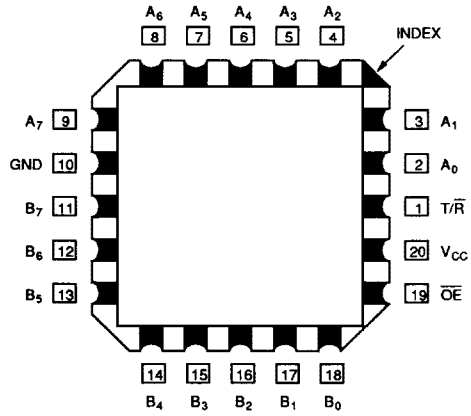
PIN CONFIGURATIONS

'FCT643T





DIP (D2, P2), SOIC (S2)



LCC (L2)

1726 02

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1726 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1726 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min.	Max.
Military	–55°C	+125°C
Commercial	0°C	+70°C

1726 Tbl 03

Supply Voltage (V_{CC})	Min.	Max.
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1726 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[3]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –15mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –24mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	V_{IN} = V_{CC}
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1726 Tbl 05

Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, T/$\overline{R}$ = $\overline{OE}$ = GND and $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V,
I_C	Total Power Supply Current[5]	2.0	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, T/$\overline{R}$ = $\overline{OE}$ = GND and $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.3	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, T/$\overline{R}$ = $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND
		3.5	6.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, T/$\overline{R}$ = $\overline{OE}$ = GND and $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		5.5	14.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, T/$\overline{R}$ = $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND

1726 Tbl 06

Notes:
1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLES

'FCT640T		
Enable $\overline{OE}$	Direction Control T/$\overline{R}$	Operation
L	L	$\overline{B}$ Data to Bus A
L	H	$\overline{A}$ Data to Bus B
H	X	High Z State

1726 Tbl 07

'FCT643T		
Enable $\overline{OE}$	Direction Control T/$\overline{R}$	Operation
L	L	B Data to Bus A
L	H	$\overline{A}$ Data to Bus B
H	X	High Z State

1726 Tbl 08

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care

AC CHARACTERISTICS

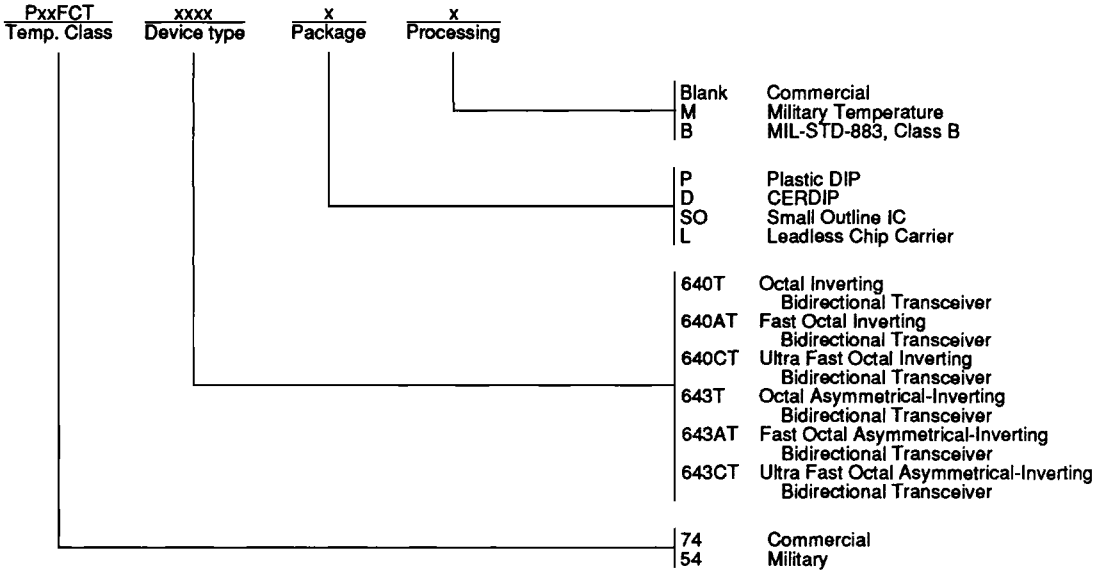
Symbol	Parameter	'FCT640T 'FCT643T				'FCT640AT 'FCT643AT				'FCT640CT 'FCT643CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.5	8.0	1.5	7.0	1.5	5.3	1.5	5.0	1.5	4.7	1.5	4.4	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ or T/$\overline{R}$ to A or B	1.5	16.0	1.5	13.0	1.5	6.5	1.5	6.2	1.5	6.2	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ or T/$\overline{R}$ to A or B	1.5	12.0	1.5	10.0	1.5	6.0	1.5	5.0	1.5	5.2	1.5	4.8	ns	1, 7, 8

1726 Tbl 09

Note:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
   AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

ORDERING INFORMATION



1726 03

7