

NJW1102

PRELIMINARY

The NJW1102 is a monolithic BICMOS IC designed for use not only in Dolby Pro-Logic Surround but also in other types of surround systems such as HALL, MATRIX, SIMULATED, etc.. This IC incorporates all functions, necessary for Dolby Pro-Logic and other surround types except time delay. The NJW1102 features serial data control for all functions including center and surround channel level trim.

Dolby® and the double-D symbol are trademarks of Dolby Laboratories Licensing Corporation, San Francisco, CA 94103-4813, USA.
This device is available only to licensees of Dolby Labs. Licensing and application information may be obtained from Dolby Labs.

■ Features

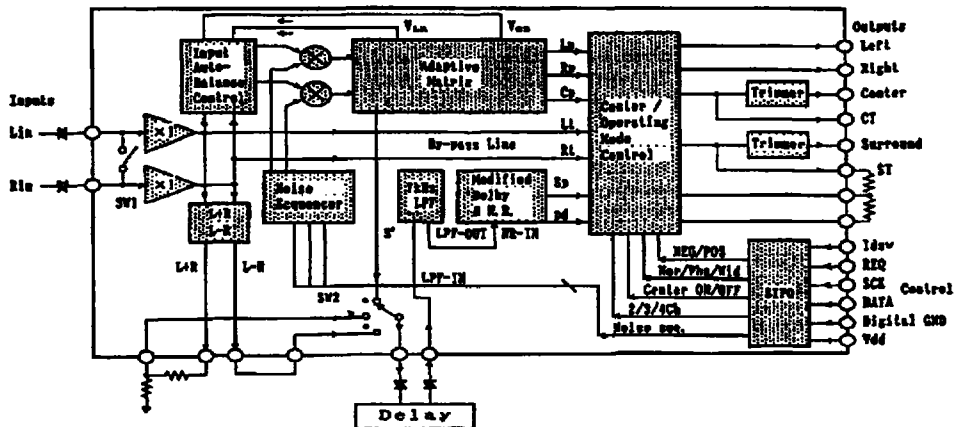
Dolby Operating Level: 300mVrms
Operating Supply Voltage Range: 5V and 9V ~ 13V, or $\pm 5V$
Level Trim: -15 to 15dB/1dB step (-15 to 3dB/1dB step at Pro-Logic Mode)
Internal Mode Control Switches

■ Package Outline

■ Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Supply Voltage	V_{CC}	13.0 V
	V_{DD}	6.5V
Power Dissipation	P_D	SDIP: 700 mW QFP: 1,000 mW
Operating Temperature Range	T_{OPR}	$-20 \sim 75^\circ\text{C}$
Storage Temperature Range	T_{STG}	$-40 \sim 125^\circ\text{C}$

■ Active Surround Decoder Block Diagram



■ Electrical Characteristics

(Ta=25 °C, V_{CC}=10V, V_{DD}=5V, 0dB Reference is 300mVrms/1kHz at Cch out, unless otherwise specified (Cch trimmer=0dB.))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL						
Supply Voltage Range	V _{CC}		9	10	12	V
	V _{DD}		4.5	5.0	5.5	V
Supply Current	I _{CC}	No Signal	25	35	45	mA
	I _{DD}	No Signal	0.45	0.60	0.75	mA
Reference Voltage	V _{ref}	No Signal	3.6	4.0	4.4	V
Threshold Voltage	V _{thh}	Digital Input "H" Level	0.7V _{DD}		V _{DD}	V
	V _{thl}	Digital Input "L" Level	0		0.3 V _{DD}	V
INPUT SHORT SWITCH						
Resistance	R _{ON}	Input Short		150	500	Ω
Switch Crosstalk	SC	V _{IN} =15dB, f=1kHz		-60		dB
INPUT AUTO BALANCE						
Capture Range	CPR			±5		dB
Error Correction	CER			±5		dB
ADAPTIVE MATRIX						
Output Level Accuracy relative to Cch	ΔV _{ol}	L, R, S'ch out	-0.5	0.0	0.5	dB
Matrix Rejection Relative	MR	L, R, C, S'ch out	25	40		dB
Headroom	HRAM	V _{CC} =9V at THD=1%	15	17		dB
Total Harmonic Distortion	THDAM	L, R, C, S'ch out at 4ch mode		0.05	0.20	%
		L, Rch out at 2ch mode		0.01	0.10	%
Signal-to-Noise Ratio	SNAM	Rg=0, weighted: CCIR/ARM at 4ch mode	75	80		dB
		L, Rch out at 2ch mode	93	100		dB
NOISE SEQUENCER						
Output Noise Level	V _{no}		-15.0	-12.5	-10.0	dB
Output Noise Level Accuracy relative to Cch	ΔV _{no}	L, R, S'ch out	-0.5	0.0	0.5	dB
MODIFIED B TYPE NOISE REDUCTION (0dB Reference is input level at NR-IN when adjust to 300mV/100Hz at Sch out (Sch trimmer=0dB.))						
Voltage Gain	VGNR	V _{IN} =0dB, f=100Hz		9.0		dB
Decode Response 1	DEC1	V _{IN} =0dB, f=1.0kHz	-1.6	-0.1	1.4	dB
Decode Response 2	DEC2	V _{IN} =-15dB, f=1.4kHz	-3.0	-1.5	0.0	dB
Decode Response 3	DEC3	V _{IN} =-20dB, f=1.4kHz	-4.9	-3.4	-1.9	dB
Decode Response 4	DEC4	V _{IN} =-40dB, f=5.0kHz	-6.8	-5.3	-3.8	dB
Total Harmonic Distortion	THDNR	V _{IN} =0dB, f=1.0kHz		0.07	0.30	%
Headroom	HRNR	V _{CC} =9V at THD=1%	15	17		dB
Signal-to-Noise Ratio	SNNR	Rg=0, weighted: CCIR/ARM	73	78		dB
OTHER SURROUND						
Total Harmonic Distortion	THDOS	V _{IN} =0dB, f=1.0kHz, L+R, L-R output		0.05	0.20	%
Headroom	HROS	V _{CC} =9V at THD=1%, L+R, L-R output	15	17		dB
Signal-to-Noise Ratio	SNOS	Rg=0, weighted: CCIR/ARM, L+R, L-R output	75	80		dB
Adder Gain	AG			0		dB
C, Sch TRIMMER						
Trim Range	TR		±12	±15	±18	dB
Trim Step	TS		0.6	1.0	1.4	dB

Pin Configuration

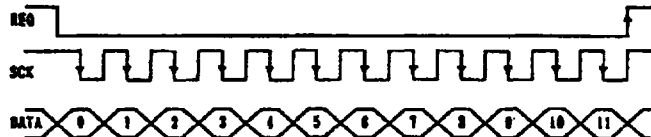
Pin	SDIP	QFP	Pin	SDIP	QFP	Pin	SDIP	QFP	Pin	SDIP	QFP
1	RLC2	LLI	17	VCC	NC	33	CMC	SMRI	49	DBC3	NC
2	RLC1	LBPF	18	NGC3	DATA	34	SMRO	NC	50	PSC3	PSC3
3	RLC4	RLI	19	NGC2	SCK	35	SMRI	SD	51	PSC6	PSC6
4	RLC7	RBPF	20	NGC1	REQ	36	SD	SIMB	52	PSC2	PSC2
5	RLC3	LT	21	VDD	IDS	37	SIMB	SIMA	53	PSC5	PSC5
6	RLC8	RT	22	DATA	VSS	38	SIMA	L+R	54	PSC1	PSC1
7	RLC6	LIN	23	SCK	LOUT	39	L+R	L-R	55	PSC4	PSC4
8	LLI	RIN	24	REQ	ROUT	40	L-R	GND	56	RLC5	RLC5
9	LBPF	HOLDC	25	IDS	NC	41	GND	VREF	57	-----	RLC2
10	RLI	VCC	26	VSS	CT	42	VREF	VREFG	58	-----	RLC1
11	RBPF	NGC3	27	LOUT	COUT	43	VREFG	IREF	59	-----	RLC4
12	LT	NGC2	28	ROUT	ST	44	IREF	DBIN	60	-----	RLC7
13	RT	NGC1	29	CT	SOUT	45	DBIN	LPIN	61	-----	RLC3
14	LIN	NC	30	COUT	CMC	46	LPIN	DBC1	62	-----	RLC8
15	RIN	NC	31	ST	SMRO	47	DBC1	DBC2	63	-----	RLC6
16	HOLDC	VDD	32	SOUT	NC	48	DBC2	DBC3	64	-----	NC



■ External Parts List

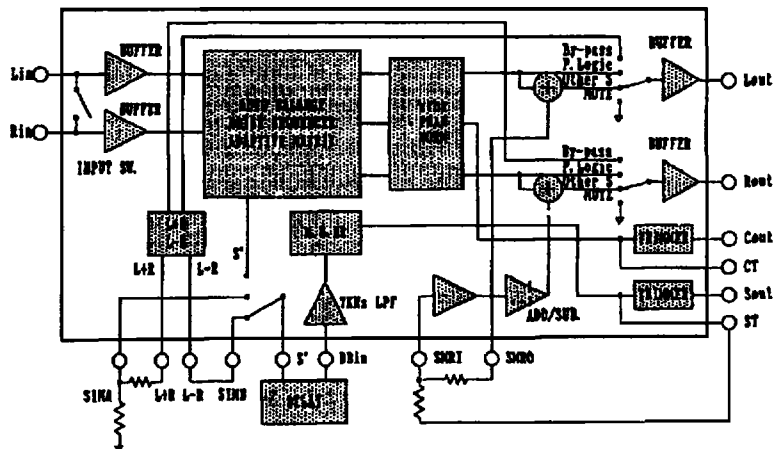
Parts No.	Value	Unit	Tolerance	Comment	Parts No.	Value	Unit	Tolerance	Comment
C10	100	μF		≥100 μF	C131	4.7	nF	10%	
C11	220	μF		≥150 μF	C132	5.6	nF	10%	
C12	100	μF		≥100 μF	C133	5.6	nF	5%	
C101	10	μF			C134	47	nF	5%	
C102	10	μF			C135	680	nF	10%	
C103	22	μF	20%	Low Leak	C136	100	nF	10%	
C104	10	μF			C137	10	μF		
C105	4.7	nF	5%		C138	10	μF		
C106	22	μF	10%		C139	10	μF		
C107	680	pF	5%		C140	10	μF		
C108	100	nF	5%						
C109	100	nF	5%		R10	10	kΩ	Selectable Total ≥10kΩ	
C110	680	pF	5%		R11	4.7	kΩ		
C111	100	nF	5%		R12	1	kΩ		≥1kΩ
C112	100	nF	5%		R13	10	kΩ		≥10kΩ
C113	47	nF	5%		R101	22	kΩ	1%	
C114	47	nF	5%		R102	22	kΩ	1%	
C115	22	nF	5%		R103	4.7	kΩ	10%	
C116	100	nF	20%		R104	100	kΩ	5%	
C117	100	nF	20%		R105	47	kΩ	5%	
C118	100	nF	20%		R106	15	kΩ	5%	
C119	100	nF	20%		R107	7.5	kΩ	5%	
C120	22	nF	5%		R108	47	kΩ	5%	
C121	220	nF	10%		R109	15	kΩ	5%	
C122	4.7	μF	20%		R110	7.5	kΩ	5%	
C123	220	nF	10%		R111	100	kΩ	1%	
C124	220	nF	10%		R112	8.2	kΩ	5%	
C125	4.7	μF	20%		R113	15	kΩ	5%	
C126	220	nF	10%		R114	8.2	kΩ	5%	
C127	10	μF			R115	8.2	kΩ	5%	
C128	10	μF			R116	330	kΩ	10%	
C129	10	μF							
C130	470	pF	10%						

BIT	0	1	2	3	4	5	6	7	8	9	10	11
	DATA					ADDRESS			ID CODE			

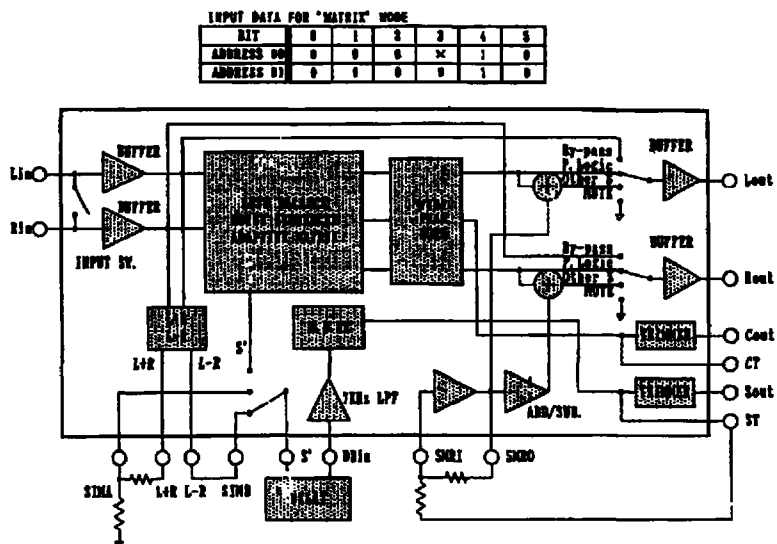


● HALL

INPUT DATA FOR "HALL" MODE						
BIT	0	1	2	3	4	5
ADDRESS 00	0	0	0	1	1	0
ADDRESS 01	1	0	0	0	1	0



● MATRIX



● SIMULATED

