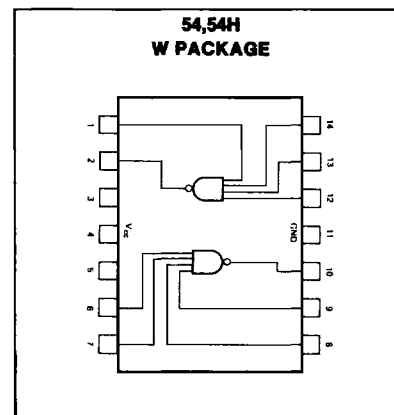
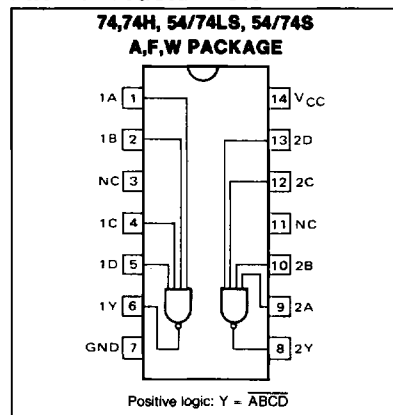


SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

TEST CONDITIONS	54/74			54/74H			54/74LS			54/74S			
	$C_L = 15\text{pF}$ $R_L = 133\Omega$			$C_L = 25\text{pF}$ $R_L = 93\Omega$			$C_L = 45\text{pF}$ $R_L = 667\Omega$			$C_L = 50\text{pF}$ $R_L = 93\Omega$			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		13	22		8.5	12		12	24	2	4 $C_L = 150\text{pF}$ 6	6.5	ns
t_{PHL} High-to-low		8	15		6.5	12		12	24	2	4 $C_L = 150\text{pF}$ 6	6.5	ns

Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

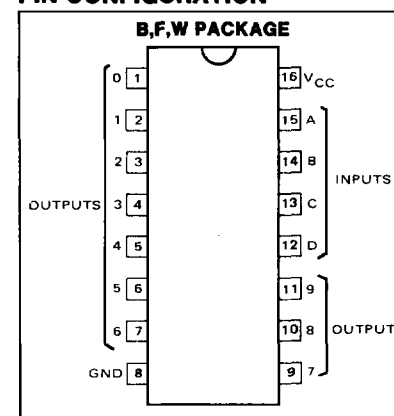
54	F,W	74	B,F
54LS	F,W	74LS	B,F

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

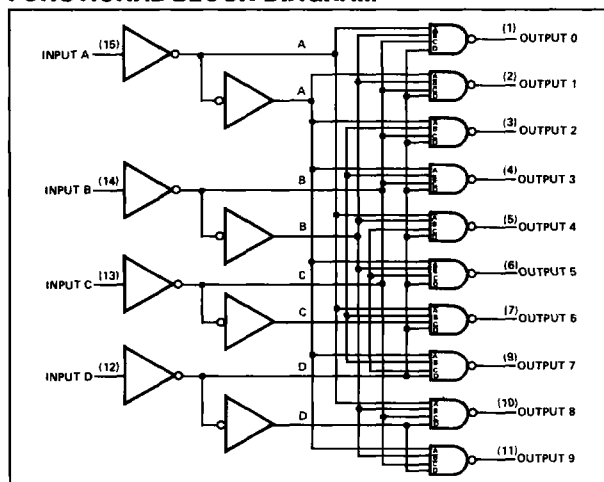
TEST CONDITIONS			54/74			54/74LS			
			$C_L = 15pF$ $R_L = 400\Omega$			$C_L = 15pF$ $R_L = 2K\Omega$			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high	A,B,C,D	through 2 logic levels		10	25		10	25	ns
t_{PHL} High-to-low				14	25		14	25	
t_{PLH} Low-to-high	A,B,C,D	through 3 logic levels		17	30		17	30	ns
t_{PHL} High-to-low				17	30		17	30	

Load circuit and waveforms shown at front of section (totem pole outputs).

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H

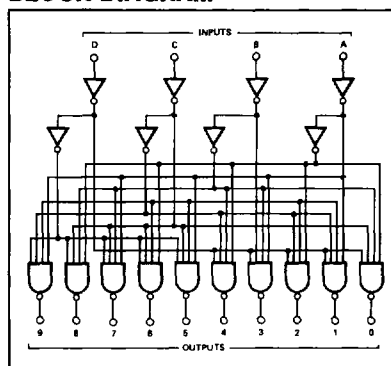
H = high level, L = low level

EXCESS 3-TO-DECIMAL DECODER

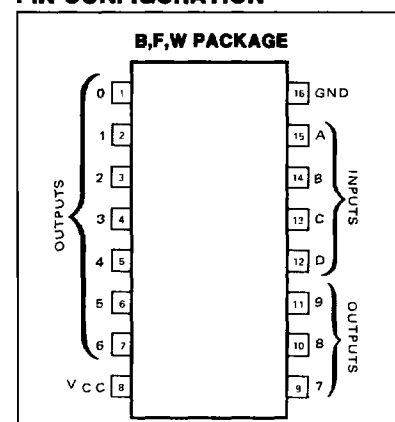
SPEED/PACKAGE AVAILABILITY

54 F,W, 74 B,F

BLOCK DIAGRAM



PIN CONFIGURATION

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25^\circ C$

TEST CONDITIONS			54/74			
			C _L = 15pF R _L = 400Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time						
t _{PLH} Low-to-high		through 2 logic levels	10	17	25	ns
t _{PHL} High-to-low			10	22	30	
t _{PLH} Low-to-high		through 3 logic levels		26	35	ns
t _{PHL} High-to-low				23	35	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE-EXCESS INPUT

D	C	B	A
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
0	0	0	0
0	0	0	1
0	0	1	0

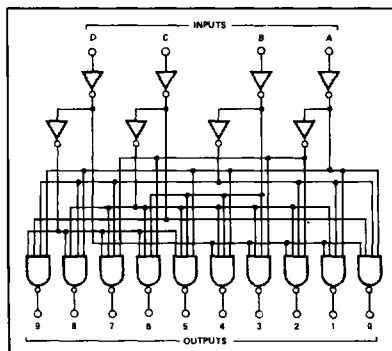
DECIMAL OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

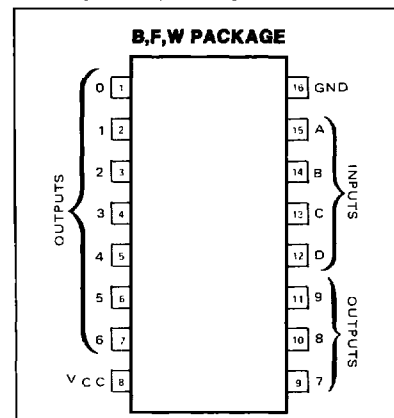
SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC}=5V, T_A=25^{\circ}C$

TEST CONDITIONS			54/74			
			$C_L = 15pF$ $R_L = 400\Omega$			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time						
t_{PLH} Low-to-high		through 2 logic levels	10	17	25	ns
t_{PHL} High-to-low			10	22	30	
t_{PLH} Low-to-high		through 3 logic levels		26	35	ns
t_{PHL} High-to-low				23	35	

Load circuit and typical waveforms are shown at the front of section.

01601

TRUTH TABLE-EXCESS INPUT

D	C	B	A
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0
0	0	0	0
0	0	0	1
0	0	1	1

DECIMAL OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

BCD-TO-DECIMAL DECODER/DRIVER

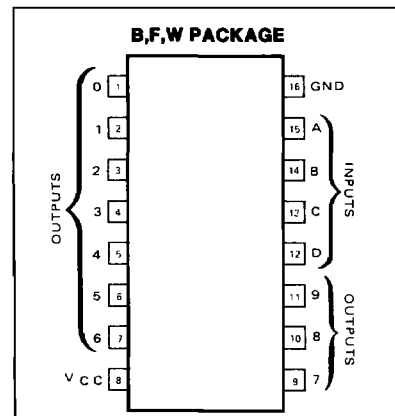
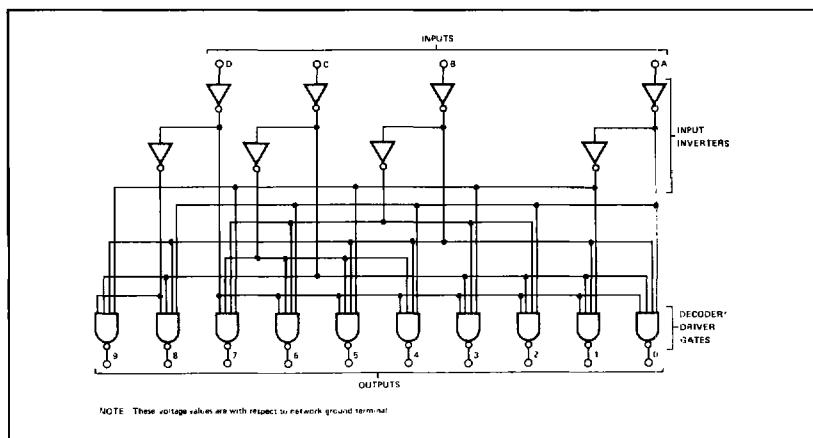
54/7445

SPEED/PACKAGE AVAILABILITY

54 F,W, 74 B,F

PIN CONFIGURATION

BLOCK DIAGRAM

SWITCHING CHARACTERISTICS $V_{CC}=5V$, $T_A=25^\circ C$

TEST CONDITIONS	54/74			
	$C_L = 15\text{pF}$ $R_L = 100\Omega$			
PARAMETER	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high			50	ns
t_{PHL} High-to-low			50	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE-INPUTS

D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

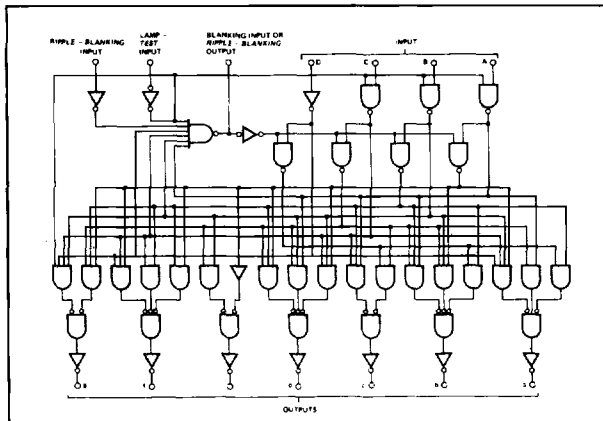
TRUTH TABLE-OUTPUTS

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

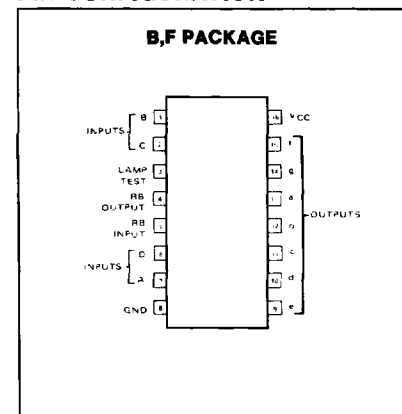
SPEED/PACKAGE AVAILABILITY

54 F 74 B,F

BLOCK DIAGRAM



PIN CONFIGURATION

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25^\circ C$

TEST CONDITIONS			54/74			
			$C_L = 15\text{pF}$ $R_L = 120\Omega$			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high	A,RBI	Any			100	ns
t_{PHL} High-to-low	A or RBI				100	

Load circuit and typical waveforms are shown at the front of section.

10G10

TRUTH TABLE

74181 8-BIT ALU															
INPUTS							OUTPUTS								
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	B1/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	x	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	x	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	x	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	x	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	x	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	x	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	x	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	x	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	x	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	x	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	x	1	0	1	1	1	1	0	0	1	1	0	0	
12	1	x	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	x	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	x	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	x	1	1	1	1	1	1	1	1	1	1	1	1	
BI	x	x	x	x	x	x	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	x	x	x	x	x	1	0	0	0	0	0	0	0	4

NOTES:

- BI/BRO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = Input may be high or low.
- When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.
- When ripple-blanking input (RBI) is at a logical 0 and A = B = C = D = logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).
- When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 0.

SPEED/PACKAGE AVAILABILITY

54 F

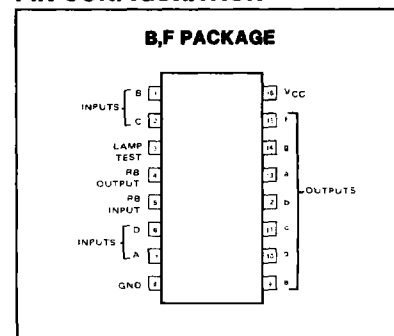
74 B,F

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25^\circ C$

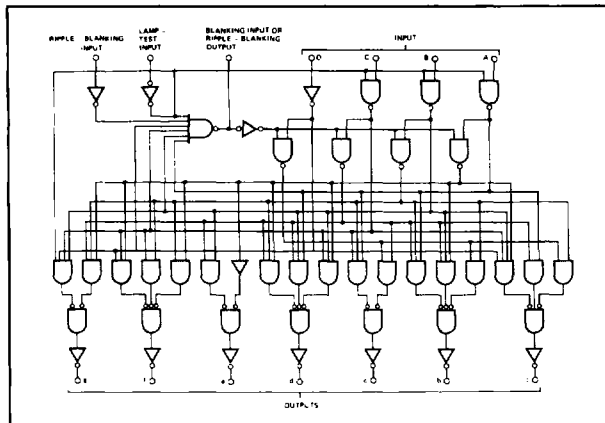
TEST CONDITIONS			54/74			
			$C_L = 15pF$ $R_L = 120\Omega$			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time						
t_{PLH} Low-to-high	A,RBI	Any			100	ns
t_{PHL} High-to-low					100	ns

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION



LOGIC DIAGRAM



TRUTH TABLE

INPUTS							OUTPUTS								
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	x	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	x	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	x	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	x	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	x	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	x	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	x	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	x	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	x	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	x	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	x	1	0	1	1	1	1	1	0	0	1	1	0	
12	1	x	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	x	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	x	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	x	1	1	1	1	1	1	1	1	1	1	1	1	
BI	x	x	x	x	x	x	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	x	x	x	x	x	1	0	0	0	0	0	0	0	4

NOTES:

1. BI/RBO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.
2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) is at a logical 0 and A = B = C = D = logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 0.

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