Integrated Circuit Systems, Inc.

ICS87949
LOW SKEW ÷1, ÷2 CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS87949 is a low skew, ÷1, ÷2 Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87949 has selectable single ended clock or LVPECL clock inputs. The single ended clock input accepts LVCMOS or LVTTL input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 15 to 30 by utilizing the ability of the outputs to drive two series terminated lines.

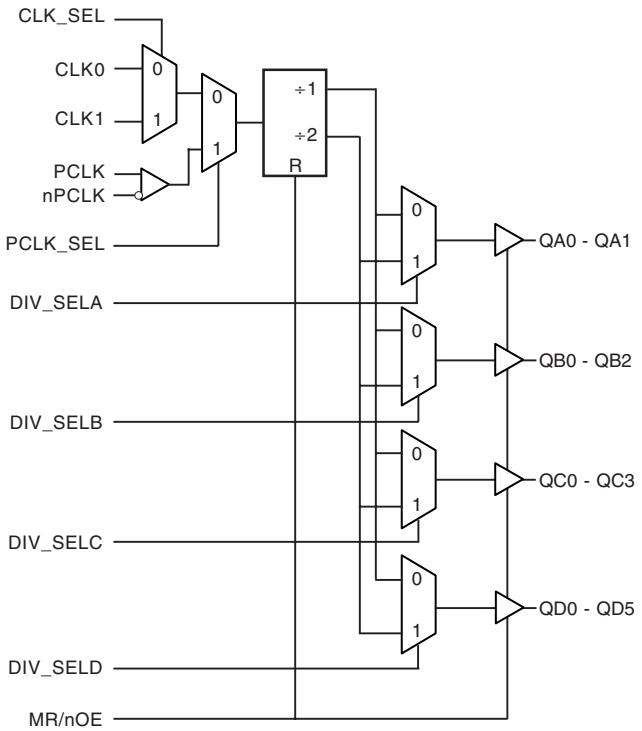
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset input, MR/nOE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The ICS87949 is characterized at 3.3V core/3.3V output. Guaranteed output and part-to-part skew characteristics make the ICS87949 ideal for those clock distribution applications demanding well defined performance and repeatability.

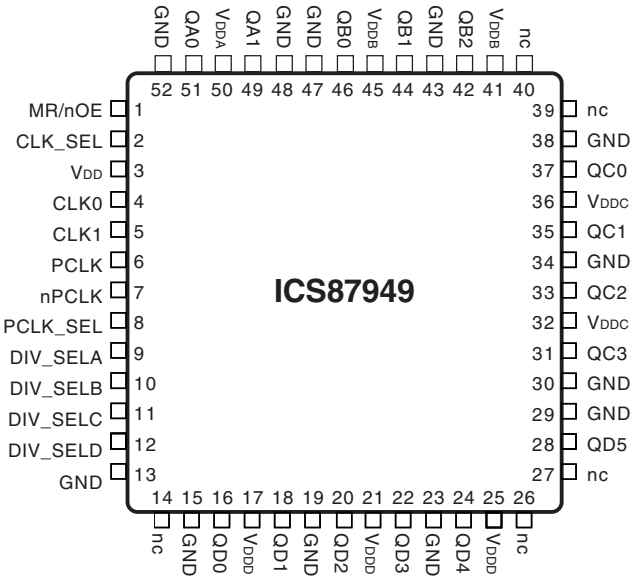
FEATURES

- 15 single ended LVCMOS outputs, 7Ω typical output impedance
- Selectable LVCMOS or LVPECL clock inputs
- CLK0 and CLK1 can accept the following input levels: LVCMOS and LVTTL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum input frequency: 250MHz
- Output skew: 350ps (maximum)
- Part-to-part skew: 2.75ns (maximum)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Pin compatible to the MPC949

BLOCK DIAGRAM



PIN ASSIGNMENT



52-Lead LQFP
10mm x 10mm x 1.4mm package body
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	MR/nOE	Input	Pulldown	Master reset and output enable. Resets outputs to tristate. Enables and disables all outputs. LVCMOS interface levels.
2	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1. When LOW, selects CLK0. LVCMOS / LVTTL interface levels.
3	V_{DD}	Power		Positive supply pin. Connect to 3.3V.
4, 5	CLK0, CLK1	Input	Pullup	LVCMOS / LVTTL clock inputs.
6	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
8	PCLK_SEL	Input	Pulldown	PCLK select input.
9	DIV_SELA	Input	Pulldown	Controls frequency division for Bank A outputs. LVCMOS interface levels.
10	DIV_SELB	Input	Pulldown	Controls frequency division for Bank B outputs. LVCMOS interface levels.
11	DIV_SELC	Input	Pulldown	Controls frequency division for Bank C outputs. LVCMOS interface levels.
12	DIV_SELD	Input	Pulldown	Controls frequency division for Bank D outputs. LVCMOS interface levels.
13, 15, 19, 23, 29, 30, 34, 38, 43, 47, 48, 52	GND	Power		Power supply ground. Connect to ground.
14, 26, 27, 39, 40	nc	Unused		No connect.
16, 18, 20, 22, 24, 28	QD0, QD1, QD2, QD3, QD4, QD5	Output		Bank D outputs. LVCMOS interface levels. 7Ω typical output impedance.
17, 21, 25	V_{DDD}	Power		Positive supply pins for Bank D outputs. Connect to 3.3V.
31, 33, 35, 37	QC3, QC2, QC1, QC0	Output		Bank C outputs. LVCMOS interface levels. 7Ω typical output impedance.
32, 36	V_{DDC}	Power		Positive supply pins for Bank C outputs. Connect to 3.3V.
41, 45	V_{DDB}	Power		Positive supply pins for Bank B outputs. Connect to 3.3V.
42, 44, 46	QB2, QB1, QB0	Output		Bank B outputs. LVCMOS interface levels. 7Ω typical output impedance.
49, 51	QA1, QA0	Output		Bank A outputs. LVCMOS interface levels. 7Ω typical output impedance.
50	V_{DDA}	Power		Positive supply pins for Bank A outputs. Connect to 3.3V.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, *V_{DDx} = 3.6V		TBD		pF
R_{OUT}	Output Impedance			7		Ω

*NOTE: V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}, V_{DDD}.

TABLE 3. FUNCTION TABLE

Inputs					Outputs			
MR/nOE	DIV_SELA	DIV_SELB	DIV_SELC	DIV_SELD	QA0 - QA1	QB0 - QB2	QC0 - QC3	QD0 - QD5
1	X	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z
0	0	X	X	X	fIN/1	Active	Active	Active
0	1	X	X	X	fIN/2	Active	Active	Active
0	X	0	X	X	Active	fIN/1	Active	Active
0	X	1	X	X	Active	fIN/2	Active	Active
0	X	X	0	X	Active	Active	fIN/1	Active
0	X	X	1	X	Active	Active	fIN/2	Active
0	X	X	X	0	Active	Active	Active	fIN/1
0	X	X	X	1	Active	Active	Active	fIN/2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	42.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDx}$ = 3.3V±0.3V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
*V_{DDx}	Output Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Core Supply Current			50		mA
**I_{DDx}	Output Supply Current			12		mA

*V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}, V_{DDD}.
**I_{DDx} denotes I_{DDA}, I_{DDB}, I_{DDC}, I_{DDD}.

TABLE 4B. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDx}$ = 3.3V±0.3V, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE		2		V_{DD} + 0.3	V
		CLK0, CLK1		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE		-0.3		0.8	V
		CLK0, CLK1		-0.3		1.3	V
I_{IH}	Input High Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE	*V_{DDx} = V_{IN} = 3.6V			150	µA
		CLK0, CLK1	*V_{DDx} = V_{IN} = 3.6V			5	µA
I_{IL}	Input Low Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE	*V_{DDx} = 3.6V, V_{IN} = 0V	-5			µA
		CLK0, CLK1	*V_{DDx} = 3.6V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage		I_{OH} = -20mA	2.5			V
V_{OL}	Output Low Voltage		I_{OL} = 20mA			0.4	V
I_{OZL}	Output Tristate Current Low					TBD	V
I_{OZH}	Output Tristate Current High					TBD	V

*NOTE: V_{DDx} denotes V_{DD}, V_{DDA}, V_{DDB}, V_{DDC}, V_{DDD}.

TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{DD} = V_{DDx} = 3.3V \pm 0.3V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	$*V_{DDx} = V_{IN} = 3.6V$			150	µA
		nPCLK	$*V_{DDx} = V_{IN} = 3.6V$			5	µA
I_{IL}	Input Low Current	PCLK	$*V_{DDx} = 3.6V$, $V_{IN} = 0V$	-5			µA
		nPCLK	$*V_{DDx} = 3.6V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.5		V_{DD}	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{DD} + 0.3V.
NOTE: $*V_{DDx}$ denotes V_{DD}, V_{DDA}, V_{DDB}, V_{DDC}, V_{DDD}.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDx} = 3.3V \pm 0.3V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1			3.5		ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1			3.5		ns
*t*sk(o)	Output Skew; NOTE 2, 5	Measured on rising edge at $V_{DDx}/2$			350	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5	Measured on rising edge at $V_{DDx}/2$			2.75	ns
t_R	Output Rise Time; NOTE 4	0.8 to 2.0V	.1		1.0	ns
t_F	Output Fall Time; NOTE 4	0.8 to 2.0V	.1		1.0	ns
t_{EN}	Output Enable Time;NOTE 4				11	ns
t_{DIS}	Output Disable Time;NOTE 4				11	ns

NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDx}/2$ of the output.
NOTE 2: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDx}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDx}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

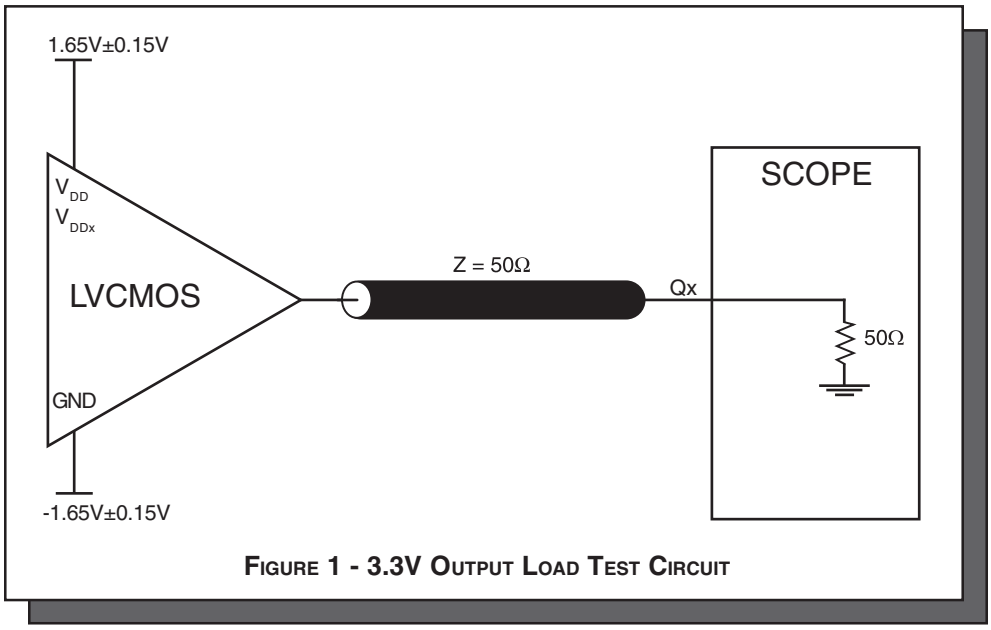


FIGURE 1 - 3.3V OUTPUT LOAD TEST CIRCUIT

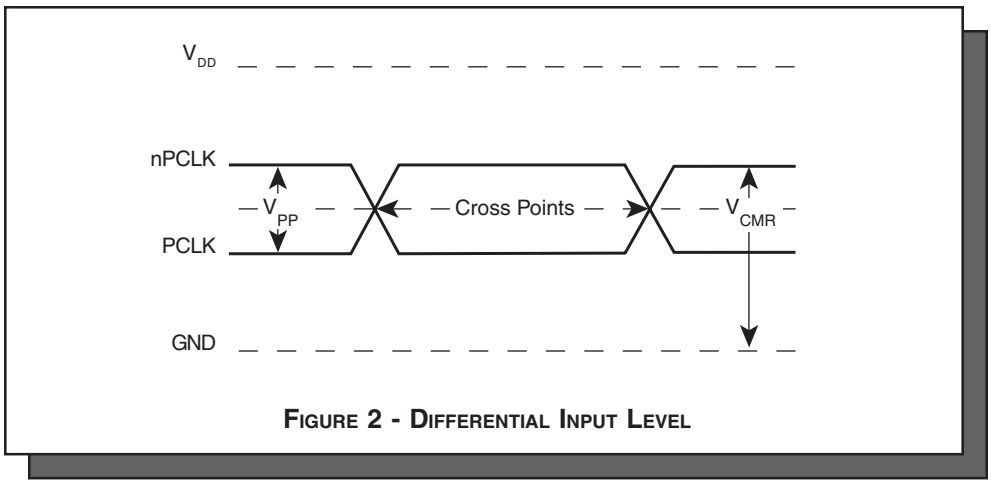


FIGURE 2 - DIFFERENTIAL INPUT LEVEL

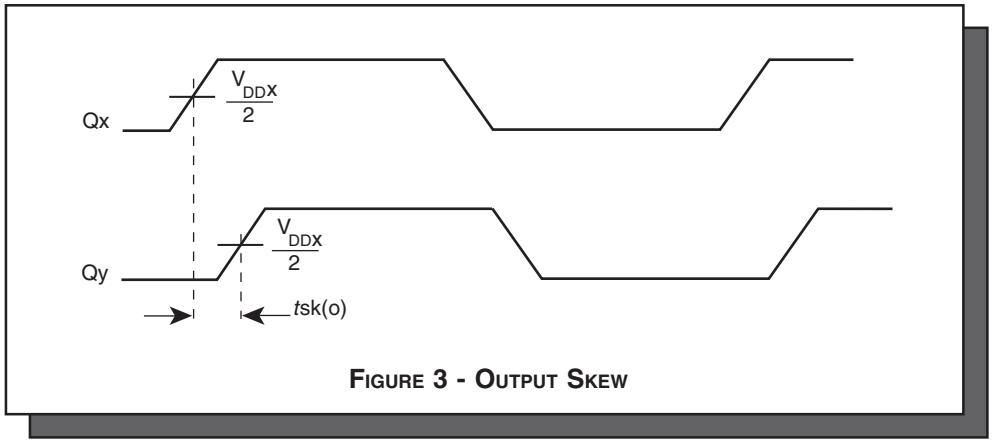


FIGURE 3 - OUTPUT SKEW

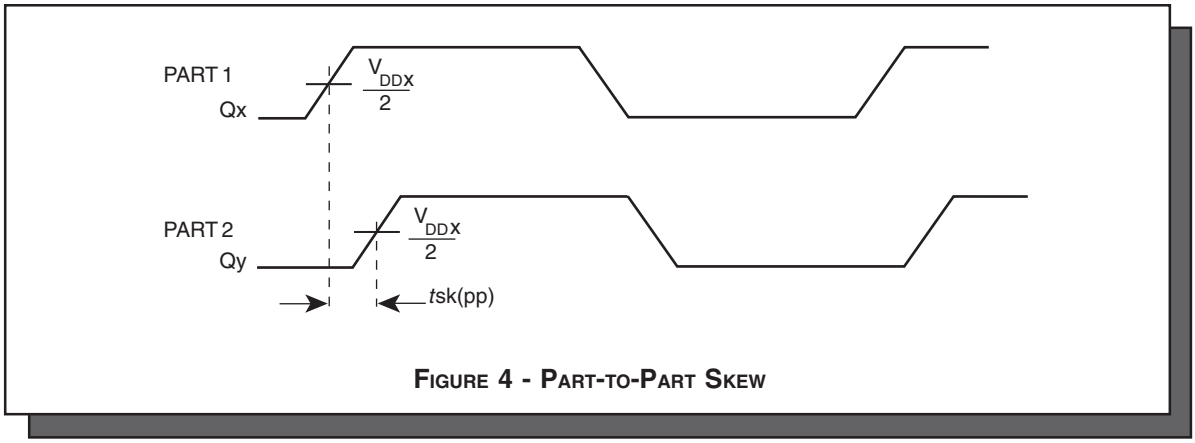


FIGURE 4 - PART-TO-PART SKEW

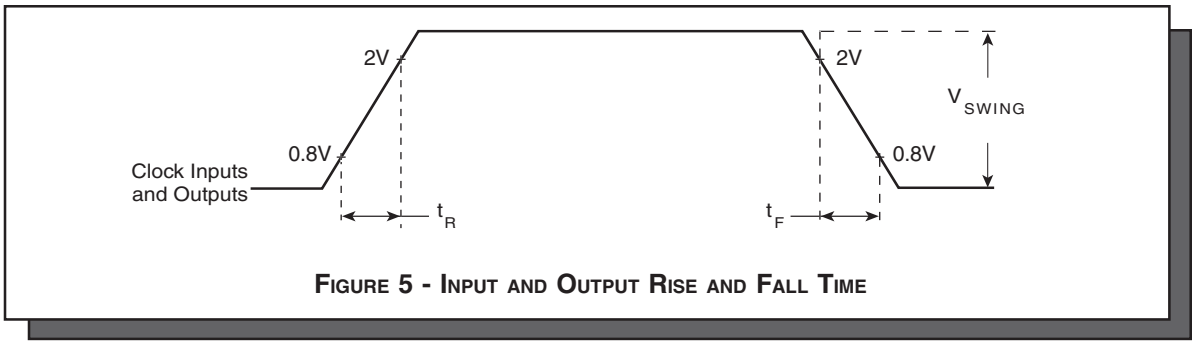


FIGURE 5 - INPUT AND OUTPUT RISE AND FALL TIME

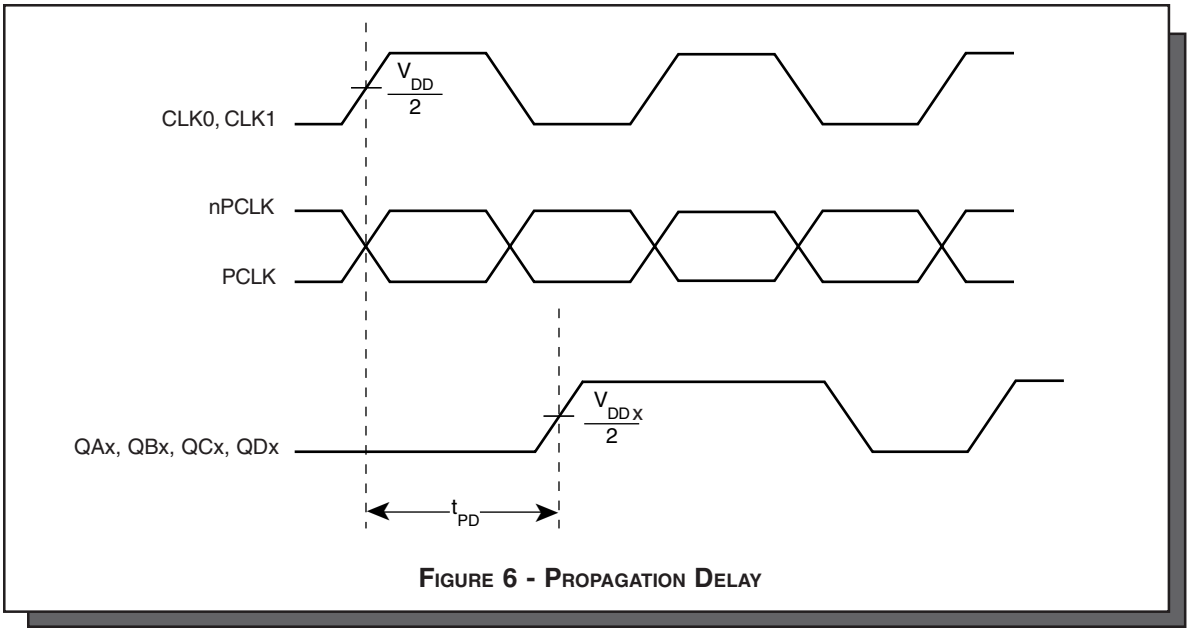


FIGURE 6 - PROPAGATION DELAY

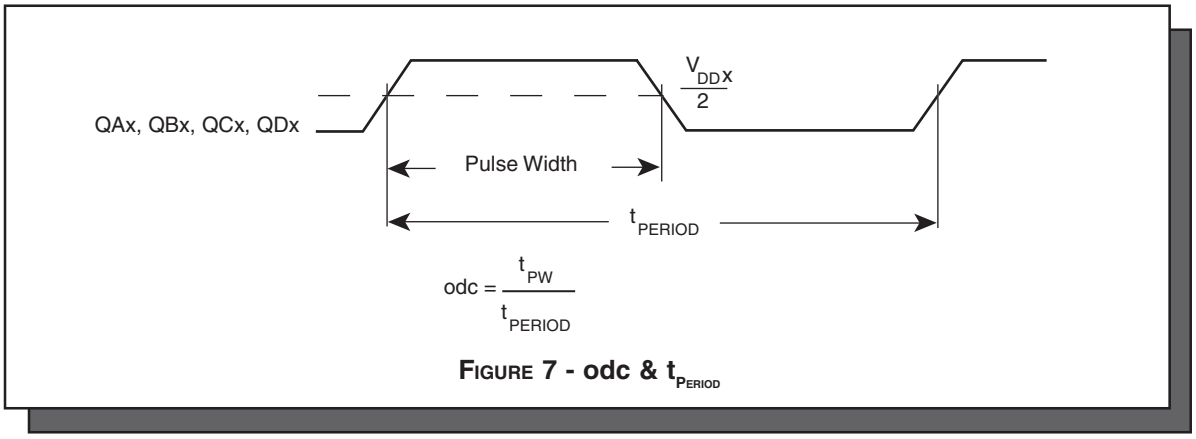


FIGURE 7 - odc & t_{PERIOD}

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87949 is: 1545

PACKAGE OUTLINE - Y SUFFIX

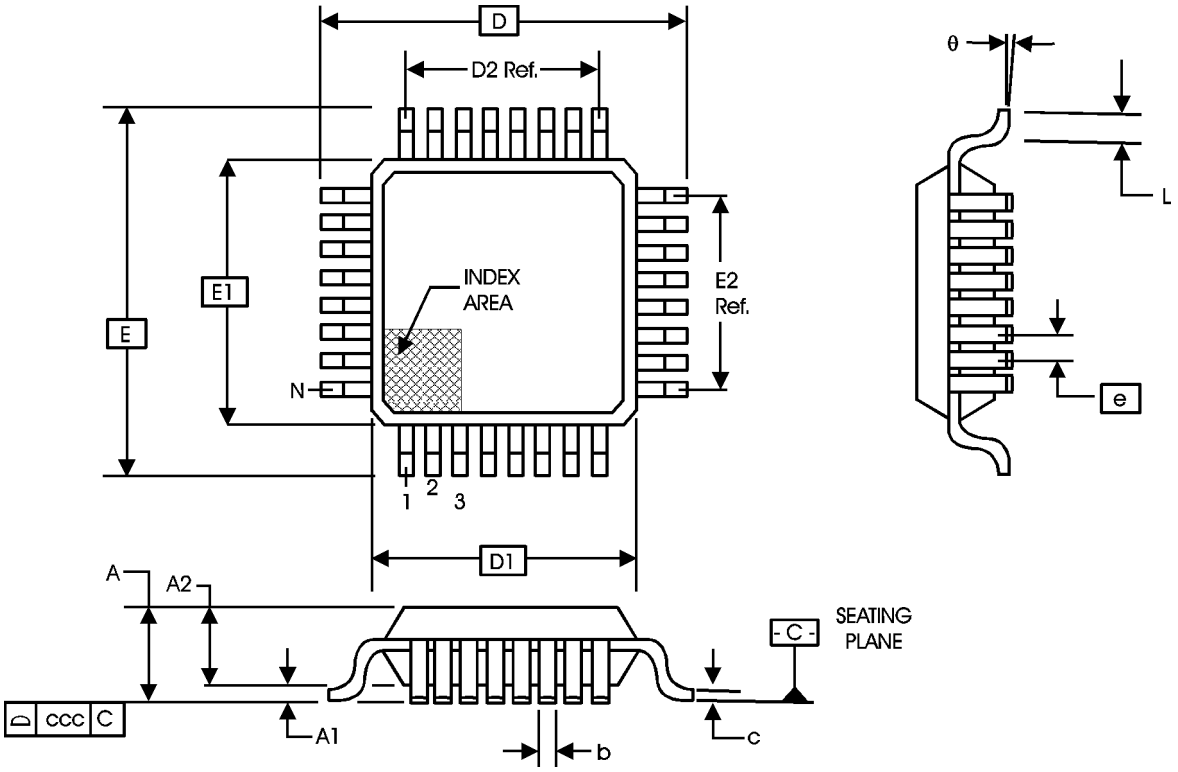


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N		52	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
b1	0.22	0.30	0.33
D		12.00 BASIC	
D1		10.00 BASIC	
E		12.00 BASIC	
E1		10.00 BASIC	
e		0.65 BASIC	
ccc	0.45	--	0.10
ddd	--	--	0.13

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87949AY	ICS87949AY	52 Lead LQFP	160 per tray	0°C to 70°C
ICS87949AYT	ICS87949AY	52 Lead LQFP on Tape and Reel	500	0°C to 70°C

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