National Semiconductor

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FGA Series ASPECT™ ECL Gate Arrays

General Description

The FGA Series is a new generation of ECL gate arrays based on National's ASPECT process. These advanced ECL gate arrays, ranging from 200 to over 30,000 equivalent gates, offer typical internal propagation delays of 150 ps and consume thirty percent less power than conventional ECL arrays. (Refer to Table I.)

With system clock frequencies up to 1.2 GHz, the speed domain of Gallium Arsenide, FGA Series gate arrays are especially well-suited for such high-performance applications as mainframe and supermini computers, fiber-optic communications, and many military and aerospace systems.

With only internal cells and I/O cells, FGA Series arrays are easy to use. Designers can implement logic using two-level or three-level series gating circuit structures within an array, with no complex signal mixing rules required. An extensive macro library, common to all FGA Series arrays, contains more than eighty SSI/MSI logic functions and 36 supporting I/O macros. In addition, internal macros may be grouped to form re-usable "soft macros" with even greater functional complexity.

All FGA Series gate arrays feature CAD-programmable speed/power options that allow the designer to maximize performance by individually assigning the switching speed and output drive currents for each internal macro. The speed/power feature provides maximum ECL speed where needed, yet allows overall chip power to remain at air-coolable levels. On-chip termination to −2V for the internal output emitter followers further reduces power consumption.

All FGA Series products interface with ECL 100K, ECL 10K and ECL 10KH components, and, except for the FGA200, FGA14000, FGA14040R, and FGA30000, are fully FAST®/TTL compatible. The TTL interface eliminates requirements for separate off-chip signal converters in mixed logic level systems, thereby resulting in reduced board space and cost, as well as avoiding the performance and reliability penalties associated with off-chip signal converters.

In addition to providing superior speed/power performance with high density, the ASPECT process is scalable to submicron dimensions. FGA Series arrays are designed to accommodate multiple ASPECT process generations to allow designs implemented today to migrate to tomorrow's arrays based on future ASPECT processes.

Features

- New generation ECL gate arrays with complexity to 30,000 equivalent logic gates
- Manufactured with 1.5-micron ASPECT process
- CAD-programmable speed/power options
- 150 ps typical internal delay
- Flexible array architecture with only two cell types: Internal cells and I/O cells
- F100K, 10K or 10KH ECL-compatible I/Os
- Mixable ECL/TTL I/Os
- Allows large number of simultaneously switching outputs

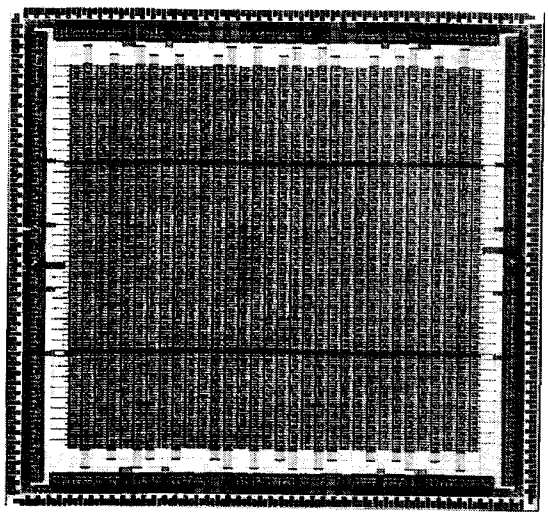

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FIGURE 1. FGA Series Gate Array

Note 1: FGA150, 600, 1300, 4000 and 15000 offer mixable ECL/TTL I/Os.

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temp. (T_J)	+150°C
Case Temp. under Bias (T_C)	−55°C to +125°C
V_{EE} Pin Potential to V_{CC} Pins (V_{MAX})	−7.0V to +0.5V
Input Voltage (DC) (V_I)	V_{EE} to (V_{CC} + 0.5V)
Output Current (DC Output HIGH) (I_O)	−50 mA
Operating Range ECL (V_{EE})	−5.7V to −4.2V
Operating Range TTL (V_{TTL})	4.5V to 5.5V

Note: Stresses greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Specifications

All FGA Series gate arrays operate from a standard ECL power supply and an additional −2V supply (V_{TT}) which terminates internal cell emitter followers to reduce power consumption. With F100K inputs and outputs, the FGA series is designed to operate from a standard 100K power supply, although a standard 10K power supply may be used instead. When used for mixed ECL/TTL operations, an additional power supply is required. The following table provides the power requirements for each allowable interface configuration.

Power Supply Requirements

I/O	V_{CC} (V)	V_{TT} (V)(Note 2)	V_{EE} (V)	V_{TTL} (V)	Arrays
F100K	GND	−1.9 to −2.1	−4.2 to −5.7	—	All
F10K	GND	−1.9 to −2.1	−4.7 to −5.7	—	
F100K/TTL	GND	−1.9 to −2.1	−4.2 to −5.7	4.5 to 5.5	Except FGA200, FGA14000, FGA14040R and FGA 30000
F10K/TTL	GND	−1.9 to −2.1	−4.7 to −5.7	4.5 to 5.5	
Pseudo TTL	V_{TTL}	(V_{TTL} −2) ±0.1	GND	4.75 to 5.25	

F100K ECL DC Characteristics

V_{EE} = −4.5V, V_{TT} = −2V, V_{CC} = V_{CCA} = GND, T_J = −10°C to +125°C (Note 3)

Symbol	Parameter	Conditions (Note 4)		Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{IN} = $V_{IH\ (max)}$	Loaded with 50Ω to −2.0V	−1035	−955	−870	mV
V_{OL}	Output LOW Voltage	or $V_{IL\ (min)}$		−1830	−1705	−1605	mV
V_{IH} (Note 5)	Input HIGH Voltage	Guaranteed HIGH Signal for All Inputs		−1125		−880	mV
V_{IL} (Note 5)	Input LOW Voltage	Guaranteed LOW Signal for All Inputs		−1810		−1605	mV

Note 1: Unless otherwise specified contractually.

Note 2: For internal cell output emitter follower termination to save power.

Note 3: Equilibrium temperature

Note 4: Conditions for testing are chosen to guarantee operation under worst case conditions.

Note 5: Forcing one input at a time. Apply $V_{IH\ (max)}$ or $V_{IL\ (min)}$ to all other inputs.

F10K ECL DC Characteristics $V_{EE} = -5.2V, V_{TT} = -2V, V_{CC} = V_{CCA} = GND$

Parameter	Conditions	Junction Temperature				Units
		0°C	25°C	65°C	125°C	
V_{OH} Max	$V_{IH} = V_{IH}$ Max, $V_{IL} = V_{IL}$ Min	−897	−862	−810	−732	mV
V_{OH} Min		−1112	−1077	−1025	−947	mV
V_{OL} Max		−1656	−1644	−1620	−1584	mV
V_{OL} Min		−1920	−1920	−1920	−1920	mV
V_{IH} Max (Note 1)		−888	−858	−810	−738	mV
V_{IL} Min (Note 1)		−1920	−1920	−1920	−1920	mV
V_{IHA} Min (Note 1)		−1209	−1172	−1125	−1045	mV
V_{ILA} Max (Note 1)		−1604	−1567	−1520	−1440	mV

TTL DC Characteristics over Operating Temperature Range

$V_{CC} = 5V \pm 5\%, T_J = -10°C$ to $+125°C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	$V_{CC} = 4.75V$	2.7	3.0	—	V
V_{OL}	Output LOW Voltage	$I_{OH} = 8.0$ mA/20 mA	$V_{CC} = 4.75V$	—	0.25	0.5	V
V_{IH}	Input HIGH Voltage			2.0	—	—	V
V_{IL}	Input LOW Voltage			—	—	0.80	V
I_{IH}	Input HIGH Current (Note 2)	$V_{CC} = 5.25V, V_{IN} = 2.4V$		—	—	40	μA
I_{IL}	Input LOW Current (Note 2)	$V_{CC} = 5.25V, V_{IN} = 0.4V$		—	—	−400	μA
I_{OZH}	Output OFF Current HIGH	$V_{CC} = 5.25V, V_{OUT} = 2.4V$		—	—	40	μA
I_{OZL}	Output OFF Current LOW	$V_{CC} = 5.25V, V_{OUT} = 0.4V$		—	—	−40	μA
I_{OS}	Output Off Short Circuit Current (Note 3)	8/20 mA Driver	$V_{CC} = 5.25V$, $V_{OUT} = 0$	−15	—	−130	mA

Note 1: Forcing one input at a time. Apply V_{IH} (max) or V_{IL} (min) to all other inputs.

Note 2: Current per input.

Note 3: Not more than one output should be shorted at a time. Output should not be shorted for more than one second.

FGA Series ECL Gate Array Family

TABLE I. The FGA Gate Array Series

Description	FGA0150	FGA0200	FGA0600	FGA1300	FGA4000	FGA14000	FGA14040R	FGA15000	FGA30000
Equivalent Gates	269	269	792	1642	4704	16709	7853 + 4.6K RAM	16644	28486
Internal Cells (MAU)	75	75	240	528	1600	5904	2624 Plus RAM	5920	10266
Internal Gate Delay	150PS	150PS	150PS	150PS	150PS	150PS	150PS	150PS	150PS
Speed/Power Options	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
100K/10K/10KH Compatible	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ECL/TTL Mixed I/O	22	0	36	72	128	0	0	220	0
ECL Only I/O	0	22	12	0	0	256	256	0	256
Power/Ground	6	6	12	40	48	56	56	72	56
Typical Power (W)	0.5–1.0	0.5–1.0	0.5–1.5	1–3	3–6	10–20	10–20	10–20	15–30
Standard Packages	16, 24 Metal Flat 28 PLCC/LDCC	16, 24 Metal Flat 28 PLCC/LDCC	44LDCC 75PGA	109PGA 116LDCC 75PGA*	173PGA 172LDCC 99PGA**	323PGA	323PGA	303PGA	323PGA
Available	Now	Now	Now	Now	Now	Now	Now	Now	1Q90

*Maximum of 48 I/O

**Maximum of 64 I/O

ASPECT Process

FGA Series arrays use a National proprietary process called ASPECT which uses conservative 1.5-micron design rules to achieve VLSI density and 150 ps typical internal gate delays at thirty percent of conventional ECL power consumption levels.

ASPECT is the first bipolar process to use polysilicon for emitter and base structures. Polysilicide serves as a source of impurities for both the emitter and the base. This permits the fabrication of extremely shallow (500Å below the surface) emitters and narrow base regions. The combination of shallow emitters and base leads to transistors with a very high switching speed. ASPECT also uses polysilicon resistors.

Such resistors exhibit low junction capacitance, making them ideal passive elements for high-speed logic circuits.

An important feature is the self-aligning process used in ASPECT gate arrays. This insensitivity to misalignment makes ASPECT a high-yield process and enables the move to smaller geometries with less difficulty than conventional bipolar processes.

Array Organization

Electrical components (transistors, resistors, diodes and capacitors) are organized into repeating structures called cells, Macros, which are the basic building blocks of gate array logic design, are built by interconnecting the components in one or more cells.

Array Organization (Continued)

The FGA Series employs only two cell types: internal cells and I/O cells. The internal cells are the workhorses of the array, where most of the circuit logic is implemented. All signals going to or coming from the outside world must exit or enter the array through an I/O cell. Since all signal level conversions are performed in the I/O cells, no signal mixing takes place within the array, thus simplifying the design effort. Cell types and their functions are described in greater detail in the following paragraphs.

The bonding pads are located around the periphery of the array. In addition to performing I/O functions, some of the pads are reserved for power and ground busses. Biasing occurs in dedicated routing channels and is optimally performed automatically by placement and routing CAD software.

All FGA Series arrays employ three-layer metalization for signals and bussing. The first metal layer connects components within macros and makes horizontal connections between macros. Layer two is primarily for vertical connections between macros, while layer three contains most of the power bussing. Future versions of the ASPECT process may include four metal layers. In that case, first-layer metal would not be needed to connect macros, thus eliminating routing channels and increasing gate counts for a given die size.

Internal Cell and Logic Complexity

The basic internal cell in an FGA Series array is called a "minimum addressable unit", or MAU. It is the smallest portion of the chip that a CAD system can access for placing or routing.

The number of elements in this minimum cell is actually smaller than on any competing array. In fact, this small, compact cell structure, said to have a fine granularity, increases efficiency. In general, the larger the cell, the greater the likelihood that some cell resources go unused, thereby decreasing efficiency.

Single-level, two-level, and three-level series gated ECL structures are used in FGA Series arrays to implement various logic functions. Series gating allows complex logic functions to be implemented with fewer gates while maintaining optimum performance. Additional logic complexity at no cost in cell utilization may be gained in internal cells by connecting the outputs together (emitter dotting) to form wired-OR functions.

Speed/power options can be used to assign the current settings in each internal cell macro. This feature allows the designer to maximize speed when needed, yet minimize the power consumption. The termination of internal output emitter followers to a $-2V$ internal bus further reduces power consumption.

Typically, internal cell utilization of eighty-five percent is considered optimum. Designs can be completed with up to one-hundred percent utilization; however placement and routing at this level sometimes requires special interactive layout.

The FGA Macro Library contains a number of physical macros with MSI-level complexity. The final portion of this data sheet includes a representative sample of macros included in the FGA Series Macro Library. Full documentation for all macros, including specifications, can be found in the FGA Series Macro Library Reference Manual.

I/O and Interface Capabilities

I/O cells in the FGA Series are capable of performing input, output, transceiver logic and ECL/TTL conversion functions. The array's I/O organization is flexible, with each signal pad supported by a dedicated I/O cell. An incoming signal can enter the internal array through any I/O cell and, after completing the logic implementation, can then exit the array through any I/O cell without restriction.

The flexible functionality of individual I/O cells can be especially useful in system applications requiring latched inputs and outputs. The ability of an FGA Series I/O cell to be

I/O and Interface Capabilities

(Continued)

configured as a latch saves having to use an internal cell for this function. In addition, although most ECL devices drive 50Ω loads, I/Os can be paired to drive 25Ω loads.

Each I/O cell offers a choice of signal termination options. For relatively short signal paths, designers may build series-terminated outputs, simplifying designs in systems where placing termination resistors on the board is not practical. To minimize noise, internal pull-down resistors are provided to keep unused inputs from floating.

Either F100K, 10K, or 10KH interface capability is available on all FGA Series arrays. All input thresholds and logic levels must uniformly belong to the same ECL family. Likewise, the output interface must be the same as that used for input. With the exception of the FGA0200, FGA14000, FGA14040R and FGA30000, each I/O can also be a mixable ECL/TTL I/O. This means that every I/O can be independently configured as either ECL or TTL. The TTL I/O is capable of producing totem-pole, open-collector, or three-state output levels. *Figure 2* illustrates the acceptable interface options for FGA Series arrays.

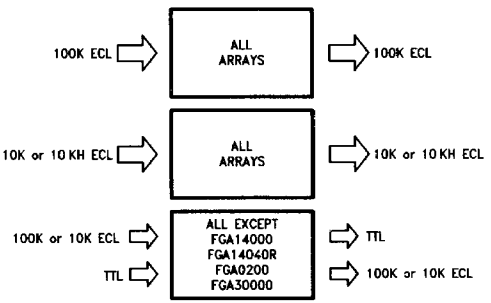

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FIGURE 2. Interface Capabilities

Embedded RAM

The embedded RAM block is a self-timing memory device with the capabilities of supporting various memory configurations, different bit select patterns, output power options, and different clock systems. The embedded RAM block contains 576 bits, and is organized as 64 words by 9 bits. There are 8 RAM blocks in the FGA14040R with the total of 4608 bits. Each embedded RAM block has its own built-in decoder and control circuit, thus improving system performance and reliability while saving board space. The embedded RAM has three modes of operation, Normal mode, Scan mode and Test mode. At high power operation, the typical access time is 3.75 ns and the worst case access time is 5 ns. Two output drive options, 0.6 mA and 1.2 mA, are available to support the driving capabilities of the embedded RAM. Note that the memory is called self-timed memory device because it generates and shapes its own write strobe internally. This pulse is generated off of the rising edge of the clock which is applied to the embedded RAM.

Speed/Power Options

Speed/power options are a feature of all FGA Series gate arrays. This feature allows the designer to maximize speed where needed, yet minimize overall chip power consumption.

Two sets of macros are available for each logic function in the FGA arrays, the standard macros and the double macros (see Table IV). The double macros use two times as much current as standard macros, and are designed for use in the critical circuitry. These two macro types can be used interchangeably within the same chip.

Essentially, speed/power options are used to assign one or two current values (high = 0.3 mA, low = 0.15 mA) to the current source which controls switching speed; and one of two current values (high = 0.6 mA, low = 0.3 mA) to the true and complement outputs for output drive currents. The latter setting permits zero power consumption for unused outputs. *Figure 3* illustrates circuit options for each of the three settings.

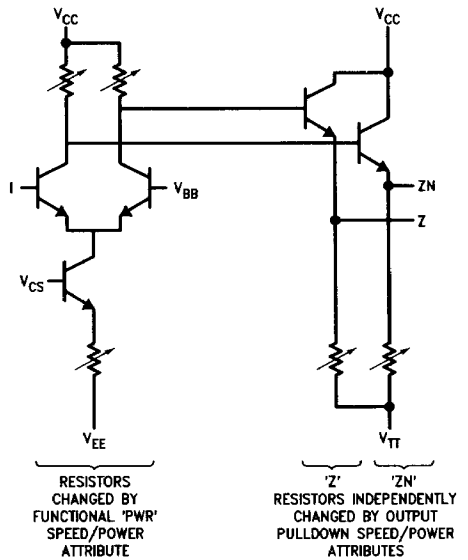

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FIGURE 3. Speed/Power Options

The speed/power options are assigned during schematic capture. Default values for each setting may be specified during schematic capture as well. Designers may use the speed/power options to fine tune the design after placement and routing simply by returning to schematic capture and reassigning values without having to repeat placement and routing.

The examples in Table III illustrate how speed/power options can affect propagation delay vs. power consumption at the macro level. Additional speed/power tradeoffs are listed in "Macro Performance Examples" later in this data sheet.

Speed/Power Options (Continued)

TABLE III. Macro Speed/Power Tradeoffs

Macro		Speed (ps)	Power (mW)
2-Input NOR ORN02	High	235	2.5
	Low	410	1.2
D Flip-Flop DFI01	High	415	7.5
	Low	680	5.6

TABLE IV. Current Setting of Speed/Power Options

Current μA	Standard Macro (S)		Double Macros (D)	
	High Speed	Low Power	High Speed	Low Power
Source Current	300	150	600	300
OEF Current	600	300	600	300

AC Specifications

FGA Series macro propagation delays are specified as MIN, TYP, and MAX values, with variations due to process, power supply and temperature, as shown in the "AC Performance Variations" table.

Macro Performance Examples

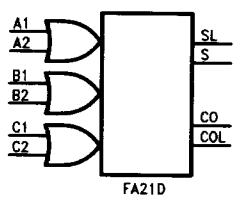
The following pages contain performance specifications for some important internal cell macros. Complete information, including design rules and application notes, can be found in the FGA Series Design Manual and FGA Series Macro Library.

AC Performance Variations

Variation Type	Derating from Typical (%) (Note 2)	
	Minimum (Note 1)	Maximum (Note 3)
Temperature	−10	15
Voltage	~0	~0
Process	−20	20
Total	−30%	35%

Note 1: Minimum: T_J = 0°C, V_{EE} = −4.8V, Best Case Process
Note 2: Typical: T_J = 25°C, V_{EE} = −4.5V, Normal Process
Note 3: Maximum: T_J = 125°C, V_{EE} = −4.2V, Worst Case Process

FA21D One Bit Full Adder with Gates Inputs



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Propagation Delay (units in ps)

From Inputs	To Output	High Power			Low Power		
		Min	Typ	Max	Min	Typ	Max
A1, A2	S ↗	330	410	550	420	530	710
A1, A2	S ↘	380	470	640	420	530	710
B1, B2	S ↗	380	470	640	470	580	790
B1, B2	S ↘	450	560	760	490	620	830
C1, C2	S ↗	200	250	340	200	250	340
C1, C2	S ↘	240	300	400	280	350	480
A1, A2	C0 ↗	190	230	310	190	240	330
A1, A2	C0 ↘	190	240	330	290	360	490
B1, B2	C0 ↗	240	300	400	260	330	450
B1, B2	C0 ↘	260	330	450	380	470	640
C1, C2	C0 ↗	240	300	400	260	330	450
C1, C2	C0 ↘	260	330	450	380	470	640

Macro Performance Examples (Continued)

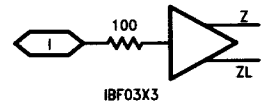
Current in Base Macro

Power ATT	Min	Typ	Max
IEE (mA)			
HIGH	1.36	1.80	2.26
LOW	0.92	1.20	1.52
ITT (mA)			
HIGH	0.21	0.30	0.39
LOW	0.21	0.30	0.39

Current in Macro Outputs

Power ATT	Min	Typ	Max
ITT (mA)			
HIGH	0.42	0.60	0.78
LOW	0.21	0.30	0.39

IBF03X2(3) Input Buffer



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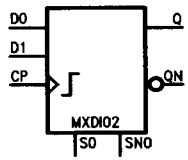
Propagation Delay (units in ps)

From Input	To Outputs	Min	Typ	Max
I	Z, ZL ↗	220	280	380
I	Z, ZL ↘	220	280	380

Current in Base Macro

Min	Typ	Max
IEE (mA)		
0.60	0.80	1.0
ITT (mA)		
0.84	1.20	1.56

MXDI02—D Flip Flop with Multiplexed Data Inputs



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Propagation Delay (units in ps)

From Input	To Output	High Power			Low Power		
		Min	Typ	Max	Min	Typ	Max
CP	Q ↗	340	420	570	530	660	890
CP	Q ↘	300	380	510	530	660	890
CP	QN ↗	340	430	580	540	670	910
CP	QN ↘	310	390	530	540	680	920

Current in Base Macro

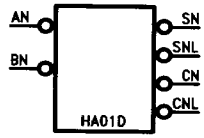
Power ATT	Min	Typ	Max
IEE (mA)			
HIGH	0.92	1.20	1.52
LOW	0.68	0.90	1.14
ITT (mA)			
HIGH	0.84	1.20	1.56
LOW	0.84	1.20	1.56

Current in Macro Outputs

Power ATT	Min	Typ	Max
ITT (mA)			
HIGH	0.42	0.60	0.78
LOW	0.21	0.30	0.39

Macro Performance Examples (Continued)

HA01D—Half Adder



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Propagation Delay (units in ps)

From Inputs	To Output	High Power			Low Power		
		Min	Typ	Max	Min	Typ	Max
AN	SN ↗	160	200	270	160	200	270
AN	SN ↘	170	210	280	200	250	340
AN	CN ↗	150	190	250	140	180	240
AN	CN ↘	150	190	250	190	230	310
BN	SN ↗	200	250	340	190	240	330
BN	SN ↘	230	290	390	270	340	460
BN	CN ↗	200	250	340	200	250	340
BN	CN ↘	220	280	370	270	340	460

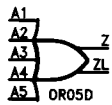
Current in Base Macro

Power ATT	Min	Typ	Max
IEE (mA)			
HIGH	0.68	0.90	1.13
LOW	0.46	0.60	0.76

Current in Macro Outputs

Power ATT	Min	Typ	Max
ITT (mA)			
HIGH	0.42	0.60	0.78
LOW	0.21	0.30	0.39

0R05D—5 Input OR Gate



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Propagation Delay (units in ps)

From Input	To Outputs	High Power			Low Power		
		Min	Typ	Max	Min	Typ	Max
A	Z, ZL ↗	160	200	270	180	230	310
A	Z, ZL ↘	160	200	270	200	250	340

Current in Base Macro

IEE (mA)

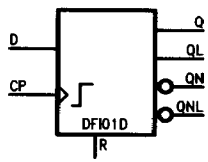
Power ATT	Min	Typ	Max
HIGH	0.45	0.60	0.75
LOW	0.23	0.30	0.38

Current in Macro Outputs

ITT (mA) for each macro output used:

Power ATT	Min	Typ	Max
HIGH	0.42	0.60	0.78
LOW	0.21	0.30	0.39

DFI01D—D Flip Flop with Reset



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Propagation Delay (units in ps)

From Inputs	To Output	High Power			Low Power		
		Min	Typ	Max	Min	Typ	Max
CP	Q ↗	340	420	570	500	620	840
CP	Q ↘	350	430	580	380	480	650
CP	QN ↗	310	390	530	400	500	680
CP	QN ↘	340	430	580	400	490	670
CP LOW							
R	Q ↘	300	380	510	550	680	920
R	QN ↗	350	430	590	490	610	820
CP HIGH							
R	Q ↘	370	460	620	560	710	950
R	QN ↗	370	460	630	520	650	880

Macro Performance Examples (Continued)

Current in Base Macro

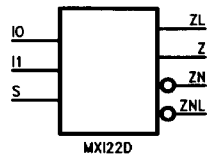
Power ATT	Min	Typ	Max
IEE (mA)			
HIGH	1.13	1.50	1.88
LOW	0.69	0.90	1.14
ITT (mA)			
HIGH	0.84	1.20	1.56
LOW	0.84	1.20	1.56

Current in Macro Outputs

Power ATT	Min	Typ	Max
ITT (mA)			
HIGH	0.42	0.60	0.78
LOW (Note 1)	0.21	0.30	0.39

Note 1: Output Q is hard wired to 0.6 mA current source and cannot be assigned power attributes.

MXI22D—2:1 Multiplexer



TL/U/10560–13

Propagation Delay (units in ps)

From Input	To Output	High Power			Low Power		
		Min	Typ	Max	Min	Typ	Max
I	Z ↗	170	210	280	190	230	310
I	Z ↘	170	210	280	230	290	390
I	ZN ↗	160	200	270	160	200	270
I	ZN ↘	170	210	280	200	250	340
S	Z ↗	240	300	400	320	400	540
S	Z ↘	240	300	400	320	400	540
S	ZN ↗	230	290	390	260	330	450
S	ZN ↘	230	290	390	260	330	450

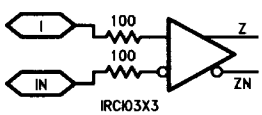
Current in Base Macro

Power ATT	Min	Typ	Max
IEE (mA)			
HIGH	0.68	0.90	1.13
LOW	0.46	0.60	0.76

Current in Macro Outputs

Power ATT	Min	Typ	Max
ITT (mA)			
HIGH	0.42	0.60	0.78
LOW	0.21	0.30	0.39

IRCI03X2 (3)—Differential Input Buffer



TL/U/10560–14

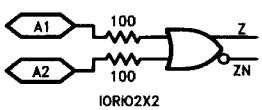
Propagation Delay (units in ps)

From Inputs	To Output	Min	Typ	Max
I, IN	Z ↗	120	150	210
I, IN	Z ↘	120	150	210
I, IN	ZN ↗	120	150	210
I, IN	ZN ↘	120	150	210

Current in Base Macro

Min	Typ	Max
IEE (mA)		
0.60	0.80	1.0
ITT (mA)		
0.84	1.20	1.56

I0RI02X2—2 Input OR/NOR Gate



TL/U/10560–15

Propagation Delay (units in ps)

From Input	To Outputs	Min	Typ	Max
A	Z ↗	190	240	320
A	Z ↘	180	230	310
A	ZN ↗	160	200	270
A	ZN ↘	200	250	340

Current in Base Macro

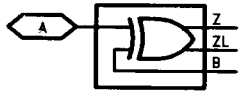
Min	Typ	Max
IEE (mA)		
0.60	0.80	1.0

Current in Macro Outputs

Min	Typ	Max
ITT (mA)		
0.84	1.20	1.56

Macro Performance Examples (Continued)

IXOR02X2—2 Input XOR Gate



IXOR02X2

TL/U/10560–16

Propagation Delay (units in ps)

From Input	To Outputs	Min	Typ	Max
A	Z, ZL ⌐	210	270	370
A	Z, ZL ⌙	190	240	320
A	Z, ZL ⌐	330	410	550
A	Z, ZL ⌙	300	380	510

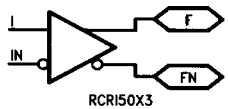
Current in Base Macro

Min	Typ	Max
IEE (mA)		
1.20	1.60	2.0

Current in Macro Outputs

Min	Typ	Max
ITT (mA)		
0.84	1.20	1.56

RCRI50X3—Differential Output Buffer



RCRI50X3

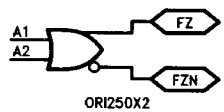
TL/U/10560–17

Propagation Delay (units in ps)

From Inputs	To Outputs	Min	Typ	Max
I, IN	FZ, FZN ⌐	400	470	640
I, IN	FZ, FZN ⌙	300	370	500

Current in Base Macro

Min	Typ	Max
IEE (mA)		
4.35	5.80	7.25



ORI250X2

TL/U/10560–18

Propagation Delay (units in ps)

From Input	To Output	Min	Typ	Max
A	FZ ⌐	290	360	490
A	FZ ⌙	290	360	490
A	FZN ⌐	280	350	470
A	FZN ⌙	290	360	490

Current in Base Macro

Min	Typ	Max
IEE (mA)		
4.95	6.60	8.25

Current in Macro Outputs

Min	Typ	Max
IVCCA (mA)		
23.8	28.0	32.2

Macro Cells Library

Internal Macros

Name	Function	Cells
BUFFERS, INVERTERS		
BF01	Buffer	1
BFI01	Buffer/Inverter	2
RCR01D	Differential Receiver/Buffer	1
RCR11D	Differential Receiver/Buffer	1
RCRI01	Differential Receiver/Buffer	2
RCRN01	Inverting Differential Receiver	1
GATES		
ANI02	2-Input AND/NAND	2
OAI23D	3-3 OR/AND—Invert	2
OAI23S	3-3 OR/AND—Invert, 1.2 mA Ioef	4
OAI24	4-4 OR/AND—Invert	2
OAI32DT	2-2-2 OR/AND—Invert	3
OAI44D	4-3-3-3 OR/AND—Invert	4
OAI44S	4-3-3-3 OR/AND—Invert	4
OAI46	5-4-5-6 OR/AND—Invert	5
OAI55DT	5-4-3-2-1 OR/AND—Invert	5
OAI66DT	6-6-4-4-2-2 OR/AND—Invert	7
OR02	2-Input OR	2
OR02D	2-Input OR	1
OR05	5-Input OR	1
OR05D	5-Input OR	1
ORI02	2-Input OR/NOR	2
ORI02D	2-Input OR/NOR	2
ORI02S	2-Input OR/NOR	4
ORI05	5-Input OR/NOR	2
ORI05D	5-Input OR/NOR	2
ORI05S	5-Input OR/NOR, 1.2 mA Ioef	4
ORI08	8-Input OR/NOR	2
ORI08D	8-Input OR/NOR	2
ORI012D	12-Input OR/NOR	3
ORN02	2-Input NOR	2
ORN02D	2-Input NOR	1
ORN05	5-Input NOR	1
ORN05D	5-Input NOR	1
2OR02D	Dual 2-Input OR, 0.6 mA Ioef	2
4OR02S	Quad 2-Input OR, 1.2 mA Ioef	4
XOR04	4-Input XOR	4
XOR09	9-Input XOR	8
XORI03DT	3-Input XOR/XNOR	3
XORI03ST	3-Input XOR/XNOR, 1.2 mA Ioef	4
XORI22D	Gated 2-Input XOR/XNOR	2
XORI22S	Gated 2-Input XOR/XNOR, 1.2 mA Ioef	4
XORI23	Gated 2-Input XOR/XNOR	2
XORN04D	4-Input XNOR	3
XORN04S	4-Input XNOR, 1.2 mA Ioef	5
XORN06DT	6-Input XNOR	5

Macro Cells Library (Continued)

Internal Macros (Continued)

Name	Function	Cells
DECODERS, MULTIPLEXERS		
DCE02DT	2:4 Decoder with Enable	4
DCE22	2:4 Decoder with Enable	4
MX22	2:1 MUX	1
MX34	4:1 MUX, 3 Select Inputs	3
MXI02	2:1 MUX, Low Enable, OR Gated Select, Comp. Outputs	3
MXI02DT	2:1 MUX, Low Enable, Complement Outputs	2
MXI02ST	2:1 MUX, Low Enable, 1.2 mA Ioef	4
MXI04	4:1 MUX, Low Enable, Complement Outputs	4
MXI04DT	4:1 MUX, Complement Outputs	3
MXI08ST	8:1 MUX, High Enable, Comp. Outputs 1.2 mA Ioef	9
MXI22	2:1 MUX, Low Enable, OR Gated Select, Comp. Outputs	2
MXI22D	2:1 MUX	2
MXI24DT	4:1 MUX, Low Enable, Complementary Outputs	4
2MX04DT	Dual 4:1 Multiplexer	6
2SELI04D	Dual 4:1 Multiplexer	5
4MXI22D	Quad 2:1 Multiplexer	8
4MXI22S	Quad 2:1 Multiplexer, 1.2 mA Ioef	5
LATCHES, MUX LATCHES		
LAI01	D Latch with Reset and 2-Input OR Enable	2
FLIP-FLOPS		
2DFN04	Dual D Flip-Flop with a Common Clock	4
DFI01	M/S D Flip-Flop with Asynchronous Reset	4
DFI01D	M/S D Flip-Flop with Asynchronous Reset	4
DFI02	M/S D Flip-Flop with Set, Reset, Gated Data & Clock	4
DFI02D	M/S D Flip-Flop with Set, Reset, Gated Data & Clock	4
DFI02DT	M/S D Flip-Flop with Active Low Enable	4
DFI04	M/S D Flip-Flop, Positive Edge Triggered	3
DFI21	M/S D Flip-Flop with Asynchronous Reset	3
DFI22	M/S D Flip-Flop with Scan Input	4
DFS02DT	M/S D Flip-Flop with Scan Input	5
DFS02ST	M/S D Flip-Flop with Scan Input, 1.2 mA Ioef	7
DFS21DT	M/S D Flip-Flop with Scan Input, Data Enable	5
DFS21ST	M/S D Flip-Flop with Scan Input, Data Enable, 1.2 mA Ioef	7
JKI02	M/S JN-K Flip-Flop	4
MXDI02	M/S D Flip-Flop with Multiplexed Data Input	4
COMPARATORS		
None Available at This Time		
MISCELLANEOUS		
AD01	1-Bit Carry Look Ahead Adder	3
FA21D	1-Bit Full Adder w/Gated Inputs	4
FA21S	1-Bit Full Adder w/Gated Inputs, 1.2 mA Ioef	8
HA01D	1-Bit Half Adder	2
HLI01	High-Low Level Generator with Temperature Diode	1
MEMORY		
IDC02X2	Shared Input Buffer, 0.6 mA Ioef	1
IDC12X2	Shared Input Buffer, 0.6 mA Ioef	1
MTX50X2	Shared Output Buffer, 50Ω	1
RS69D	64 X 9 RAM	

Macro Cells Library (Continued)

Input Macros

Name	Function	Cells
BUFFERS, INVERTERS		
IBF02X2 (3)	High Fan-Out Buffer, 10 mA Ioef (Note 1)	1
IBF03X2 (3)	Input Buffer, 0.6 mA Ioef	1
IBFI03X2 (3)	Input Buffer, Complementary Outputs, 0.6 mA Ioef	1
IBFN03X2	Input Buffer, Inverting 0.6 mA Ioef	1
DIFFERENTIAL RECEIVERS		
ICKD0X2	Differential Input Clock Driver, 18 mA Ioef (Note 1)	2
ICKD0X3	Differential Input Clock Driver, 18 mA Ioef (Note 1)	2
ICKD1X2	Differential Input Clock Driver, 18 mA Ioef (Note 2)	2
IRCI02X2 (3)	Differential Input Buffer, Comp. Outputs, 10 mA Ioef	2
IRCI03X2 (3)	Differential Input Buffer, Comp. Outputs, 0.6 mA Ioef	2
GATES		
IOR02X2	2-Input OR, 0.6 mA Ioef	2
IORI02X2	2-Input OR/NOR, 0.6 mA Ioef	2
IORN02X2	2-Input NOR, 0.6 mA Ioef	2
IXOR02X2	2-Input XOR, 0.6 mA Ioef	1
IXORN2X2	2-Input XNOR, 0.6 mA Ioef	1
MISCELLANEOUS		
IN00X2 (3)	Input Pad (Zero Resistance)	1

Note 1: ICKD0X2 and ICKD0X3 uses two external cells for electrical connection and cover, respectively, 90 and 50 internal cells for clock distribution.

Note 2: ICKD12X2 uses two external cells for electrical connection and covers 44 internal cells for clock distribution.

Output Macros

Name	Function	Cells
BUFFERS, INVERTERS		
BF50X2 (3)	Output Buffer, 50Ω, F100K	1
BFI50X3	Complementary Output Buffer, 50Ω, F100K	2
BFN50X2	Output Inverter, 50Ω, F100K	1
RCRI50X3	Differential Output Buffer, 50Ω, F100K	2
GATES		
OR220X2	2-Input OR, 25Ω, F100K	1
ORI220X2	2-Input OR/NOR, 25Ω, F100K	2
OR250X2	2-Input OR, 50Ω, F100K	1
ORN250X2	2-Input NOR, 50Ω, F100K	1
ORI250X2	2-Input OR/NOR, 50Ω, F100K (FGA 14K)	2
ORI250X3	2-Input OR/NOR, 50Ω, F100K (FGA 4K)	2
OR450X2	4-Input OR, 50Ω, F100K	1
ORN450X2	4-Input NOR, 50Ω, F100K	1
ORI450X2	4-Input OR/NOR, 50Ω, F100K	2
BUS DRIVERS		
BD20X2	2-Input OR, 25Ω, F100K	1
BDN20X2 (3)	2-Input NOR, 25Ω, F100K	1

Macro Cells Library (Continued)

Transceivers

Name	Function	Cells
TR20X3	2-Input OR ECL Transceiver, 25Ω	1
TRN20X3	2-Input NOR ECL Transceiver, 25Ω	1
TRN50X2 (3)	2-Input NOR ECL Transceiver, 50Ω	1

Miscellaneous

Name	Function	Cells
OUT00X2 (3)	Output Pad (Zero Resistance)	1

TTL Macros

Name	Function	Cells
INPUT BUFFERS		
TED11X3	TTL Input Buffer	1
TES11X3	TTL Input Buffer (+5V Only)	1
OUTPUT BUFFERS		
TOBD01X3	8 mA TTL Output Buffer	1
TOBD11X3	20 mA TTL Output Buffer	1
TOBS11X3	20 mA TTL Output Buffer (+5V Only)	1
TRANSCEIVERS		
TTRD11X3	20 mA TTL Transceiver	1
TTRS01X3	8 mA TTL Transceiver (+5V Only)	1

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