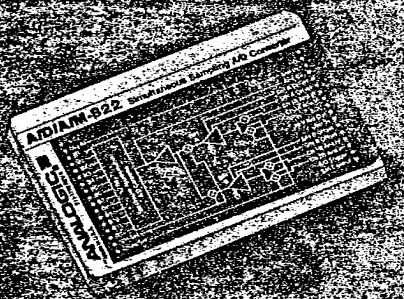


ANALOGIC®

A/D/A/M-822

Simultaneously Sampling Low Cost 12-bit Analog-to-Digital Converter

DESCRIPTION

The A/D/A/M-822 is a self-contained, two-channel, analog-to-digital conversion module complete with two simultaneously operating sample-and-hold (S/H amplifiers, a stable reference, and a 12-bit successive approximation A/D converter. An added feature is the fact that this unit includes four input channels that can be chosen in two groups of two each. This module has been designed to simplify the hardware and software of systems that utilize two or more phase- or time-related signal channels or cross-channel measurements such as quadrature demodulated signal processor front-ends, component transfer function testers, and colorimeters. By adding a multiplexer to each of the four inputs of the A/D/A/M-822, a mini-DAS (Data Acquisition System) can be configured at a very modest cost.

In many systems, information of interest is often carried by the time-or phase-interrelationship among signal channels. Such information may be lost when time-shared S/H's are used or when dedicated S/H's are triggered with insufficient simultaneity. Sequential sampling of the related signals may require costly software correction of errors induced by the sampling process; such correction methods are generally useful only if the delay between samples is known precisely. The A/D/A/M-822 eliminates these sources of error and additional system cost by providing simultaneous sampling of either channel pair—within 5ns of each other. For an equivalent system configuration, only half of the number of A/D converters need be used, further reducing overall system costs.

The specification for the A/D/A/M-822 is based on an end-to-end error budget that accounts for all internal error sources, including S/H droop at a 26 kHz sampling rate, error due to aperture uncertainty for band limited signals up to 12.5 kHz, S/H pedestal non-linearities, input switching crosstalk, and A/D non-linearities. With a throughput time for two digitized samples of less than 40 microseconds, it provides 12-bit (±1 LSB) overall accuracy. The use of discrete component S/H amplifiers contributes greatly to the overall accuracy of the A/D/A/M-822—

(continued on page 3)

FEATURES

- **Guaranteed Overall Transfer Accuracy**
  ±0.025% FSR, maximum
- **High Throughput Rate at Low Cost**
  Two Channels at 26,000 samples per second each
  Single Channel at 52,600 samples per second
- **Low Aperture Uncertainty Time—5 ns**
  Minimizes phase error between simultaneously sampled channels
- **Universal Data Systems Compatibility**
  Standard TTL digital inputs/outputs
- **Low Power**
  1.25W, typ.
- **Low Noise**
  0.01% FSR
- **Flexibility**
  Independently selectable input channel pairs
  Multiple units can be driven by single TTL line driver for multiple simultaneously sampled channels
- **Ratiometric Operation**
- **Superior Performance**
  Lower cost and higher overall accuracy when compared to functionally equivalent designs based on integrated circuits.
- **Small Size**
  2" X 3" X 0.375"
  (50.8 mm X 76.2 mm X 9.53 mm)
- **RFI & EMI Shielded**

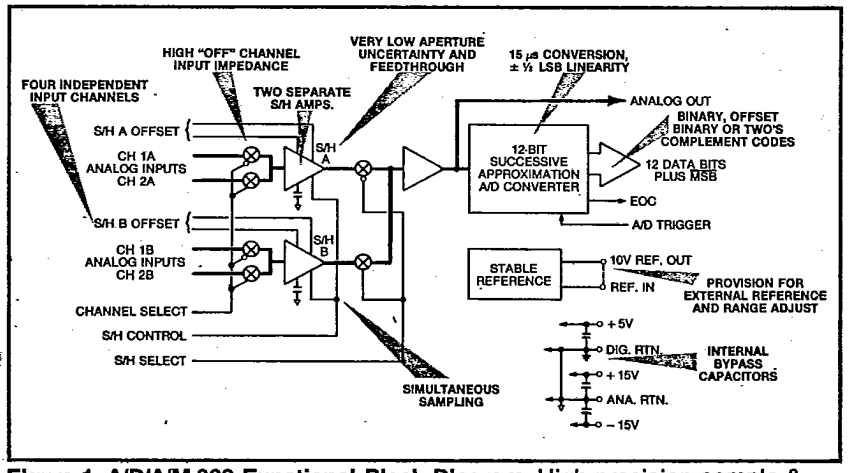


Figure 1. A/D/A/M-822 Functional Block Diagram. High precision sample & holds ensure low aperture uncertainty and high measurement accuracy.

ANALOGIC®
Solutions...not Slogans

A/D/A/M 822 SPECIFICATIONS

ANALOG INPUTS

Number of Channels	4 (2 pair)
Configuration	Voltage follower input
Full Scale Range (FSR)	0 to +10V, ±5V, ±10V (see Ordering Guide)
Maximum Input Without Damage	±15V
Input Impedance	>100 MΩ
Input Bias Current[1]	≤1nA (at 25°C)

ACCURACY (at 26 kHz sampling rate and 25°C, nominal)

Relative Accuracy[2]	±0.025% FSR max.
Differential Non-Linearity	±½ LSB max.
±3σ Noise (Shorted Input; measured over dc to 1 MHz Bandwidth)	0.01% FSR, p-p Referenced to Input, max.
Monotonicity	Guaranteed; No missing codes
S/H Hold Mode Feedthrough Rejection Ratio[3]	−82 dB; 1 kHz square wave, full scale
Channel-to-Channel Crosstalk[4]	−110 dB @ 10 kHz
Offset Error (Untrimmed)[5]	25 mV, max.; adjustable to zero
Gain Error (Untrimmed)[5,6]	±0.25% FSR max.
Gain Accuracy Between Channels	±7.5 mV max.

DYNAMIC PERFORMANCE

Maximum Dual Channel Sampling Rate[7]	26 kHz (2 samples/39 microseconds)
Maximum Single Channel Sampling Rate[8]	52.6 kHz
S/H Acquisition Time to ½ LSB	5 μs max.
S/H Aperture Delay Time	50 ns typ.
S/H Aperture Uncertainty Time	5 ns typ.
S/H Droop Rate (at 25°C)[1]	0.02 μV/μs typ., 0.2 μV/μs max.
Input Switching and S/H Multiplexer Settling Time to ± ½ LSB	Refer to timing diagram (Figure 2)

STABILITY

Tempco of Differential Non-Linearity	±3 ppm/°C FSR max.
Tempco of Offset — Unipolar	±10 ppm/°C, FSR max.
Tempco of Offset — Bipolar	±15 ppm/°C, FSR max.
Tempco of Gain	±20 ppm/°C, FSR max.
Power Supply Sensitivity	0.003% FSR/% change in V_{supply}
Recommended Recalibration Interval	6 months
Warm-up Time to Specified Accuracy	5 minutes

DIGITAL INTERFACES

General	Inputs: 1 TTL LS load, each; Outputs: 2 TTL load fanout, each
	TTL positive true is logic "1" Logic "0": 0.4V max. for outputs; 0.8V max. for inputs Logic "1": 2.4V min. for outputs; 2.0V min. for inputs

Inputs

Input Channel Select	Logic "0" selects channel 1; logic "1" selects channel 2
S/H Select	Logic "0" selects S/H A; logic "1" selects S/H B
S/H (Mode) Control	Logic "0" selects HOLD mode; logic "1" selects SAMPLE
A/D Trigger	Positive pulse, trailing edge triggered; 0.1 μs pulse width minimum

Outputs

Data	12 data bits in Binary, 2's Complement, or Offset Binary (see Coding Table for format)
EOC	Logic "1" during conversion

POWER & ENVIRONMENTAL

Analog Power Requirements[9]	+15V ±3% @ 35 mA, typ. & −15V @ 35 mA, typ.
Digital Power Requirement[9]	+5V, ±3% 40 mA, typ.
Operating Temperature	0°C to 70°C
Storage Temperature	−25°C to +85°C
Relative Humidity	Up to 95%, non-condensing
Modupac™ Dimensions	2" X 3" X 0.375" (50.8 mm X 76.2 mm X 9.53 mm)
Electromagnetic Shielding	5 sides
Electrostatic Shielding	6 sides

NOTES:

1. Doubles every 10°C.
2. Includes effects of input switching, buffer amplifiers, S/H Amp and ADC.
3. Measured on S/H output, in HOLD mode with input signal as stated.
4. Measured on Channel A S/H output with input grounded. Input signal applied to Channel B input. Both channels in SAMPLE mode.
5. Offset and gain errors are externally adjustable — see Figures 3 and 4.
6. With 50Ω, 1% fixed resistor installed per Figure 4.
7. On ±10V FSR.
8. On ±5V FSR; 50 kHz on ±10V FSR.
9. Digital Ground, Analog Ground, and case are tied internally.

2

DESCRIPTION

(continued from page 1)

by contrast functionally comparable monolithic S/H's commonly exhibit more than 1 LSB equivalent error at the 12-bit level by themselves.

As a member of the A/D/A/M series of analog data acquisition modules, the A/D/A/M-822 is fully integrated and tested as a subsystem. This frees the system engineer from performing a myriad of time-consuming design tasks and minimizes system production and test efforts. With no need to design a printed circuit layout for critical analog components, users avoid potential costly PC design iterations, which are commonly required to eliminate ground loops and other noise and error sources. A fully tested and shielded subsystem, the A/D/A/M-822 offers superior performance, ease of use, and integration, at a lower cost than the parts alone for a comparable custom design.

TYPICAL TIMING

Figure 2 shows a typical timing relationship among the various control signals required by the A/D/A/M-822. In this example, channels 2A and 2B are selected first. Their input signals are sampled simultaneously, then the samples are sequentially converted to digital data. Subsequently, the process is repeated for channels 1A and 1B.

The S/H amplifiers require 5 μs to simultaneously acquire the signals on both input channels (to within ½ LSB for a worst case full-scale input step). Once the signal pair is acquired, the S/H Control can be switched to the HOLD mode. Because the sample-to-hold-mode settling time (input switch settling time) is less than the A/D Trigger's internal propagation delay, the S/H Control input can be used as the A/D Trigger input, if the application warrants.

The diagram shows input switch settling time and S/H Select settling time to be 2 μs each. These are maximum times; typical values are 1 μs each. The diagram also shows that the output data from the A/D converter is valid at the instant of the EOC falling edge transition. The output data can be read at this instant or at any time up to the next A/D Trigger, since the last bit (LSB) decision is made, and the result settled, prior to the EOC transition. The S/H Control can be switched to SAMPLE while the data is being read, with no effect on the data.

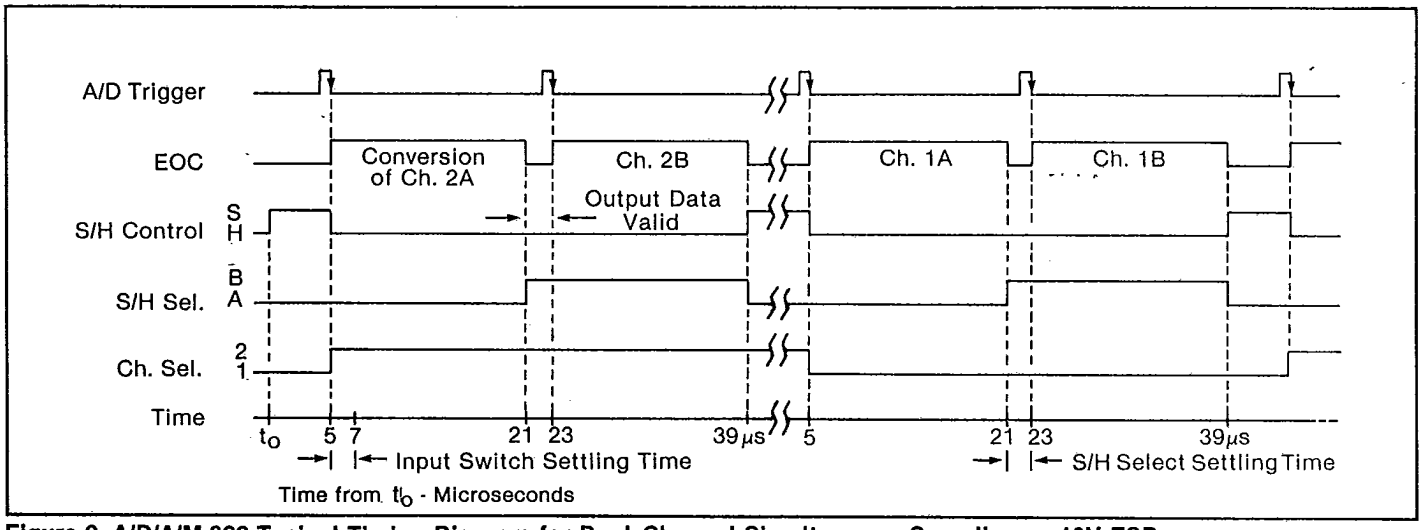


Figure 2. A/D/A/M-822 Typical Timing Diagram for Dual-Channel Simultaneous Sampling, ±10V FSR.

OUTPUT CODING

Unipolar Binary		Offset Binary*		Two's Complement*	
Input	B1, B2, ..., B12	Input	B1, B2, ..., B12	Input	$\overline{B1}$, B2, ..., B12
+9.9976V	111 111 111 111	+9.9951V	111 111 111 111	+9.9951V	011 111 111 111
0.0000V	000 000 000 000	0.0000V	100 000 000 000	0.0000V	000 000 000 000
		−10.0000V	000 000 000 000	−10.0000V	100 000 000 000

*For ±5V Full Scale Range, divide voltages by 2

ADJUSTMENTS & CALIBRATION

OFFSET

A separate, external 20 kΩ multi-turn potentiometer for each S/H amplifier is recommended, per Figure 3. The +15V source used to power the A/D/A/M-822 may be used for the offset circuit as well.

With S/H A selected and the S/H Control line at logic "1" (Sample), supply the input indicated in the Calibration Voltages table to either Ch. 1 or Ch 2. Adjust the S/H A offset pot until the LSB of the output data word varies equally between 0 and 1. Repeat the above procedure for S/H B.

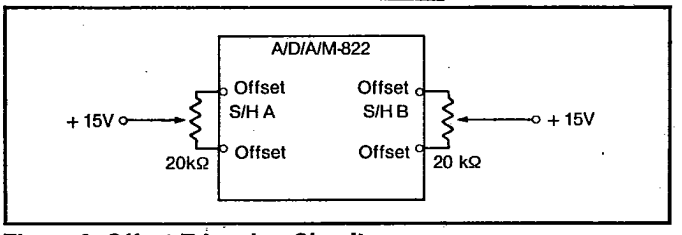


Figure 3. Offset Trimming Circuit.

GAIN

If gain trimming is required by the application, a 100Ω, multi-turn potentiometer connected between the 10V Ref Out and Ref In pins per Figure 4 will provide an approximate ±0.25% FSR adjustment in gain. For many applications, a fixed, 50Ω 1% resistor may be used in place of the trimpot.

Gain will rarely require recalibration in most applications. If gain is to be adjusted, follow the procedure below, after performing the offset adjust procedure for both S/H's.

Select any channel by providing the appropriate logic levels to the Channel Select, S/H Select, and S/H Control lines (S/H Control should be in the SAMPLE mode—logic "1"). Supply the input indicated in the Calibration Voltages table to the selected channel. Adjust the optional 100Ω trimpot until the LSB of the data word varies equally between 0 and 1.

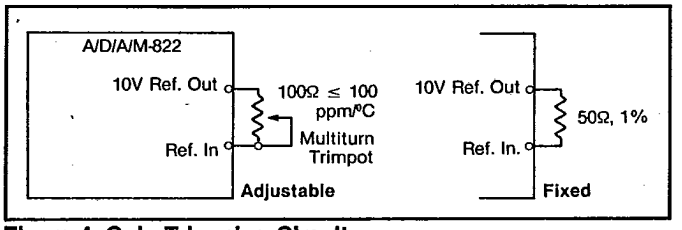
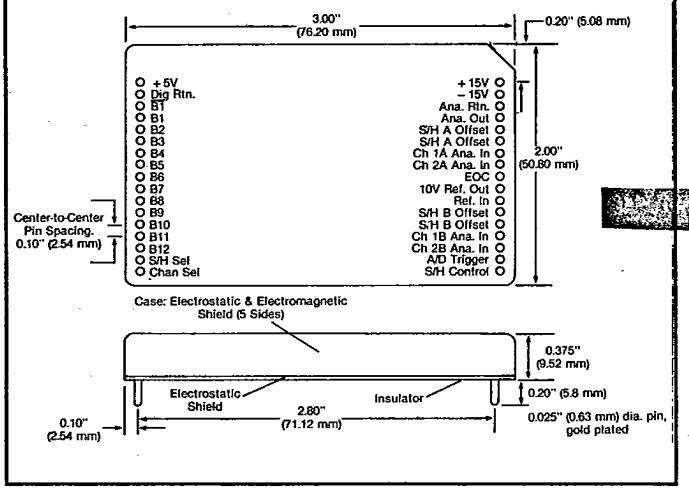


Figure 4. Gain Trimming Circuit.

Calibration Voltages

Adjustment Procedure	Input Full Scale Range		
	0 to +10V	±10V	±5V
Offset	+0.0012V	+0.0024V	+0.0012V
Gain	+9.9976V	+9.9951V	+4.9975

MOUNTING DIMENSIONS & PINOUTS



ORDERING GUIDE

For an input voltage range of:	Simply Specify:
0 to +10V FSR	☐ A/D/A/M 822-1
±10V FSR	☐ A/D/A/M 822-2
±5V FSR	☐ A/D/A/M 822-3

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