FLOPPY DISK CONTROLLER

DESCRIPTION

The μPD372D is a single LSI floppy disk controller chip which contains the circuitry to read, write, track seek, load and unload the head, generate and detect CRC characters, and perform all other floppy disk operations. It is completely compatible with the IBM, Minifloppy*TM, hard sector, and other formats and controls up to 4 floppy disk drives. The μPD372D may be interfaced directly to a host processor; or to a controller processor first, which in turn is interfaced to the host. These processors do not necessarily have to be of the 8080A type.

Data transfers to and from the μPD372D are done through addressable internal registers. These internal regsiters allow a large variety of system architectures to be configured; they provide status information on the drive, as well as perform data transfers between the drive and the processor.

The μPD372D issues interrupts to the processor upon detection of an address mark and then when each subsequent data byte is available during either reading or writing. An 8-bit bi-directional data bus and 5 register select lines provide access to the 9 internal registers' contents. An internal interval timer is provided which facilitates performing such drive timing functions as: stepping rate, head settling time, track settling time, etc.

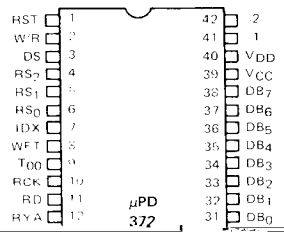
*TMShugart Associates.

FEATURES

- Compatible with IBM 3740 format
- Also compatible with other formats including Minifloppy and hard sector
- Controls up to four floppy disk drives
- Can perform overlap seeks
- Input and output TTL compatible (except for $\phi 1$ and $\phi 2$)
- Interfaces to most microprocessors including 8080A
- Standard power supplies (+12V, +5V and –5V)
- Controls most floppy disk drives including:

CALCOMP 140, 142	ORBIS 74, 76/77
CDC BR803	PERSCI 70, 75
INNOVEX 210, 410	REMEX RFS 7400
PERTEC FD400	SHUGART SA400 (Minifloppy)
POTTER DD4740	WANGCO 82 (Minifloppy)
SHUGART SA900, SA800	GSI MDD50 (Minifloppy)
GSI 110	

PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−1.0 to +8 Volts①
All Input Voltages	−1.0 to +8 Volts①
Clock Voltage	−1.0 to +16 Volts①
Supply Voltage V_{DD}	−1.0 to +16 Volts①
Supply Voltage V_{CC}	−1.0 to +8 Volts①
Supply Voltage V_{BB}	−10 to +0 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

Note: ① V_{BB} = −5V ± 5%

DC CHARACTERISTICS

T_a = −70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
High Level Input Voltage	V_{IH}	+3.0		V_{CC}	V	
Low Level Input Voltage	V_{IL}	0		+0.8	V	
High Level Output Voltage	V_{OH}	+3.5			V	I_{OH} = −1.0 mA
Low Level Output Voltage	V_{OL1}①			+0.5	V	I_{OL} = +1.7 mA
	V_{OL2}②			+0.5	V	I_{OL} = +3.3 mA
High Level Clock Voltage	$V_{\phi H}$	+9		V_{DD}	V	
Low Level Clock Voltage	$V_{\phi L}$	0		+0.8	V	
High Level Input Leakage Current	I_{LIH}			+10	μA	V_I = +3.0V
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_I = +0.8V
High Level Clock Leakage Current	$I_{L\phi H}$			+10	μA	V_ϕ = +9.0V
Low Level Clock Leakage Current	$I_{L\phi L}$			−10	μA	V_ϕ = +0.8V
High Level Output Leakage Current	I_{LOH}			+10	μA	V_O = +3.5V
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_O = +0.5V
Power Supply Current (V_{DD})	I_{DD}		+20		mA	
Power Supply Current (V_{CC})	I_{CC}		+23		mA	
Power Supply Current (V_{BB})	I_{BB}			−2	mA	

Notes: ① CKS, REQ, UA_0, UA_1, UB_0, UB_1, DB_0–DB_7.
② WD, HLD, LCT, WE, WFR, SOS, SID.

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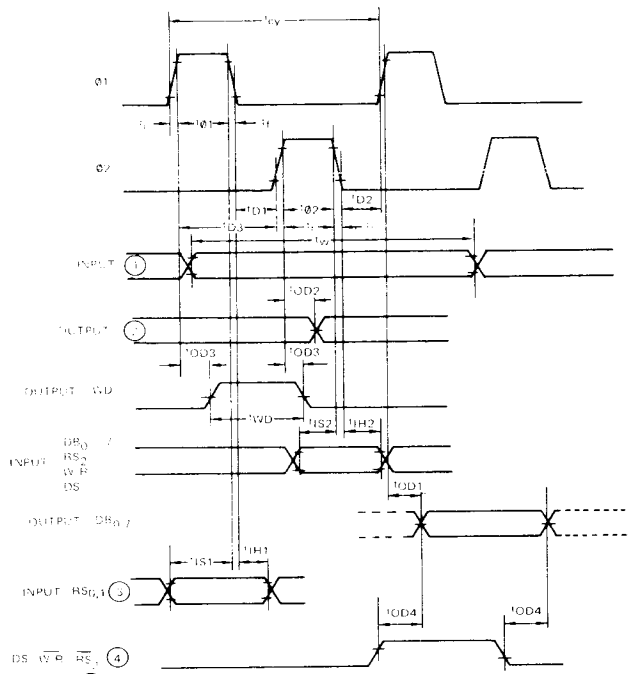
AC CHARACTERISTICS

T_a = 0 to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY}	480		2000	ns	
Clock Rise and Fall Times	t_r, t_f	0		50	ns	
Ø1 Pulse Width	$t_{\phi 1}$	60			ns	
Ø2 Pulse Width	$t_{\phi 2}$	90			ns	
Ø1 to Ø2 Delay	t_{D1}	0			ns	
Ø2 to Ø1 Delay	t_{D2}	70			ns	
Delay Ø1 to Ø2 Leading Edges	t_{D3}	100			ns	
Data Out Delay from Ø1	t_{OD1}			90	ns	1 TTL and C_l = 30 pF
Data Out Delay from Ø2 ①	t_{OD2}			200	ns	1 TTL and C_l = 30 pF
Data Out Delay from Ø2 ②	t_{OD2}			200	ns	2 TTL and C_l = 50 pF
WD Delay Time	t_{OD3}			120	ns	2 TTL and C_l = 50 pF
Data Out Delay from DS · $\overline{WR}$ · $\overline{RS_2}$	t_{OD4}			200	ns	
Data Setup Time to Ø1	t_{IS1}	150			ns	
Data Setup Time to Ø2	t_{IS2}	120			ns	
Data Hold Time from Ø1	t_{IH1}	10			ns	
Data Hold Time from Ø2	t_{IH2}	10			ns	
WD pulse width	t_{WD}	t_{D3}+40	t_{D3}		ns	
Input pulse width ③	t_W	t_{CY}+150			ns	

Notes: ① CKS, AWL, REQ, UA_0, UA_1, UB_0, UB_1.
② HLD, LCT, WFR, WE, SOS, SID.
③ IDX, RYA, RYB, RST, WFT, T_{00}, WCK, RCK.

TIMING WAVEFORMS



Notes: ① IDX, RYA, RYB, RST, WFT, T_{00}, WCK, RCK.
② CKS, WFR, SOS, SID, REQ, HLD, $UA_{0,1}$, $UB_{0,1}$, WE, LCT.
③ RS_0, RS_1 input must not make level transition within t_{IS1} and t_{IH1} times, or register contents may be modified.
④ The logic condition which places μPD372 information on DB_{0-7} is DS · $\overline{WR}$ · $\overline{RS_2}$. Care must be taken to insure that this condition is not met inadvertently if DS, WR and RS_2 are allowed to change state asynchronously.

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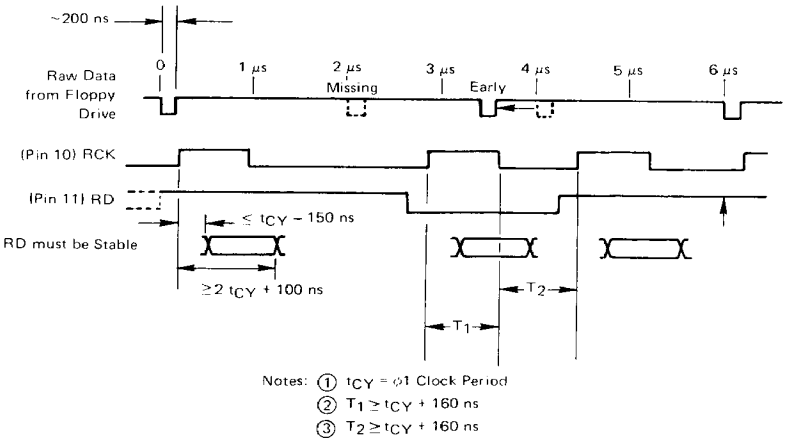
READ CLOCK (RCK) AND READ DATA (RD) REQUIRED BY μPD372



Notes: ① t_{CY} = Φ1 Clock Period
② $T_1 \geq t_{CY} + 160$ ns
③ $T_2 \geq t_{CY} + 160$ ns

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	INPUT/ OUTPUT	CONNECTION	FUNCTION
1	RST	Reset	Input	Processor	Initializes internal registers, counters and F/F's
2	W/R	Register Write/ Read Select			W/R = 1 implies DB_{0-7} data written into μPD372 registers
3	DS	Data Strobe			DB_{0-7} Write and read strobe
4-6	RS_0 RS_1 RS_2	Register Select			Internal Register Select
7	IDX	Index		FDD	Pulse Signal that indicates start of Disk track
8	WFT	Write Fault			Write Fault Signal
9	T_{00}	Track 00			Indicates that Head is positioned on Track 00
10	RCK	Read Clock			
11	RD	Read Data			
12	RYA	Ready A			Indicates that FDD A is Ready
13	WCK	Write Clock		Processor	
14	RYB	Ready B		FDD	Indicates that FDD B is Ready
15	CKS	Clock States	Output		
16	AWL	Always Low			Always a logic zero
17	REQ	Request		Processor	Interrupt Request
18	WD	Write Data		FDD	Serial Write Data (Clock & Data Bits)
19	HLD	Head Load			Command which causes R/W head to contact disk
22	LCT	Low Current			Command to lower write current for inner tracks
23	WFR	Write Fault Reset			Signal to reset write fault latch
24	WE	Write Enable			
25	SID	Step In or Direction			R/W head step control
26	SOS	Step Out or Step			R/W head step control
27-30	UA_0, UA_1 UB_0, UB_1	FDD Select			FDD Unit Select
31-38	DB_{0-7}	Data Bus	Input/ Output	Processor	Bi-directional data bus

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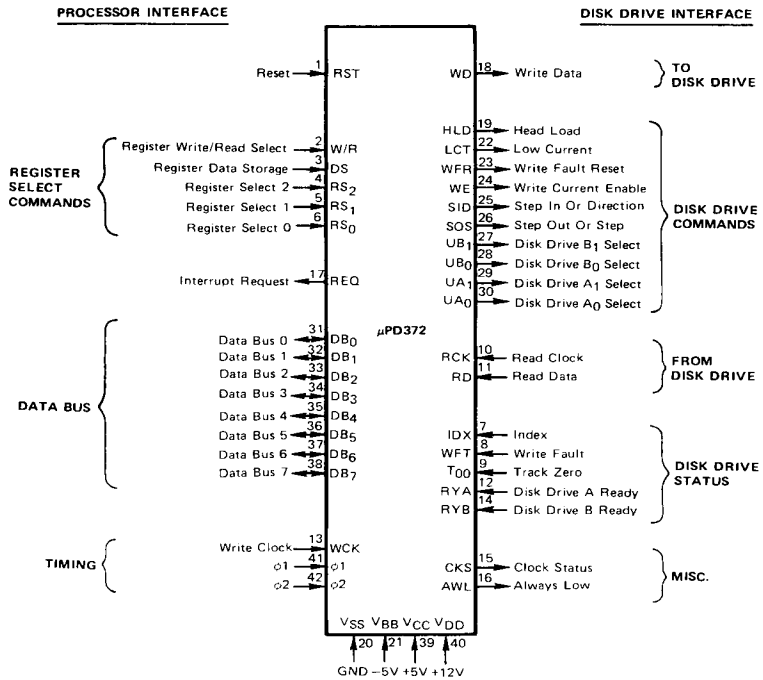
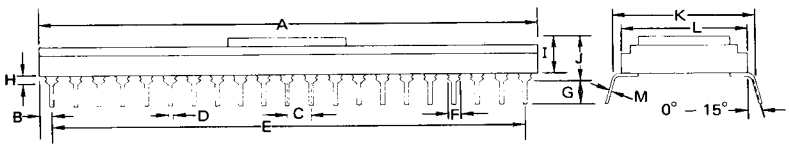
PIN IDENTIFICATION (CONT.)



PACKAGE OUTLINE μPD372D



ITEM	MILLIMETERS	INCHES
A	53.5 MAX	2.1 MAX
B	1.35	0.05
C	2.54	0.10
D	50.80	2.0
F	1.27	0.05
G	2.54 MAX	0.10 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.21 MAX
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

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BIT	SYMBOL	NAME	FUNCTION
		WRITE REGISTER 0	
0		Not Used	
1	WFR	Write Fault Reset	Resets Pin 23 to Zero
2	LCT	Low Current	Sets Pin 22, Should be Zero for TRKS > 43
3	HLD	Head Load	Sets Pin 19, Loading FDD Head
4		Not Used	
5		Not Used	
6	MBL	Must Be Low	
7	RST	Reset	Software Reset, Same Effect as Pin 1
		WRITE REGISTER 1	
0	UA_0	Unit A_0 Select	Device Select Pin 30
1	UA_1	Unit A_1 Select	Device Select Pin 29
2	UAS	Unit A Strobe	Strobe for Enabling UA_0 and OA_1 to be Loaded
3	CB_3	Clock Bit 3	Enables Clock Pulse #3 to be Written
4	CB_4	Clock Bit 4	Enables Clock Pulse #4 to be Written
5	CB_5	Clock Bit 5	Enables Clock Pulse #5 to be Written
6		Not Used	
7	CBS	Clock Bit Strobe	Enables Clock Bits to be Loaded
		WRITE REGISTER 2	
0	WD_0	Write Data Bit 0	
1	WD_1	Write Data Bit 1	
2	WD_2	Write Data Bit 2	
3	WD_3	Write Data Bit 3	
4	WD_4	Write Data Bit 4	
5	WD_5	Write Data Bit 5	
6	WD_6	Write Data Bit 6	
7	WD_7	Write Data Bit 7	
		WRITE REGISTER 3	
0	CCW	Cyclic Check Words	One During R/W, Zero for CRC Reset
1	CCG	Cyclic Check Generator Start	Starts CRC Generator in Write Mode
2	WER	Write Enable Reset	Resets Pin 24 to Zero
3	IXS	Index Start	Enable Index Hole Detection
4	WES	Write Enable Set	Sets Pin 24 to One
5	STT	Start	Enables Read and Write Operations to Occur
6	WCS	Write Clock Set	Write Clock Selected
7	RCS	Read Clock Set	Read Clock Selected
		WRITE REGISTER 4	
0	UB_0	Unit B_0 Select	Device Select Pin 28
1	UB_1	Unit B_1 Select	Device Select Pin 27
2	UBS	Unit B Strobe	Strobe for Enabling UB_0, UB_1 to be Loaded
3		Not Used	
4		Not Used	
5	SOS	Step Out or Step	Sets Pin 26 to One
6	SID	Step In or Direction	Sets Pin 25 to One
7	STS	Step Strobe	Enables SOS and SID to be Loaded
		WRITE REGISTER 5	
0–7		This Register Not Used	
		WRITE REGISTER 6	
0	DRR	Data Register Reset	Resets DRQ (RR_0 Bit 0)
1	IRR	Index Request Reset	Resets IRQ (RR_0 Bit 1)
2	TRR	Timer Request Reset	Resets TRQ (RR_0 Bit 2)
3		Not Used	
4		Not Used	
5		Not Used	
6		Not Used	
7		Not Used	

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INTERNAL REGISTER IDENTIFICATION (CONT.)

BIT	SYMBOL	NAME	FUNCTION
READ REGISTER 0			
0	DRQ	Data Request	Read Data Byte from RR_2 or Write Data Byte into WR_2
1	IRQ	Index Request	Set by Physical Index Pulse
2	TRQ	Timer Request	Set by Every 512th Write CLK Pulse
3	ERR	Error	Logical OR of WFT + RYA + COR
4	UB_0	Drive B_0 Selected	
5	UB_1	Drive B_1 Selected	
6	RYB	Drive B Ready	Ready Signal from Pin 14
7	ALH	Always High	Always Contains a Logical One
READ REGISTER 1			
0	UA_0	Drive A_0 Selected	
1	UA_1	Drive A_1 Selected	
2	WFT	Write Fault	Indicates Status of Pin 8
3	RYA	Drive A Ready	Indicates Status of Pin 12
4	COR	Command Overrun	Processor Did Not Respond in Time to a DRQ
5	DER	Data Error	CRC Error During Read
6	T_{00}	Track Zero	Indicates Status of Pin 9
7	WRT	Write Mode	Indicates which Clock WCK or RCK has been Selected
READ REGISTER 2			
0	RD_0	Read Data Bit 0	
1	RD_1	Read Data Bit 1	
2	RD_2	Read Data Bit 2	
3	RD_3	Read Data Bit 3	
4	RD_4	Read Data Bit 4	
5	RD_5	Read Data Bit 5	
6	RD_6	Read Data Bit 6	
7	RD_7	Read Data Bit 7	

ADDRESSABLE INTERNAL REGISTERS

Data is transferred to the μPD372's internal addressable registers by signals W/R (Write=1, Read=0), DS (Data Strobe) and RS_0–RS_2 (Register Select 0, 1 and 2). Timing constraints for these signals are shown in the Timing Diagram. Diagram below shows register allocations and functional content.

REGISTER ADDRESS				REGISTER NAME	BIT NUMBERS							
W/R	RS_2	RS_1	RS_0		7	6	5	4	3	2	1	0
WRITE REGISTERS												
1	0	0	0	WR_0	RST	MBL	X	X	HLD	LCT	WFR	X
1	0	0	1	WR_1	CBS	X	CB_5	CB_4	CB_3	UAS	UA_1	UA_0
1	0	1	0	WR_2	WD_7	WD_6	WD_5	WD_4	WD_3	WD_2	WD_1	WD_0
1	0	1	1	WR_3	RCS	WCS	STT	WES	TXS	WER	CCG	CCW
1	1	0	0	WR_4	STS	SID	SOS	X	X	UBS	UB_1	UB_0
1	1	1	0	WR_6	X	X	X	X	X	TRR	IRR	DRR
READ REGISTERS												
0	0	0	0	RR_0	ALH	RYB	UB_1	UB_0	ERR	TRQ	IRQ	DRQ
0	0	0	1	RR_1	WRT	T_{00}	DER	COR	RYA	WFT	UA_1	UA_0

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