

Octal Counter/Divider

The TC74HC4022A is a high speed CMOS OCTAL COUNTER DIVIDER fabricated with silicon gate C²MOS technology.

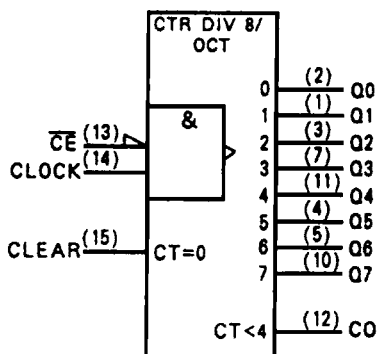
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It contains 4-stage divided-by-8 Johnson counter with 8 decoded output (Q0 ~ Q7) and carry-out bit.

The counter is advanced on the positive edge of clock signal when clock enable signal **CLOCK ENABLE** input is held low, or it is advanced on the negative edge of the enable signal when **CLOCK** input is held high, and selected one of ten outputs goes high. Holding high the **CLEAR** input, this counter is cleared to its zero state without regard to the other input conditions.

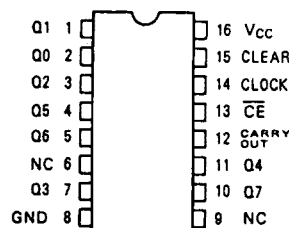
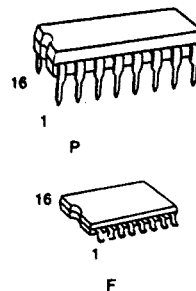
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High Speed: $f_{MAX} = 57\text{MHz(Typ.)}$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation: $I_{CC} = 4\mu\text{A(Max.)}$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%V_{CC}(\text{Min.})$
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $I_{OH} = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays: $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range: $V_{CC}(\text{opr}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 4022B



IEC Logic Symbol



(TOP VIEW)

Pin Assignment

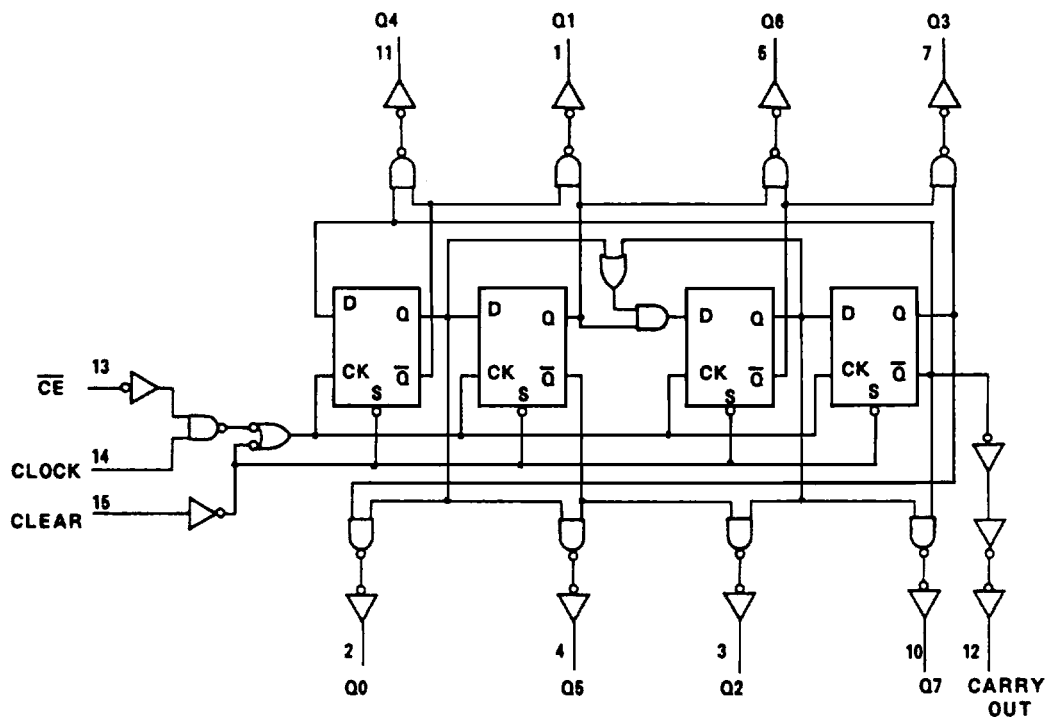
Truth Table

Inputs			Decode Output (H)
CLOCK	CE	CLEAR	
X	X	H	Q ₀
L	X	L	Q _n
X	H	L	Q _n
	L	L	Q _{n+1}
	L	L	Q _n
H		L	Q _n
H		L	Q _{n+1}

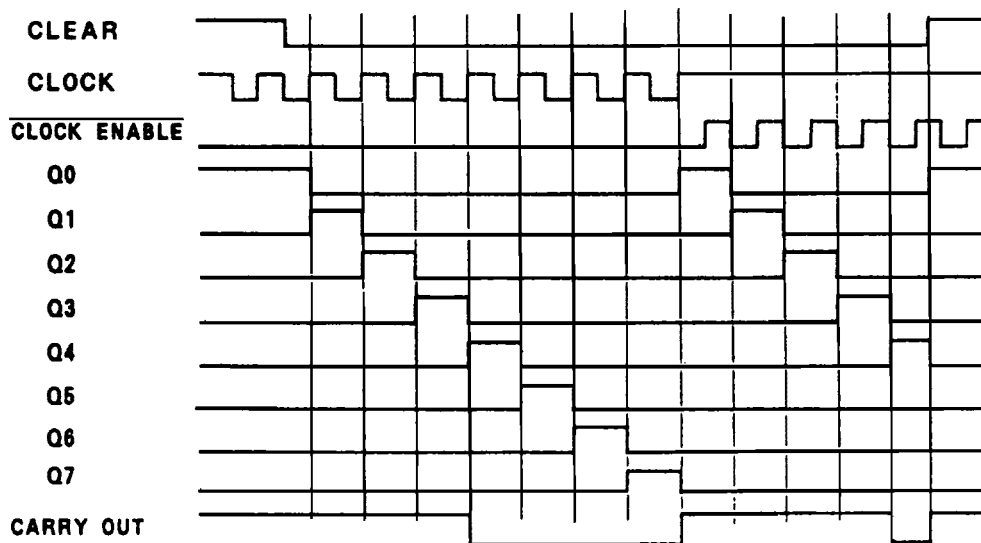
X: Don't Care

Carry Out "H"...Q₀~Q₄ = "H"

"L"...Q₅~Q₉ = "H"



Logic Diagram



Timing Chart

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} /Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SO1C)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000($V_{CC} = 2.0\text{V}$) 0 ~ 500($V_{CC} = 4.5\text{V}$) 0 ~ 400($V_{CC} = 6.0\text{V}$)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit	
				VCC	Min.	Typ.	Max.	Min.		Max.
High-Level Input Voltage	V _{IH}	—		2.0 4.5 6.0	1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	V	
Low-Level Input Voltage	V _{IL}	—		2.0 4.5 6.0	— — —	— — —	0.5 1.35 1.8	— — —	V	
High-Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			I _{OH} = -4 mA I _{OH} = -5.2mA	6.0	5.9	6.0	—	5.9	—	
				4.5	4.18	4.31	—	4.13	—	
Low-Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			I _{OL} = 4 mA I _{OL} = 5.2mA	6.0	—	0.0	0.1	—	0.1	
				4.5	—	0.17	0.26	—	0.33	
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	6.0	—	—	±0.1	—	±1.0	μA	
										4.0
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		6.0	—	—	4.0	—	40.0	

Timing Requirements (Input $t_r = t_f = 6\text{ns}$)

Parameter	Symbol	Test Condition	V_{CC}	Ta = 25°C		Ta = -40 ~ 85°C	Unit
				Typ.	Limit	Limit	
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (CLEAR)	$t_{W(H)}$	—	2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time	t_s	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Hold Time	t_h	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Removal Time (CLEAR)	t_{rem}	—	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Clock Frequency	f	—	2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	36	29	

AC Electrical Characteristics ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, Ta = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation Delay Time (CLOCK, CE-Q, CARRY)	t_{PLH} t_{PHL}	—	—	17	27	
Propagation Delay Time (CLEAR-Q, CARRY)	t_{PLH} t_{PHL}	—	—	15	25	
Maximum Clock Frequency	f_{MAX}	—	33	57	—	MHz

AC Electrical Characteristics ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Parameter	Symbol	Test Condition	V_{CC}	Ta = 25°C			Ta = -40 ~ 85°C		Unit
				Min	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time (CLOCK, CE-Q, CARRY)	t_{PLH} t_{PHL}	—	2.0	—	71	160	—	200	
			4.5	—	21	32	—	40	
			6.0	—	16	27	—	34	
Propagation Delay Time (CLEAR-Q, CARRY)	t_{PLH} t_{PHL}	—	2.0	—	69	145	—	180	ns
			4.5	—	19	29	—	36	
			6.0	—	15	25	—	31	
Maximum Clock Frequency	f_{MAX}	—	2.0	6	11	—	5	—	MHz
			4.5	31	51	—	25	—	
			6.0	36	63	—	29	—	
Input Capacitance	C_{IN}	—	—	—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$	—	—	—	53	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$