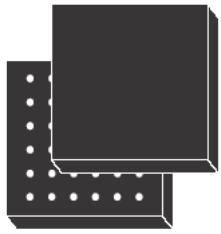
ST6G3240

Dual supply level translator for dual memory cards (mini SD/micro SD + managed NAND)

Features

- High speed: t_{PD} (A to B) = 5 ns at T_A = 85 °C with V_{CCA} = 1.8 V, V_{CCBn} = 3.0 V
- Low power dissipation: $I_{CCA} = I_{CCBn}$ = 5 µA (max.) at T_A = 85 °C
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Operating voltage range:
  - V_{CCA} (opr) = 1.4 to 3.6 V
  - V_{CCBn} (opr) = 1.4 to 3.6 V
- B-side power supplies (V_{CCB1} and V_{CCB2}) can be different and separately controlled
- Interchangeable voltage levels: V_{CCA} can either be greater than or less than V_{CCBn}
- Low power mode: when V_{CCBn} is grounded or floating, there is very low quiescent current on V_{CCA}
- Power down detection: when either one of the B-side power supplies (V_{CCB1} and V_{CCB2}) is grounded or floating, the corresponding port-n goes into high-Z state automatically
- Latch-up performance exceeds 500 mA (JESD17)
- ESD protection: 2 kV HBM
- Integrated pull-up resistor and level translator on the MS_Insert pin
- Integrated pull-up resistor for card-detect pin



µTFBGA 36

Description

The ST6G3240 is a dual supply low voltage CMOS level translator supporting the dual function of mini SD/micro SD card and managed NAND memories. It is designed for use as an interface between three systems using 3.3, 2.5 and 1.8 V respectively.

The ST6G3240 is capable of achieving high speed operation and at the same time maintaining low power dissipation.

While the A port is designed to track V_{CCA}, the Bn port (nCMD, nDAT, nCLK) is designed to track V_{CCBn}.

The device is intended for a two-way asynchronous communication between data buses.

Table 1. Device summary

Order code	Package	Packing
ST6G3240TBR	µTFBGA36 (3.6 x 3.6 mm)	Tape and reel

Contents

1 ST6G3240 general description

The ST6G3240 is a dual supply low voltage CMOS level translator supporting the dual function of mini SD/micro SD card and managed NAND memories. It is designed for use as an interface between three systems using 3.3, 2.5 and 1.8 V respectively.

The ST6G3240 is capable of achieving high speed operation and at the same time maintaining low power dissipation.

While the A port is designed to track V_{CCA}, the Bn port (nCMD, nDAT, nCLK) is designed to track V_{CCBn}.

The device is intended for a two-way asynchronous communication between data buses. The direction of data transmission is determined by CMD-dir/DATA0-dir/DAT123-dir inputs. In the typical application the Bn-port interfaces with the 3 V bus and the A-port with the 1.8V bus.

With interchangeable voltage levels, there is no restriction on the voltage settings for each supply. V_{CCA} can be less than or greater than V_{CCB1} or V_{CCB2}. For example, V_{CCA} = 2.5 V, V_{CCB1} = 3.6 V, V_{CCB2} = 1.8 V.

Full low power mode

This device can be entered into 'full lower power mode' by setting all the INn pins to low or high, which will disable the device completely.

Partial low power mode

Alternatively, the device can be set into 'partial low power mode' by grounding or floating one of the V_{CCBn} power supplies. This will set all the corresponding output Port-n to High-Z.

However, it is important to note that V_{CCA} power supply must not be grounded or floating whenever V_{CCBn} is connected to a power supply as this will lead to significant current consumption increase.

2 Pin settings

2.1 Pin connection

Figure 1. Pin connection (top through view)

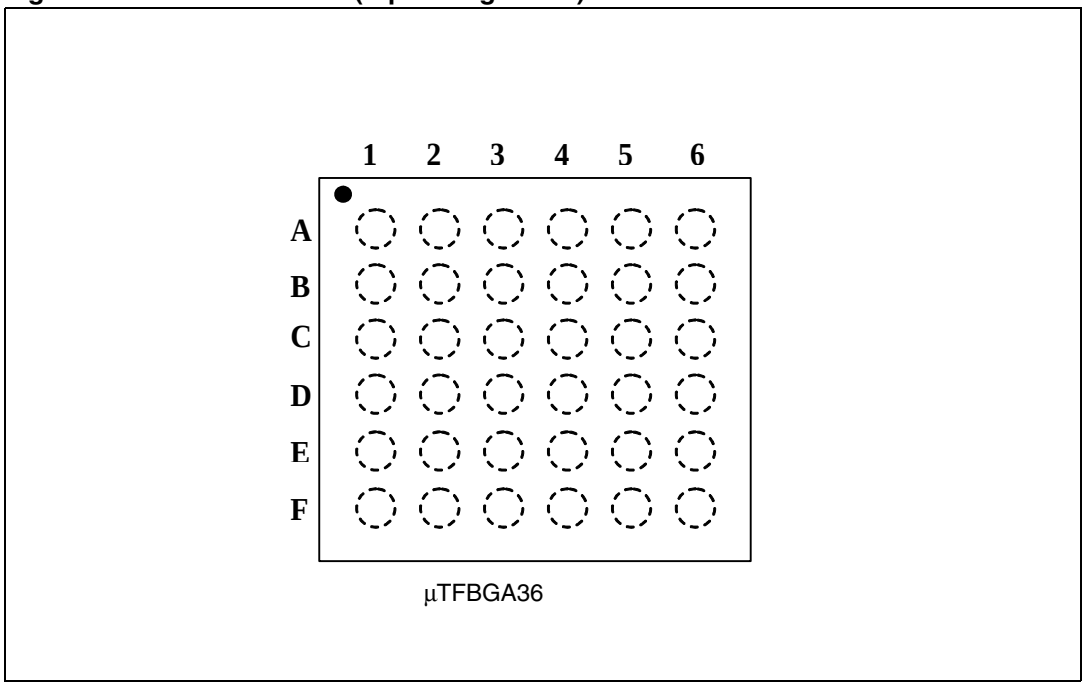


Table 2. Pin mapping

	1	2	3	4	5	6
A	VCCA	GND	IN1	CD	GND	VCCB1
B	CMD.h	CMD-dir	IN2	1CMD	1DAT0	2DAT0
C	DAT0.h	DAT0-dir	GND	2CMD	1DAT1	2DAT1
D	DAT1.h	DAT123-dir	GND	GND	1DAT2	2DAT2
E	DAT2.h	CLK-f	2CLK	1CLK	1DAT3	2DAT3
F	DAT3.h	CLK-h	MS_Insert	MS_InsertB 1	GND	VCCB2

Note: It is required that V_{CC} supply and ground pins are in close proximity, so as to allow for easy capacitive coupling in application.

2.2 Pin description

Table 3. Pin description

Pin	Type	Side	Symbol	Name and function
A1	-	A	V_{CCA}	A-side power supply
A2	-	-	GND	Ground (0 V)
A3	I	A	IN1	Output enable pin. Functions together with IN2 pin. Refer to truth table for more information on the settings
A4	-	A	CD	Card detect pin with 100 kΩ internal pull-up resistor on the A-side
A5	-	-	GND	Ground (0 V)
A6	-	B1	V_{CCB1}	B1-side power supply
B1	I/O	A	CMD.h	Command pin for A-side
B2	I	A	CMD-dir	Command direction pin HIGH => CMD.h input, nCMD output LOW => CMD.h output, nCMD input
B3	I	A	IN2	Output enable pin. Functions together with IN1 pin. Refer to truth table for more information on the settings
B4	I/O	B1	1CMD	Command pin for B1-side
B5	I/O	B1	1DAT0	Data0 pin for B1-side
B6	I/O	B2	2DAT0	Data0 pin for B2-side
C1	I/O	A	DAT0.h	Data0 pin for A-side
C2	I	A	DAT0-dir	Data direction pin for DAT0 HIGH => DAT0.h input, nDAT0 output LOW => DAT0.h output, nDAT0 input
C3	-	-	GND	Ground (0 V)
C4	I/O	B2	2CMD	Command pin for B2-side
C5	I/O	B1	1DAT1	Data1 pin for B1-side
C6	I/O	B2	2DAT1	Data1 pin for B2-side
D1	I/O	A	DAT1.h	Data1 pin for A-side
D2	I	A	DAT123-dir	Data direction pin for DAT1-DAT3 HIGH => DAT123.h input, nDAT123 output LOW => DAT123.h output, nDAT123 input
D3	-	-	GND	Ground (0 V)
D4	-		GND	Ground (0 V)
D5	I/O	B1	1DAT2	Data2 pin for B1-side

Table 3. Pin description (continued)

Pin	Type	Side	Symbol	Name and function
D6	I/O	B2	2DAT2	Data2 pin for B2-side
E1	I/O	A	DAT2.h	Data2 pin for A-side
E2	O	A	CLK-f	Feedback clock pin on A-side
E3	O	B2	2CLK	Clock Output pin for B2-side
E4	O	B1	1CLK	Clock Output pin for B1-side
E5	I/O	B1	1DAT3	Data3 pin for B1-side
E6	I/O	B2	2DAT3	Data3 pin for B2-side
F1	I/O	A	DAT3.h	Data3 pin for A-side
F2	I	A	CLK.h	Clock input pin for A-side
F3	-	A	MS_Insert	MS_Insert pin with 100 kΩ internal pull-up resistor on A-side
F4	O	B1	MS_InsertB1	MS_Insert pin on B1-side
F5	-	-	GND	Ground (0V)
F6	-	B2	V_{CCB2}	B2-side power supply

CMD

Command pin is a bidirectional line. The host and card drivers are operating in push-pull configuration.

DAT0-3

All data lines are bi-directional lines. Host and card drivers operate in push-pull mode.

CLK

Clock is a host to card signal. CLK operates in push-pull mode.

Feedback (return) clock is a feedback clock signal from level shifter to the host for controlling delays.

CD

Card detect with internal pull up resistor. Pin will be pulled to V_{CCA} when it is in high state.

IN1, IN2

Selection pins. When IN1 and IN2 are set to disabled state, all the data bus will be in high-impedance. When enabled, all the data bus will be working as a level translator between port A and port Bn (refer to the truth table for possible pin configuration).

3 Logic diagram

Figure 2. ST6G3240 logic block diagram

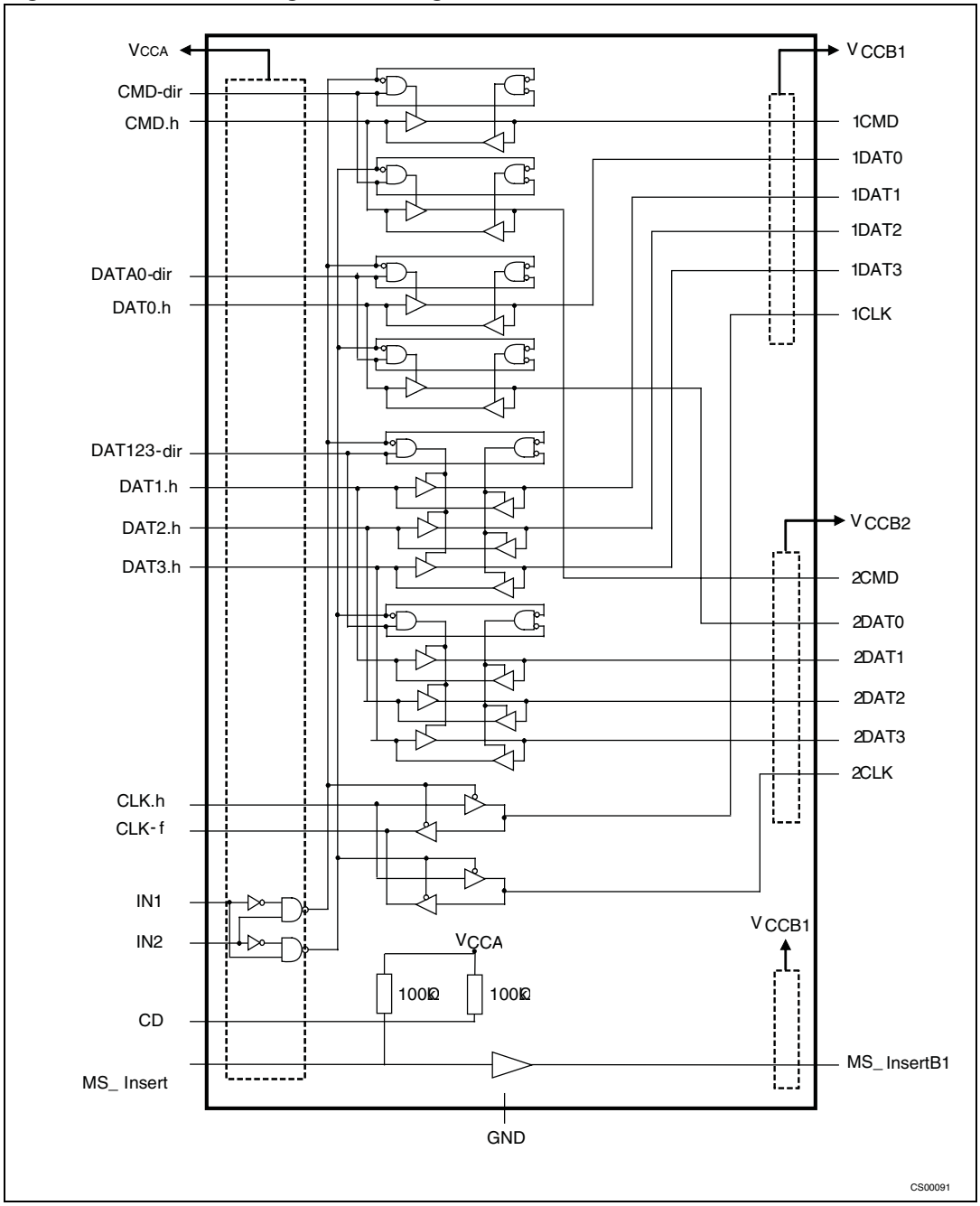


Figure 3. Input and output equivalent circuit

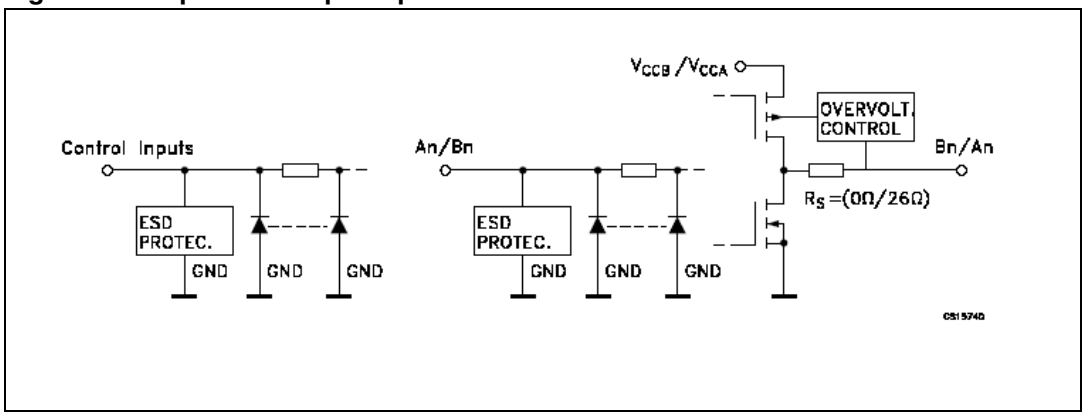


Table 4. Truth table

IN1	IN2	CMD-dir CMD.h	DAT0-dir DAT0.h	DAT123-dir DAT1.h DAT2.h DAT3.h	CLK.h CLK-f.h	1CMD 1DAT0 1DAT1 1DAT2 1DAT3 1CLK	2CMD 2DAT0 2DAT1 2DAT2 2DAT3 2CLK
H	H	H-Z	H-Z	H-Z	H-Z	H-Z	H-Z
L	H	Active	Active	Active	Active	Active	H-Z
H	L	Active	Active	Active	Active	H-Z	Active
L	L	H-Z	H-Z	H-Z	H-Z	H-Z	H-Z

H - Z: high impedance

Table 5. MS_Insert truth table

MS_Insert (referenced to V_{CCA})	MS_InsertB1 (referenced to V_{CCB1})
H	H
L	L

4 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltage	-0.5 to 4.6	V
V_{CCB1}	Supply voltage	-0.5 to 4.6	V
V_{CCB2}	Supply voltage	-0.5 to 4.6	V
V_I	DC input voltage	-0.5 to 4.6	V
$V_{I/OA}$	DC I/O voltage (output disabled)	-0.5 to 4.6	V
$V_{I/OBn}$	DC I/O voltage (output disabled)	-0.5 to 4.6	V
V_{OA}	DC output voltage	-0.5 to V_{CCA} +0.5	V
V_{OBn}	DC output voltage	-0.5 to V_{CCBn} +0.5	V
I_{IK}	DC input diode current	- 20	mA
I_{OK}	DC output diode current	- 50	mA
I_{OA}	DC output current	± 50	mA
I_{OBn}	DC output current	± 50	mA
I_{CCA}	DC V_{CCA} or ground current	± 100	mA
I_{CCBn}	DC V_{CCBn} or ground current	± 100	mA
P_D	Power dissipation at T_A = 70 ºC (1)	400	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec)	260	°C

1. Derate above 70ºC by 18.5 mW/C

Table 7. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltage	1.4 to 3.6	V
V_{CCB1}	Supply voltage	1.4 to 3.6	V
V_{CCB2}	Supply voltage	1.4 to 3.6	V
V_I	Input voltage (/IN1, /IN2, CMD-dir, DAT0-dir, DAT123-dir)	0 to V_{CCA}	V
$V_{I/OA}$	I/O voltage	0 to V_{CCA}	V
$V_{I/OBn}$	I/O voltage	0 to V_{CCBn}	V

Table 7. Recommended operating conditions (continued)

Symbol	Parameter	Value	Unit
T_{op}	Operating temperature	-40 to 85	°C
dt/dv	Input rise and fall time	0 to 10	ns/V

5 Electrical characteristics

Table 8. DC specifications for V_{CCA}

Symbol	Parameter	Test conditions			Value				Unit
		V_{CCA} (V)	V_{CCB} (V)		T_A = 25 °C		-40 to 85 °C		
					Min	Max	Min	Max	
V_{IH}	High level input voltage	1.4 –1.95	1.4 –3.6		0.65 V_{CCA}		0.65 V_{CCA}		V
		1.95 – 2.7			1.7		1.7		
		2.7 – 3.6			2.0		2.0		
V_{IL}	Low level input voltage	1.4 – 1.95	1.4 – 3.6			0.35 V_{CCA}		0.35 V_{CCA}	V
		1.95 – 2.7				0.7		0.7	
		2.7 – 3.6				0.8		0.8	
V_{OH}	High level output voltage	1.4 – 3.6	1.4 – 3.6	I_{OH} = -100 µA	V_{CCA}-0.1		V_{CCA}-0.1		V
		1.4		I_{OH} = -1 mA	1.20		1.20		
		1.65		I_{OH} = -2 mA	1.40		1.40		
		2.7		I_{OH} = -4 mA	2.30		2.30		
		3		I_{OH} = -8 mA	2.45		2.45		
		3.6		I_{OH} = -8 mA	3.05		3.05		
V_{OL}	Low level output voltage	1.4 – 3.6	1.4 – 3.6	I_{OL} = 100µA		0.10		0.10	V
		1.4		I_{OL} = 1 mA		0.20		0.20	
		1.65		I_{OL} = 2 mA		0.25		0.25	
		2.7		I_{OL} = 4 mA		0.40		0.40	
		3		I_{OL} = 8 mA		0.55		0.55	
		3.6		I_{OL} = 8 mA		0.55		0.55	
I_{IA}	Input leakage current per input channel	1.4 – 3.6	1.4 – 3.6	V_{IA} = V_{CCA} or GND		±0.5		±5	µA
I_{DIR}	Input leakage current per control input (DIR)	1.4 – 3.6	1.4 – 3.6	V_{DIR} = V_{CCA} or GND		±0.1		±2	µA

Table 8. DC specifications for V_{CCA} (continued)

Symbol	Parameter	Test conditions			Value				Unit
		V_{CCA} (V)	V_{CCB} (V)		T_A = 25 °C		-40 to 85 °C		
					Min	Max	Min	Max	
I_{OZA}	High impedance output leakage current	1.4-3.6	1.4 – 3.6	V_{IA} = GND to 3.6 V VIBn = GND to 3.6 V IN1, IN2 = V_{CCA} or IN1, IN2 = GND		±1.0		±10	µA
I_{OFF}	Power off A-side I/O leakage current	0	0	V_{IA}= 0 to 3.6 V INn = 0, DIR=0		±1.0		±10	µA
I_{CD}	CD pin input leakage current	3.6	1.4 –3.6	V_{CD} = 0		50		500	µA
I_{MS}	MS pin input leakage current	3.6	1.4 –3.6	V_{MS} = 0		50		500	µA

1 *All A-ports I/Os and control inputs are powered by V_{CCA}.*

2 *All Bn-ports I/Os are powered by V_{CCBn}.*

3 *There is no restriction on V_{CCA} or V_{CCBn}, either one can be greater than the other.*

Table 9. DC specification for V_{CCBn}

Symbol	Parameter	Test conditions			Value				Unit
		V_{CCA} (V)	V_{CCBn} (V)		T_A = 25 °C		-40 to 85 °C		
					Min	Max	Min	Max	
V_{IH}	High level input voltage	1.4 – 3.6	1.4 – 1.95		0.65 V_{CCBn}		0.65 V_{CCBn}		V
			1.95 – 2.7		1.7		1.7		
			2.7 – 3.6		2.0		2.0		
V_{IL}	Low level input voltage	1.4 – 3.6	1.4 – 1.95			0.35 V_{CCBn}		0.35 V_{CCBn}	V
			1.95 – 2.7			0.7		0.7	
			2.7 – 3.6			0.8		0.8	
V_{OH}	High level output voltage	1.4 – 3.6	1.4 – 3.6	I_{OH} = -100 µA	V_{CCBn}- 0.1		V_{CCBn}- 0.1		V
			1.4	I_{OH} = -1 mA	1.10		1.10		
			1.65	I_{OH} = -2 mA	1.20		1.20		
			2.7	I_{OH} = -4 mA	2.20		2.20		
			3.0	I_{OH} = -8 mA	2.30		2.30		
			3.6	I_{OH} = -8 mA	3.00		3.00		
V_{OL}	Low level output voltage	1.4 – 3.6	1.4 – 3.6	I_{OL} = 100 µA		0.20		0.20	V
			1.4	I_{OL} = 1 mA		0.35		0.35	
			1.65	I_{OL} = 2 mA		0.45		0.45	
			2.7	I_{OL} = 4 mA		0.55		0.55	
			3.0	I_{OL} = 8 mA		0.70		0.70	
			3.6	I_{OL} = 8 mA		0.70		0.70	
I_{IBn}	Input leakage current per input channel	1.4 – 3.6	1.4 – 3.6	V_{IBn} = V_{CCBn} or GND		±0.5		±5	µA
I_{OZBn}	High impedance output leakage current	3.6	3.6	V_{IA} = GND to 3.6 V V_{IBn} = GND to 3.6 IN1,IN2 = V_{CCA} or IN1,IN2 = GND		±1.0		±10	µA
I_{OFF}	Power off B-side I/O leakage current	0	0	V_{IBn}= 0 to 3.6 V INn= 0, DIR =0		±1.0		±10	µA

Table 10. DC quiescent current

Symbol	Parameter	Test conditions				Value				Unit
		V_{CCA} (V)	V_{CCB1} (V)	V_{CCB2} (V)		T_A = 25 °C		-40 to 85 °C		
						Min	Max	Min	Max	
I_{CCA}	Quiescent supply current for A-side	1.4 – 3.6	1.4 – 3.6	1.4 – 3.6	$V_{IA} = V_{CCA}$ or GND $V_{IBn} = V_{CCBn}$ or GND $V_{CD} = V_{MS} = V_{CCA}$		1		5	µA
		1.4 – 3.6	0	1.4 – 3.6			1		5	
		1.4 – 3.6	1.4-3.6	0			1		5	
		1.4 – 3.6	0	0			1		5	
I_{CCBn}	Quiescent supply current for Bn-side	1.4 – 3.6	1.4 – 3.6	1.4 – 3.6	$V_{IA} = V_{CCA}$ or GND $V_{IBn} = V_{CCBn}$ or GND $V_{CD} = V_{MS} = V_{CCA}$		1		5	µA
I_{CCAZ}	High impedence quiescent supply current for A-side	1.4 – 3.6	1.4 – 3.6	1.4 – 3.6	IN1 = GND/V_{CCA} IN2 = GND/V_{CCA}		0.2		1	µA
		1.4 – 3.6	1.4 – 3.6	1.4 – 3.6	IN1 = V_{CCA} and IN2 = GND		0.5		2	
		1.4 – 3.6	1.4 – 3.6	1.4 – 3.6	IN1 = GND and IN2 = V_{CCA}		0.5		2	

Table 11. AC electrical characteristics (f = 10 MHz, 50% duty cycle[1])
V_{CCA} = 1.5 V ±0.1 V

Parameter		From (input)	To (output)	V_{CCBn}=1.8 V ± 0.15 V		V_{CCBn}= 2.5 V ± 0.2 V		V_{CCBn} = 3.0 ± 0.3 V		V_{CCBn}=3.3 V ± 0.3 V		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLHAB}, t_{PHLAB}	Propagation delay time from A to B (C_L= 15 pF, R_L= 2 kΩ)	CMD.h	nCMD		9		6		5.5		5.5	ns
		CLK.h	nCLK		9		6		5.5		5.5	
		CLK.h	CLK-f		18		12		11		11	
		DATx.h	nDATx		9		6		5.5		5.5	
t_{PLHBA}, t_{PHLBA}	Propagation delay time from B to A (C_L = 7 pF, R_L = 2 kΩ)	nCMD	CMD.h		9		9		9		9	ns
		nDATx	DATx.h		9		9		9		9	
t_{PZL}, t_{PZH}	Output enable time (C_L =7 pF, R_L = 2 kΩ)	INn	A		22		22		22		22	ns
	Output enable time (C_L = 15 pF, R_L = 2 kΩ)	INn	Bn		22		22		22		22	
t_{PLZ}, t_{PHZ}	Output disable time (C_L=7 pF, R_L= 2 kΩ)	INn	A		33		33		33		33	ns
	Output disable time (C_L= 15 pF, R_L= 2 kΩ)	INn	Bn		33		33		33		33	
$t_{DIR, enable}$		DIR	A		8		8		8		8	ns
		DIR	B		9		9		9		9	
$t_{DIR, disable}$		DIR	A		7		7		7		7	ns
		DIR	B		8		8		8		8	
t_{OSLH},t_{OSHL}	Output to output skew time[2]				1		1		1		1	ns
t_{CDLH},t_{CDHL}	Clock and data skew time				1		1		1		1	ns
f_{max}	Clock	A	Bn		52		52		52		52	MHz
		Bn	A		52		52		52		52	
	Data	A	Bn		104		104		104		104	Mbps
		Bn	A		104		104		104		104	

1. Refer to figure 4.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either High or Low (t_{OSLH} = | t_{PLHm} - t_{PLHn} |, t_{OSHL} = | t_{PHLm} – t_{PHLn} |)

Table 12. V_{CCA} = 1.8 V ± 0.15 V

Parameter		From (input)	To (output)	V_{CCBn} = 1.8 V ± 0.15 V		V_{CCBn}= 2.5V ± 0.2V		V_{CCBn}= 3.0 ± 0.3 V		V_{CCBn} = 3.3 V ± 0.3V		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLHAB}, t_{PHLAB}	Propagation delay time from A to B (C_L= 15 pF, R_L= 2 kΩ)	CMD.h	nCMD		8.5		5.5		5		5	ns
		CLK.h	nCLK		8.5		5.5		5		5	
		CLK.h	CLK-f		17		11		10		10	
		DATx.h	nDATx		8.5		5.5		5		5	
t_{PLHBA}, t_{PHLBA}	Propagation delay time from B to A (C_L=7 pF, R_L= 2 kΩ)	nCMD	CMD.h		7		7		7		7	ns
		nDATx	DATx.h		7		7		7		7	
t_{PZL}, t_{PZH}	Output enable time (C_L=7pF, R_L=2 kΩ)	INn	A		15		15		15		15	ns
	Output enable time (C_L= 15 pF, R_L=2 kΩ)	INn	Bn		15		15		15		15	
t_{PLZ}, t_{PHZ}	Output disable time (C_L= 7 pF, R_L= 2 kΩ)	INn	A		22		22		22		22	ns
	Output disable time (C_L= 15 pF, R_L= 2 kΩ)	INn	Bn		22		22		22		22	
$t_{DIR, enable}$		DIR	A		7		7		7		7	ns
		DIR	B		8		8		8		8	
$t_{DIR, disable}$		DIR	A		5		5		5		5	ns
		DIR	B		6		6		6		6	
t_{OSLH},t_{OSHL}	Output to output skew time(1)				1		1		1		1	ns
t_{CDLH},t_{CDHL}	Clock and data skew time				1		1		1		1	ns
f_{max}	Clock	A	Bn		52		52		52		52	MHz
		Bn	A		52		52		52		52	
	Data	A	Bn		104		104		104		104	Mbps
		Bn	A		104		104		104		104	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = | t_{PLHm} - t_{PLHn} |, t_{OSHL} = | t_{PHLm} – t_{PHLn} |)

Table 13. V_{CCA} = 2.5 ± 0.2 V

Parameter		From (input)	To (output)	V_{CCBn}=1.8V ± 0.15V		V_{CCBn}=2.5V ± 0.2V		V_{CCBn}=3.0 ± 0.3V		V_{CCBn}=3.3V ± 0.3V		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLHAB}, t_{PHLAB}	Propagation delay time from A to B (C_L= 15 pF, R_L= 2 kΩ)	CMD.h	nCMD		7.5		5		4.5		4.5	ns
		CLK.h	nCLK		7.5		5		4.5		4.5	
		CLK.h	CLK-f		15		10		9		9	
		DATx.h	nDATx		7.5		5		4.5		4.5	
t_{PLHBA}, t_{PHLBA}	Propagation delay time from B to A (C_L= 7 pF, R_L= 2 kΩ)	nCMD	CMD.h		5		5		5		5	ns
		nDATx	DATx.h		5		5		5		5	
t_{PZL}, t_{PZH}	Output enable time (C_L= 7 pF, R_L= 2 kΩ)	INn	A		11		11		11		11	ns
	Output enable time (C_L=15 pF, R_L= 2 kΩ)	INn	Bn		11		11		11		11	
t_{PLZ}, t_{PHZ}	Output disable time (C_L=7 pF, R_L=2 kΩ)	INn	A		21		21		21		21	ns
	Output disable time (C_L= 15 pF, R_L=2 kΩ)	INn	Bn		21		21		21		21	ns
$t_{DIR, enable}$		DIR	A		5		5		5		5	ns
		DIR	B		6		6		6		6	
$t_{DIR, disable}$		DIR	A		5		5		5		5	ns
		DIR	B		6		6		6		6	
t_{OSLH},t_{OSHL}	Output to output skew time(1)				1		1		1		1	ns
t_{CDLH},t_{CDHL}	Clock and data skew time				1		1		1		1	ns
f_{max}	Clock	A	Bn		52		52		52		52	MHz
		Bn	A		52		52		52		52	
	Data	A	Bn		104		104		104		104	Mbps
		Bn	A		104		104		104		104	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = | t_{PLHm} - t_{PLHn} |, t_{OSHL} = | t_{PHLm} – t_{PHLn} |)

Table 14. V_{CCA} = 3.3 V ± 0.3 V

Parameter		From	To	V_{CCBn} = 1.8 V ± 0.15 V		V_{CCBn} = 2.5 V ± 0.2 V		V_{CCBn} = 3.0 ± 0.3 V		V_{CCBn} = 3.3 V ± 0.3 V		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLHAB}, t_{PHLAB}	Propagation delay time from A to B (C_L = 15 pF, R_L= 2 kΩ)	CMD.h	nCMD		7		4.5		4.3		4.3	ns
		CLK.h	nCLK		7		4.5		4.3		4.3	
		CLK.h	CLK-f		14		9		8.6		8.6	
		DATx.h	nDATx		7		4.5		4.3		4.3	
t_{PLHBA}, t_{PHLBA}	Propagation delay time from B to A (C_L= 7 pF, R_L= 2 kΩ)	nCMD	CMD.h		4		4		4		4	ns
		nDATx	DATx.h		4		4		4		4	
t_{PZL}, t_{PZH}	Output enable time (C_L= 7 pF, R_L= 2 kΩ)	INn	A		9		9		9		9	ns
	Output enable time (C_L = 15 pF, R_L = 2 kΩ)	INn	Bn		9		9		9		9	
t_{PLZ}, t_{PHZ}	Output disable time (C_L = 7 pF, R_L= 2 kΩ)	INn	A		20		20		20		20	ns
	Output disable time (C_L= 15 pF, R_L=2 kΩ)	INn	Bn		20		20		20		20	
$t_{DIR, enable}$		DIR	A		4		4		4		4	ns
		DIR	B		5		5		5		5	
$t_{DIR, disable}$		DIR	A		4		4		4		4	ns
		DIR	B		5		5		5		5	
t_{OSLH},t_{OSHL}	Output to output skew time(1)				1		1		1		1	ns
t_{CDLH},t_{CDHL}	Clock and data skew time				1		1		1		1	ns
f_{max}	Clock	A	Bn		52		52		52		52	MHz
		Bn	A		52		52		52		52	
	Data	A	Bn		104		104		104		104	Mbps
		Bn	A		104		104		104		104	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = | t_{PLHm} - t_{PLHn} |, t_{OSHL} = | t_{PHLm} – t_{PHLn} |)

Table 15. Output slew rate (f = 1 MHz, 50% duty cycle, C_L=15 pF on Bn-side; C_L=7 pF on A-side)

Symbol	Parameter	From	To	Test condition T_A = -40 to 85 °C V_{CCA} = 1.8 V ± 0.15V V_{CCBn} = 3.0 V ± 0.3V		Unit
				Min	Max	
t_r	Rise time	10%	90%		3.5	ns
t_f	Fall time	10%	90%		3.5	ns

Table 16. Capacitance characteristics

Symbol	Parameter	Test condition			Value					Unit
		V_{CCA} (V)	V_{CCBn} (V)		T_A = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max	
C_{INBn}	Input capacitance	Open	Open			9				pF
$C_{I/OA}$	Input/output capacitance for A-side	1.8	3.0	f = 1 MHz V_{BIAS} = 250 mV V_{PP} = 500 mV		5				pF
$C_{I/OBn}$	Input/output capacitance for Bn-side	1.8	3.0	f = 1 MHz V_{BIAS} = 250 mV V_{PP} = 500 mV		11				pF
C_{PD}	Power dissipation capacitance	2.5	3.3	f = 10 MHz		29				pF
		1.8	3.3			29				

6 Test circuit

Figure 4. Test circuit

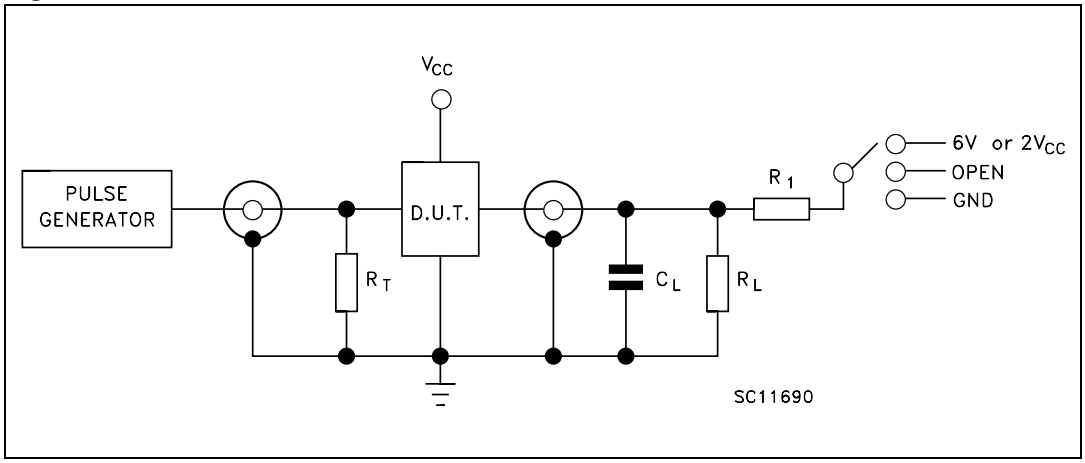


Table 17. Test circuit switches

Test	C_L (pF)		R_L/R_1 (kΩ)	Switch
	A-side	B-side		
t_{PLH}, t_{PHL}	7	15	2	Open
t_{PZL}, t_{PLZ}	7	15	2	2 V_{CC}
t_{PZH}, t_{PHZ}	7	15	2	GND

R_T is the Z_{out} of the pulse generator, typically 50Ω.

Table 18. Waveform symbol value

Symbol	V_{CC}		
	3.0 to 3.6 V	2.3 to 2.7 V	1.65 to 1.95 V
V_{IH}	V_{CC}	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_Y	V_{OH} - 0.3 V	V_{OH} - 0.15 V	V_{OH} - 0.15 V

Figure 5. Waveform - propagation delay (f = 1 MHz, 50% duty cycle)

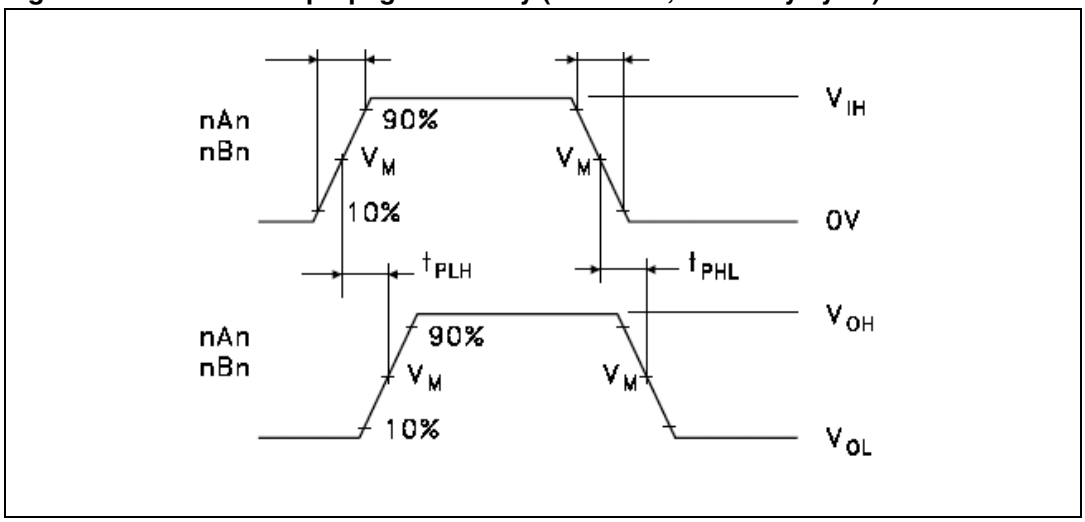


Figure 6. Waveform - output enable/disable (f = 1 MHz, 50% duty cycle)

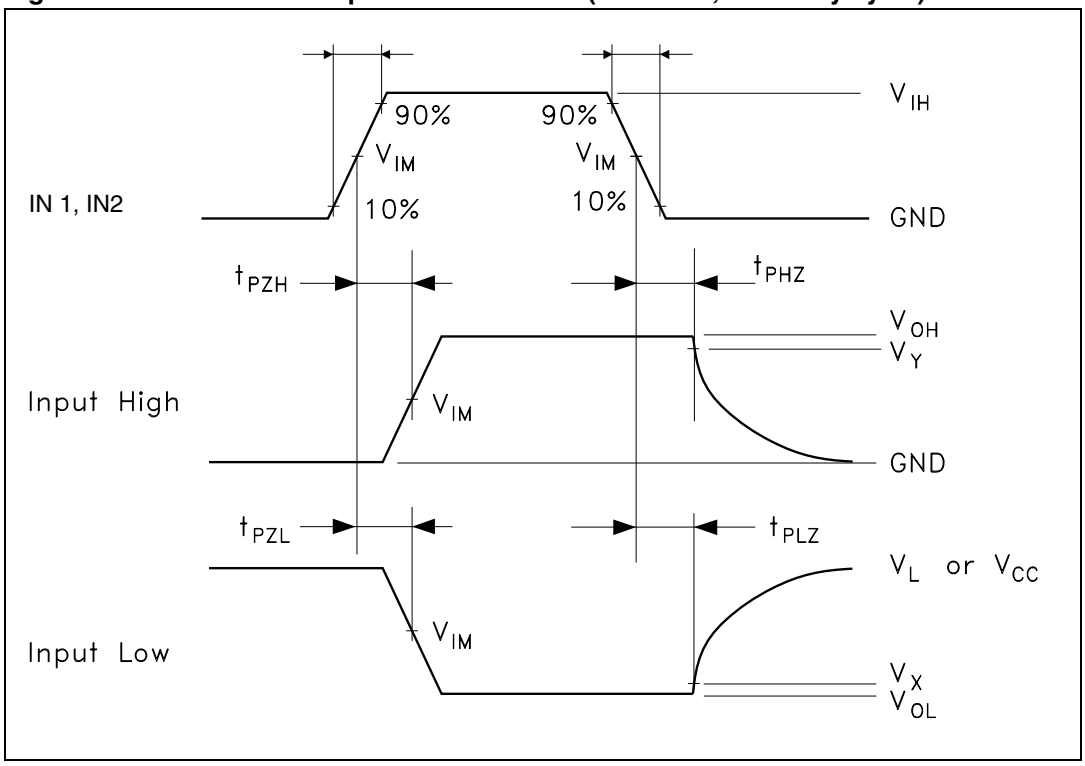
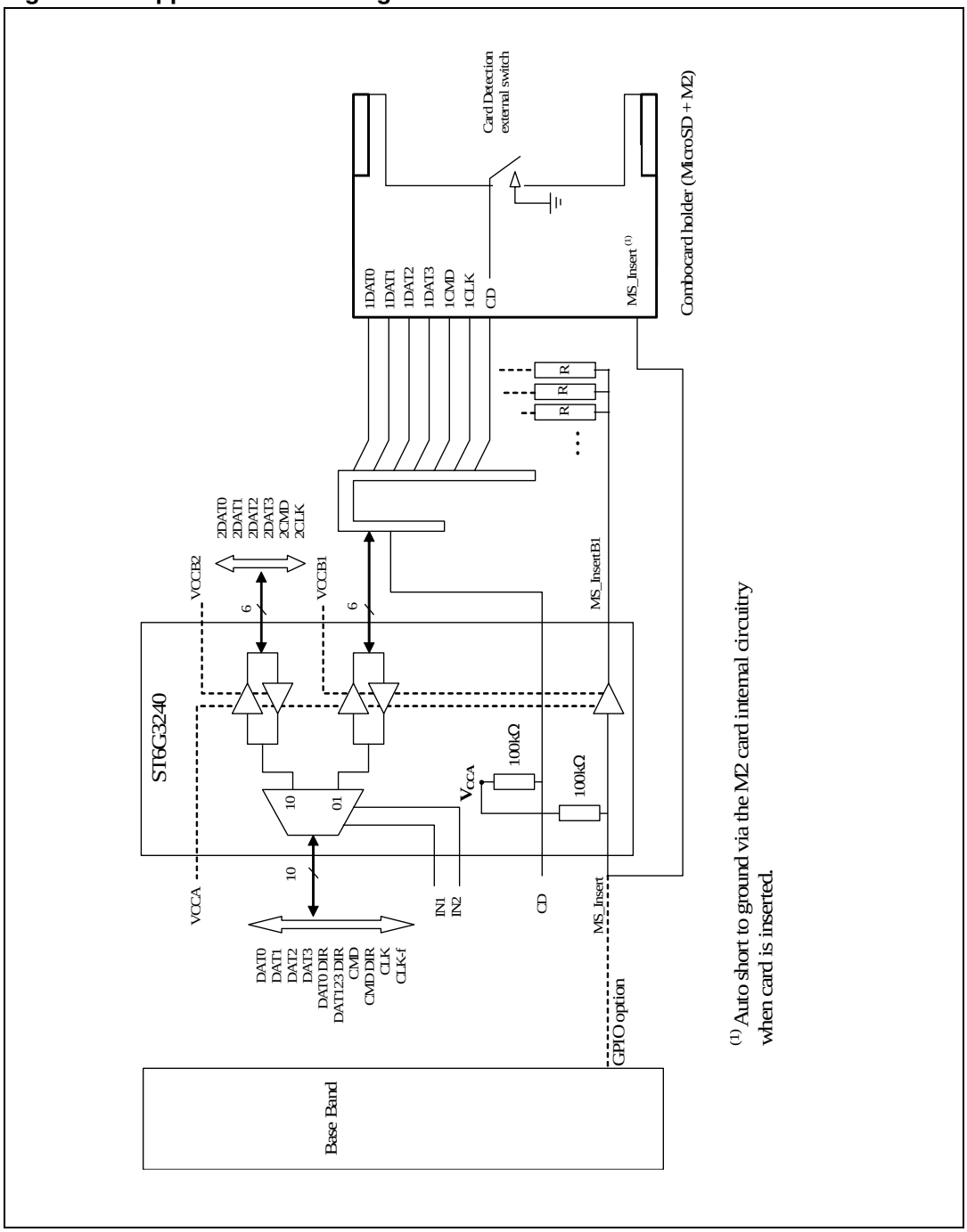


Figure 7. Application block diagram



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 8. µTFBGA package outline

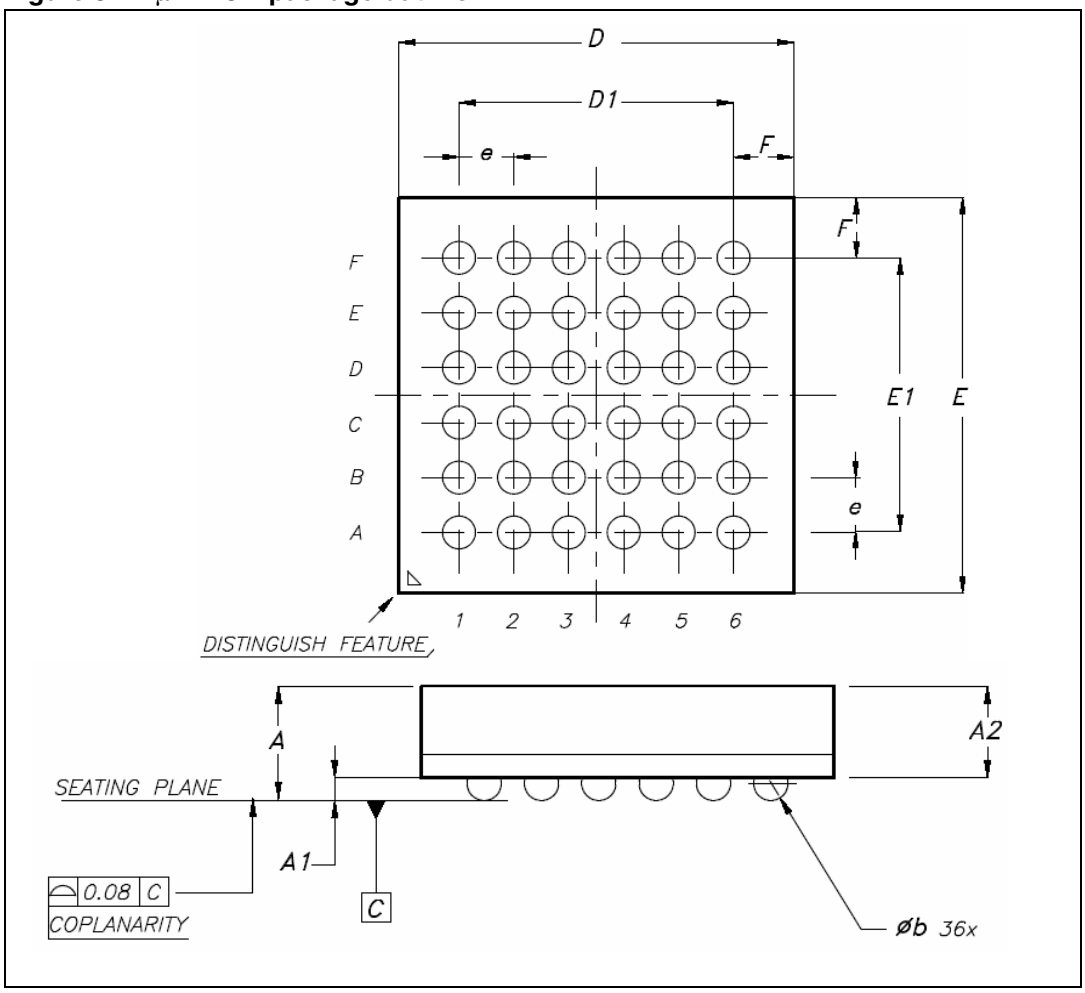


Table 19. µTFBGA 36 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	1	1.1	1.16
A1			0.25
A2	0.78		0.86
b	0.25	0.30	0.35
D	3.50	3.60	3.70
D1		2.50	
E	3.50	3.60	3.70
E1		2.50	
e		0.50	
F		0.55	

Figure 9. Recommended footprint

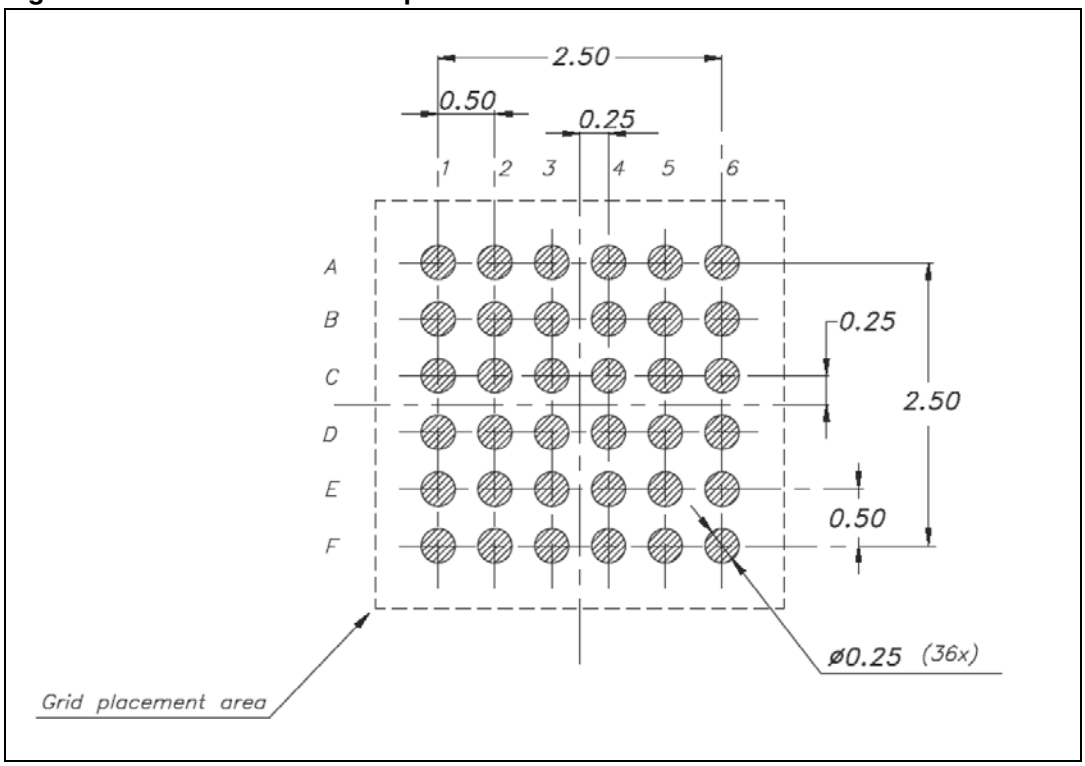


Figure 10. Carrier tape information

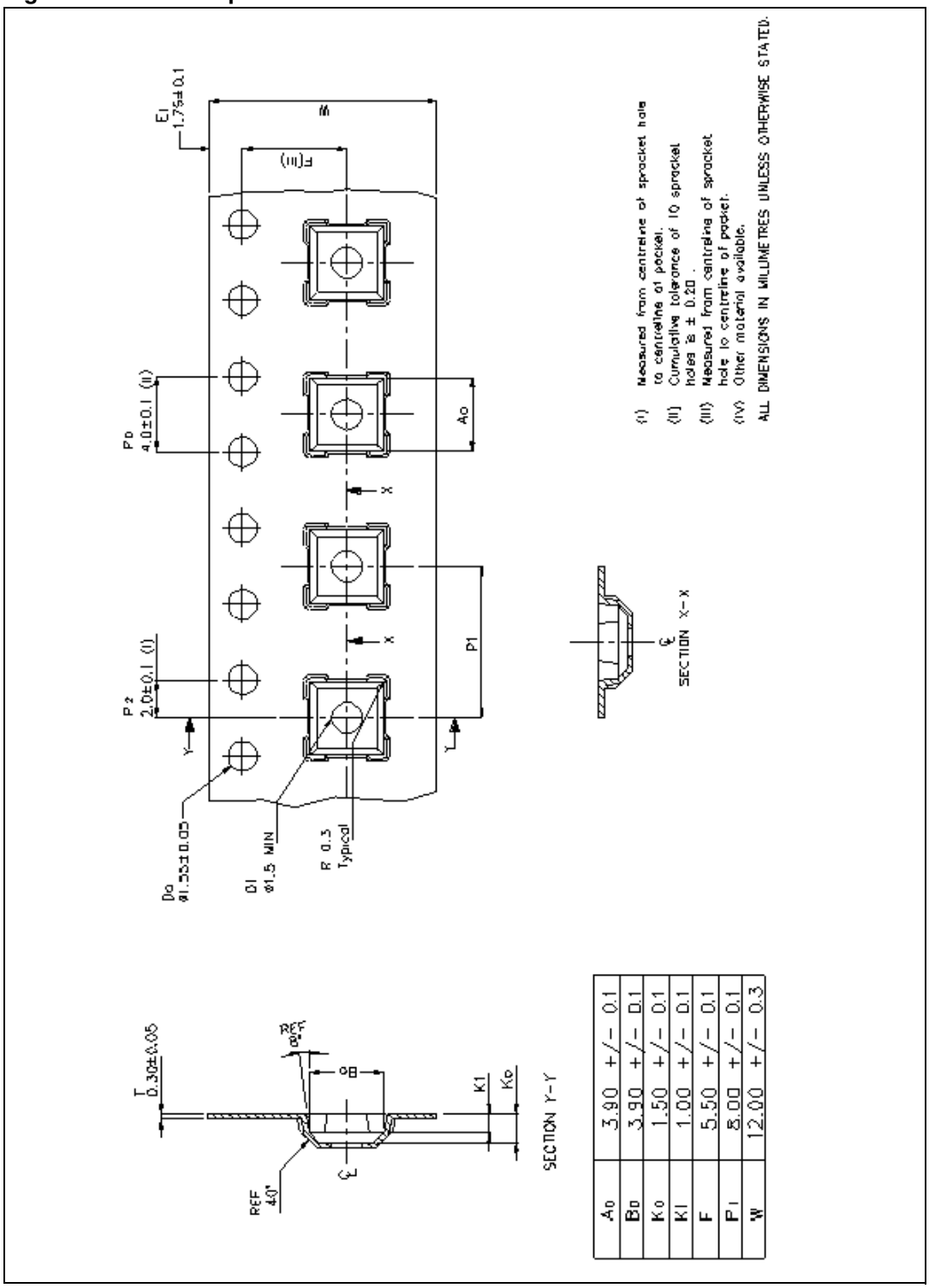


Figure 11. Reel dimensions

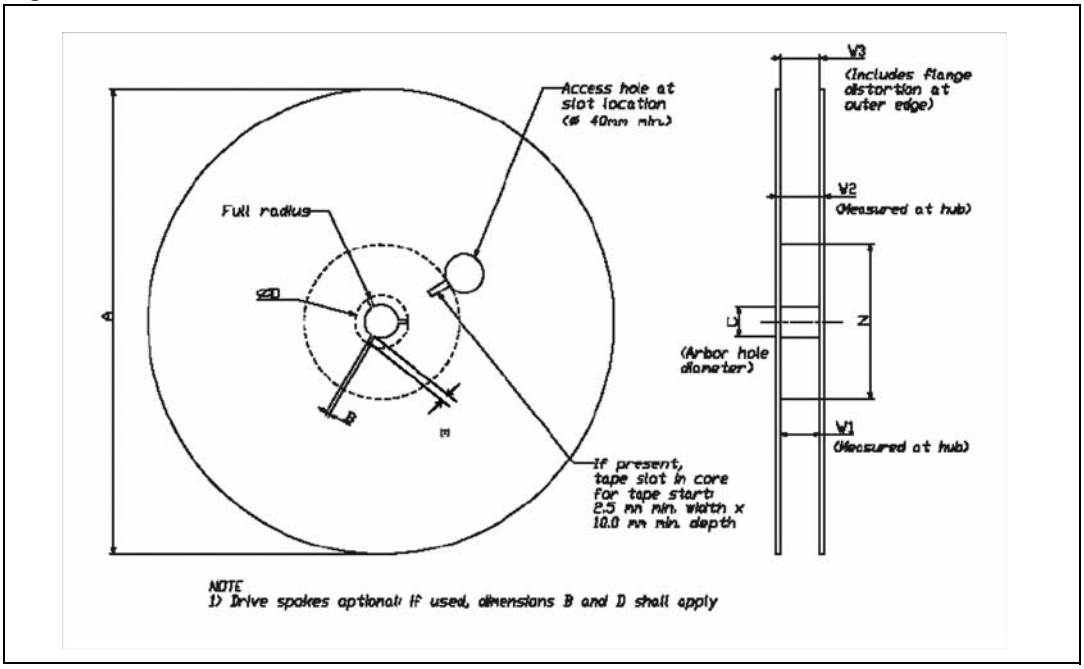
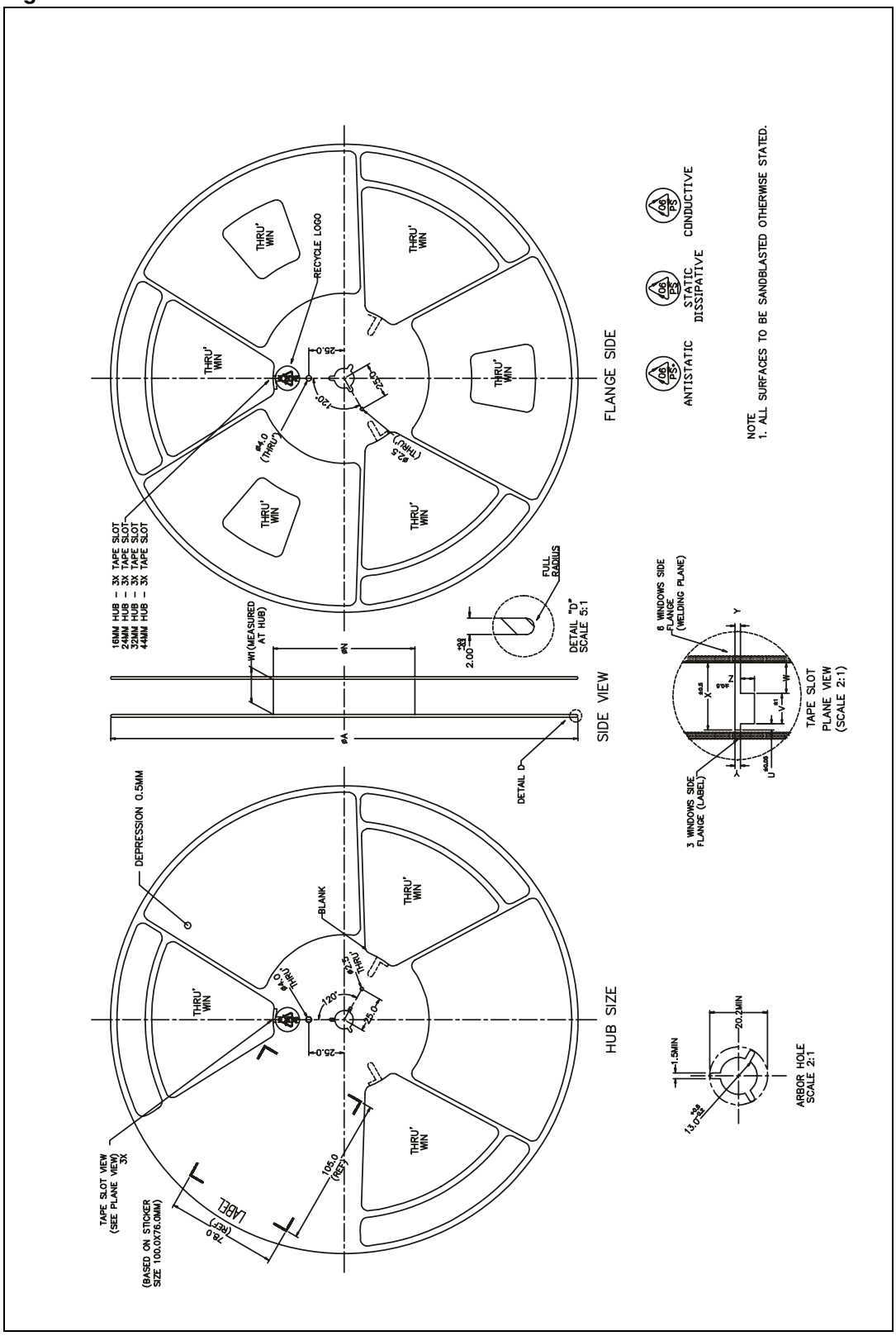


Table 20. Reel dimensions

Tape width	N	W1	W2 max	C
12	178 ± 5 mm	12.4 (+2,-0)	18.4	13 ± 0.25

Figure 12. Reel information



8 Revision history

Table 21. Document revision history

Date	Revision	Changes
27-Mar-2008	1	Initial release.
18-Apr-2008	2	Minor text changes. Modified f_{max} values in *Table 11*, *Table 12*, *Table 13* and *Table 14*.

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