MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order Number: MPC9990/D
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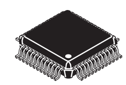
Product Preview

Low Voltage PLL Clock Driver

MPC9990

LOW VOLTAGE DIFFERENTIAL PECL–HSTL PLL CLOCK DRIVER



FA SUFFIX
48–LEAD LQFP PACKAGE
CASE 932

The MPC9990 is a low voltage PLL clock driver designed for high speed clock generation and distribution in high performance computer, workstation and server applications. The clock driver accepts a LVPECL compatible clock signal and provides 10 low skew, differential HSTL[1] compatible outputs, one HSTL compatible output for system synchronization purposes and one HSTL compatible PLL feedback output. The device operates from a dual voltage supply: 3.3 V for the core logic and 1.8 V for the HSTL outputs. The fully integrated PLL supports an input frequency range of 75 to 287.5 MHz. The output frequencies are configurable.

- Supports high performance HSTL clock distribution systems
- Compatible to IA64 processor systems
- Fully Integrated PLL, differential design
- Core logic operates from 3.3 V power supply
- HSTL outputs operate from a 1.8 V supply
- Programmable frequency by output bank
- 10 HSTL compatible outputs (two banks)
- HSTL compatible PLL feedback output
- HSTL compatible sychronization output (QSYNC)
- Max. skew of 80 ps within output bank
- Zero–delay capability: max. SPO (tpd) window of 150 ps
- LVPECL compatible clock input, LVCMOS compatible control inputs
- Temperature range of 0 to +70°C

The MPC9990 provides output clock frequencies required for high–performance computer system optimization. The device drives up to 10 differential clock loads within the frequency range of 75 to 287.5 MHz. The 10 outputs are organized in 2 banks of 3 and 7 differential outputs. In the standard configuration the QFB output pair is connected to the FB input pair closing the PLL loop and enabling zero delay operation from the CLK input to the outputs. Bank B outputs are frequency and phase aligned to the CLK input, providing exact copies of the high–speed input signal. Bank A outputs are configured to operate at slower speeds driving the system bus devices. The output frequency ratio of bank A to bank B is adjustable (for available ratios, see “MPC9990 Application: CPU to System Bus Frequency Ratios” on page 2) for system optimization. In a computer application, bank B outputs generate the clock signals for the devices operating at the CPU frequency, while Bank A outputs are configured to drive the clock signals for the devices running at lower speeds (system clock). Four individual frequency ratios are available, providing a high degree of flexibility. The frequency ratios between CPU clock and system clock provided by the MPC9990 are listed in the table “Output configuration” on page 4.

The QSYNC output functionality is designed for system synchronization purpose. QSYNC is asserted at coincident rising edges of CPU (bank B and QFB signal) and slower system clock (bank A) outputs (see “QSYNC Phase Relation Diagram” on page 4), providing baseline timing in systems with fractional clocks. The QSYNC output is asserted for one QFB high pulse, centered on the rising QFB output.

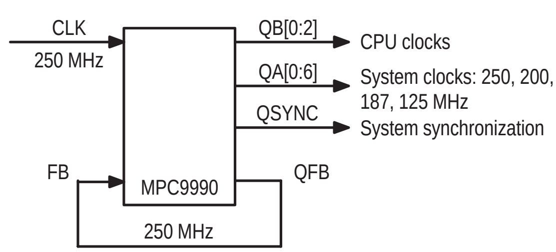


Figure 1. MPC9990 Application Example

1. In order to minimize output–to–output skew, HSTL outputs of the MPC9990 are generated with an open emitter architecture. For output termination, see ”HSTL Output Termination and AC Test Reference” on page 5.

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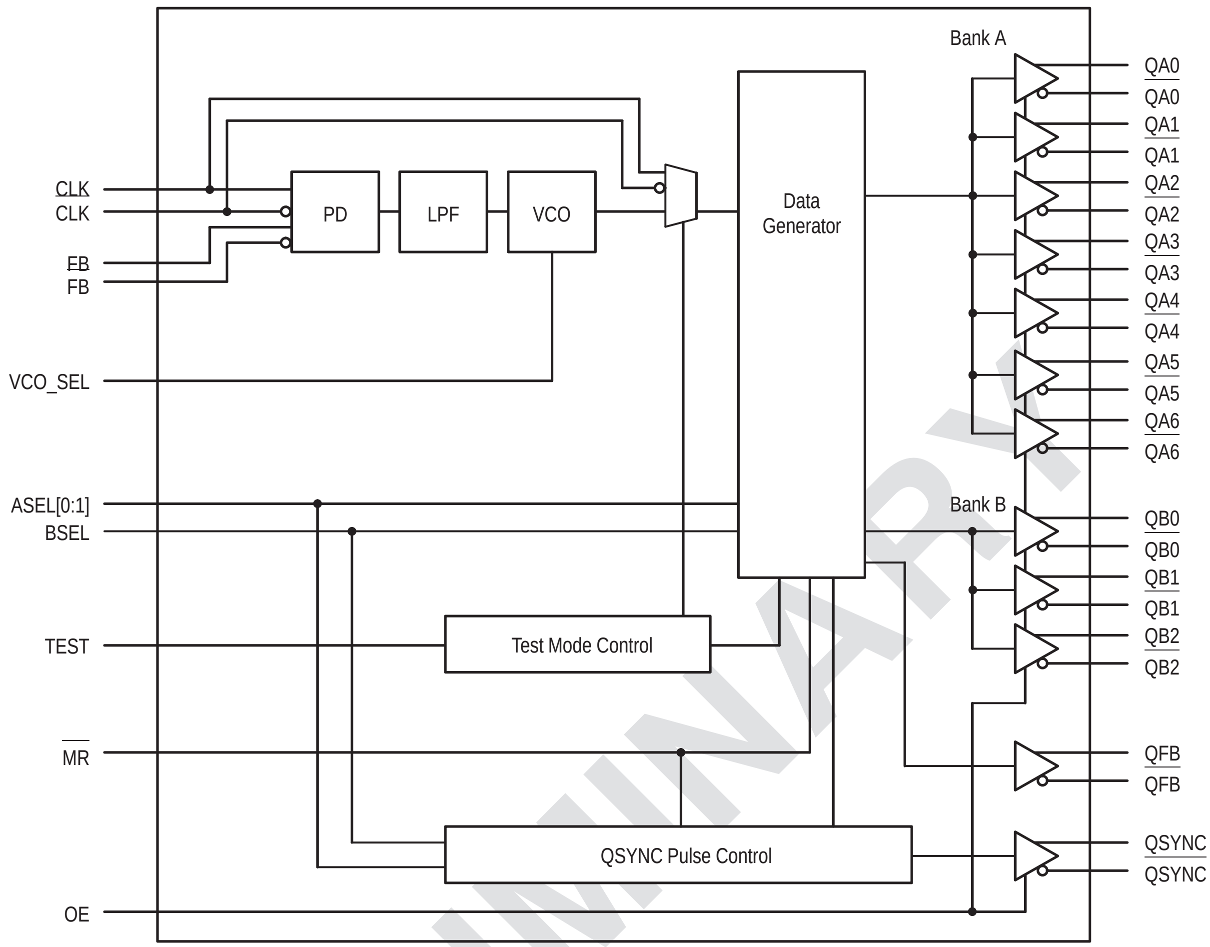


Figure 2. MPC9990 Logic Diagram

Table 1: MPC9990 Application: CPU to System Bus Frequency Ratios

QA to QB frequency ratio	1:1	1:2	3:4	4:5	
Output frequencies for CLK = 75 MHz (BSEL=1, VCO_SEL=1)					
QA output frequency	75	37.5	56.25	60	MHz
QB output frequency	75	75	75	75	MHz
Output frequencies for CLK = 100 MHz (BSEL=1, VCO_SEL=1)					
QA output frequency	100	50	75	80	MHz
QB output frequency	100	100	100	100	MHz
Output frequencies for CLK = 125 MHz (BSEL=1, VCO_SEL=1)					
QA output frequency	125	62.5	93.75	100	MHz
QB output frequency	125	125	125	125	MHz
Output frequencies for CLK = 150 MHz (BSEL=1, VCO_SEL=0)					
QA output frequency	150	75	112.5	120	MHz
QB output frequency	150	150	150	150	MHz
Output frequencies for CLK = 200 MHz (BSEL=1, VCO_SEL=0)					
QA output frequency	200	100	150	160	MHz
QB output frequency	200	200	200	200	MHz
Output frequencies for CLK = 250 MHz (BSEL=1 VCO_SEL=0)					
QA output frequency	250	125	187.5	200	MHz
QB output frequency	250	250	250	250	MHz

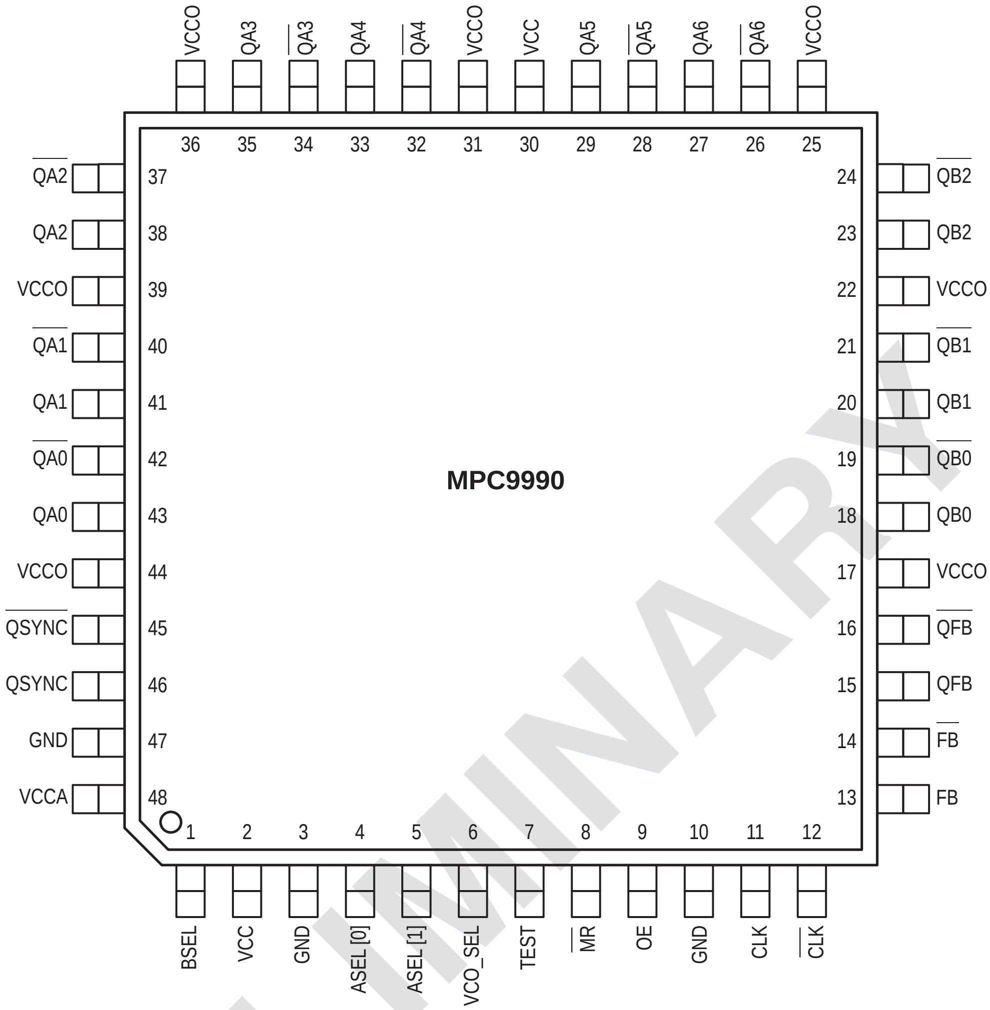


Figure 3. 48–Lead Package Pinout (Top View)

Table 2: Pin configuration

Pin	I/O	Type	Internal resistor	Description
CLK, $\overline{CLK}$	Input	LVPECL	CLK: pull-down, $\overline{CLK}$: pull-up	Differential clock frequency input
FB, $\overline{FB}$	Input	HSTLL	FB: pull-down, $\overline{FB}$: pull-up	Differential feedback input
QAn, $\overline{QAn}$	Output	HSTL		Bank A outputs
QBn, $\overline{QBn}$	Output	HSTL		Bank B outputs
QSYNC, $\overline{QSYNC}$	Output	HSTL		Synchronization output
QFB, $\overline{QFB}$	Output	HSTL		Differential feedback output
VCO_SEL	Input	LVCMOS	pull-down	Selection of operating frequency range
ASEL[0:1]	Input	LVCMOS	pull-down	Selection of bank A output frequency
BSEL	Input	LVCMOS	pull-down	Selection of bank B output frequency
TEST	Input	LVCMOS	pull-down	Selection of PLL operation or TEST mode (PLL bypass)
$\overline{MR}$	Input	LVCMOS	pull-up	Master reset. Assertion of master reset required on startup
OE	Input	LVCMOS	pull-up	Output enable
V_{CCA}		Power supply		Analog power supply, typical 3.3 V
V_{CC}		Power supply		Core power supply, typical 3.3 V
V_{CCO}		Power supply		Output power supply, typical 1.8 V
GND		Ground		Output, analog and core logic ground, 0V (VEE)

Table 3: Output Frequency Relationship for an Example Configuration

ASEL[0]	ASEL[1]	BSEL	f QAn	f QBn	f QFB	QSYNC
0	0	0	CLK	CLK	CLK	L
0	1	0	CLK ÷ 2	CLK ÷ 2	CLK	enabled
1	0	0	CLK x 3 ÷ 4	CLK x 3 ÷ 4	CLK	enabled
1	1	0	CLK x 4 ÷ 5	CLK x 4 ÷ 5	CLK	enabled
0	0	1	CLK	CLK	CLK	L
0	1	1	CLK ÷ 2	CLK	CLK	enabled
1	0	1	CLK x 3 ÷ 4	CLK	CLK	enabled
1	1	1	CLK x 4 ÷ 5	CLK	CLK	enabled

Table 4: Function Table (Controls)

Control Pin	0	1
TEST	PLL enabled	PLL bypassed (Static test mode)
$\overline{MR}$	Reset (Internal logic and PLL)	Normal operation mode
OE	Outputs disabled (Q_X = L, $\overline{Q_X}$ = H), except QFB, $\overline{QFB}$	Outputs enabled
VCO_SEL	High frequency operation (VCO frequency range from 600 to 1150 MHz)	Low frequency operation (VCO frequency range from 300 to 575 MHz)

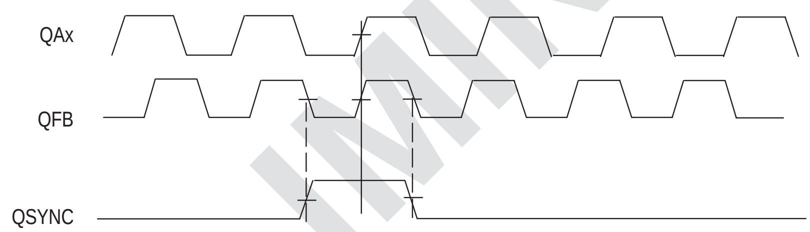


Figure 4. QSYNC Phase Relation Diagram

The MPC9990 has a system synchronization pulse output (QSYNC). The QSYNC pulse output is synchronous to the feedback clock signal (QFB) and activated when both QFB and bank A outputs are programmed to run at a frequency ratio other than 1:1. In the case of a 1:1 frequency ratio (ASEL[] = 00), QSYNC remains low. QSYNC output transitions occur prior coincident rising edges of QFB and bank A. The pulse width of the QSYNC pulse is equal to the period of the feedback clock frequency (QFB). The QSYNC pulse is asserted at the last falling edge of QFB prior to the coincident edge event, and deasserted at the next falling edge of QFB (see "QSYNC Phase Relation Diagram"). If BSEL = 1 and the PLL is frequency and phase-locked, QSYNC pulses occur on coincident edges between the QA-bank and QB-bank outputs (offset by feedback delay) due to the fixed phase relation between CLK, QFB and QB-bank outputs.

Table 5: ABSOLUTE MAXIMUM RATINGS*

Symbol	Characteristics	Min	Max	Units	Condition
V_{CCA}	Analog power supply	–0.5	3.6	V	
V_{CC}	Core power supply	–0.5	3.6	V	
V_{CCO}	Output power supply	–0.5	3.6	V	
V_{IN}	Input voltage	–0.5	V_{CC} + 0.3	V	
I_{IN}	Input current	–1.0	1.0	mA	DC
I_{OUT}	Output current	–50	50	mA	DC
T_S	Storage temperature	–50	150	°C	

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute–maximum–rated conditions is not implied.

Table 6: DC CHARACTERISTICS (V_{CC} = V_{CCA} = 3.3 V ±5%, V_{CCO} = 1.7 to 2.1V, T_A = 0° to 70°C)

Symbol	Characteristics	0 °C			25 °C			70 °C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
HSTL I/O[a]												
V_{CCO}	Output power supply	1.7	1.8	2.1	1.7	1.8	2.1	1.7	1.8	2.1		
V_{IN}	Input voltage (FB)	-0.3		1.45	-0.3		1.45	-0.3		1.45	V	Differential
V_{DIF}	Differential input voltage[b] (FB)	0.2		1.75	0.2		1.75	0.2		1.75	V	Differential
V_{CM}	Common mode input voltage[c] (FB)	0.64		0.9	0.68		0.9	0.68		1.0	V	
V_{OH}	Output high voltage	1.0	V_X+0.4	1.4	1.0	V_X+0.4	1.4	1.0	V_X+0.4	1.4	V	
V_{OL}	Output low voltage	0	V_X-0.4	0.4	0	V_X-0.4	0.4	0	V_X-0.4	0.4	V	
LVPECL I/O												
V_{CC}	Power supply voltage (core)	3.135	3.3	3.465	3.135	3.3	3.465	3.135	3.3	3.465	V	
V_{CCA}	Power supply voltage (PLL)	3.135	3.3	3.465	3.135	3.3	3.465	3.135	3.3	3.465	V	
V_{PP}	Peak-to-peak input voltage CLK, $\overline{PCLK}$	500		1000	500		1000	500		1000	mV	
V_{CMR}	Common Mode Range[d] CLK, $\overline{PCLK}$	V_{CC}-1.4		V_{CC}-0.6	V_{CC}-1.4		V_{CC}-0.6	V_{CC}-1.4		V_{CC}-0.6	V	
I_{IH}	Input high current			±150			±150			±150	µA	
I_{CC}	Power supply current (core)			400			400			400	mA	
I_{CCA}	Power supply current (PLL)		15	20		15	20		15	20	mA	
LVCMOS Inputs												
V_{IH}	Input high voltage	2		V_{CC}	2		V_{CC}	2		V_{CC}	V	
V_{IL}	Input low voltage	0		0.8	0		0.8	0		0.8	V	
I_I	Input current			±100			±100			±100	µA	

a. See “HSTL Differential Input Levels”.
b. V_{DIF} specifies the input differential voltage.
c. V_{CM} is the maximum allowable range of V_{TR} - ((V_{TR} - V_{CP})/2). V_{TR} is true input signal, V_{CP} is its complementary input signal.
d. V_{CMR} is the difference from V_{CC} and the crosspoint of the differential input signal. Normal operation is obtained when the “high” input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
e. LVPECL input level specifications will vary 1:1 with V_{CC}.

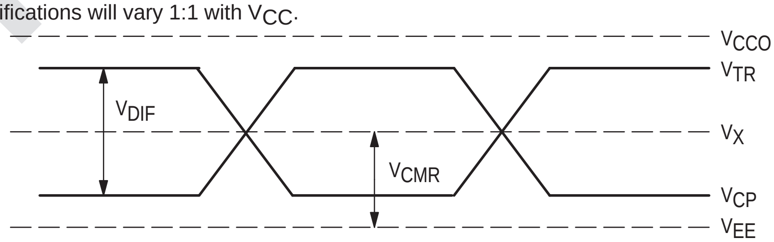


Figure 5. HSTL Differential Input Levels

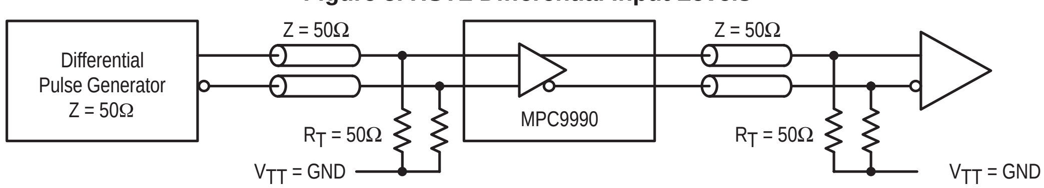


Figure 6. HSTL Output Termination and AC Test Reference

Table 7: AC CHARACTERISTICS ($V_{CCI} = V_{CCA}$ = 3.3 V ±5%, V_{CCO} = 1.7 to 2.1 V, T_A = 0° to 70°C)[a]

Symbol	Characteristics	0°C Min	0°C Typ	0°C Max	25°C Min	25°C Typ	25°C Max	70°C Min	70°C Typ	70°C Max	Unit	Condition
f_{IN}	Input frequency[b] for VCO_SEL = 0 (high range)											
	1:1 ratio, ASEL=00	150.0		287.5	150.0		287.5	150.0		287.5	MHz	600 < f_{VCO} < 1150 MHz
	1:2 ratio, ASEL=01	150.0		287.5	150.0		287.5	150.0		287.5	MHz	
	3:4 ratio, ASEL=10	200.0		287.5	200.0		287.5	200.0		287.5	MHz	
	4:5 ratio, ASEL=11	150.0		287.5	150.0		287.5	150.0		287.5	MHz	
	Input frequency[b] for VCO_SEL = 1 (low range)											
	1:1 ratio, ASEL=00	75.0		143.75	75.0		150.0	75.0		150.0	MHz	
	1:2 ratio, ASEL=01	75.0		143.75	75.0		150.0	75.0		150.0	MHz	
	3:4 ratio, ASEL=10	100.0		191.67	100.0		191.67	100.0		191.67	MHz	300 < f_{VCO} < 575 MHz
	4:5 ratio, ASEL=11	75.0		143.75	75.0		150.0	75.0		150.0	MHz	
f_{VCO}	VCO frequency											
	VCO_SEL = 0 (high range)	600		1150	600		1150	600		1150	MHz	
	VCO_SEL = 1 (low range)	300		575	300		575	300		575	MHz	
f_{OUT}	Output frequency[c]			287.5			287.5			287.5	MHz	
SPO	Static phase offset, t_{PD} between CLK and FB											
	VCO_SEL=0	-200		-50	-200		-50	-200		-50	ps	
	VCO_SEL=1	-250		-50	-250		-50	-250		-50	ps	
DC	Output duty cycle	45	50	55	45	50	55	45	50	55	%	
t_{SK}	Differential output skew											
	$t_{SK(OB)}$ within bank[d]			80			80			80	ps	Diff. HSTL outputs
	$t_{SK(O)}$ single frequency[e]			100			100			100	ps	
	$t_{SK(O)}$ multiple frequency[f]			250			250			250	ps	
	$t_{SK(OFB)}$ QFB to QA0-6											
	for ASEL=00	85		-115	85		-115	85		-115	ps	
	for ASEL=01	25		-175	25		-175	25		-175	ps	
	for ASEL=10	135		-115	135		-115	135		-115	ps	
	for ASEL=11	65		-135	65		-135	65		-135	ps	
V_{PP}[g]	Minimum input swing	0.5		1	0.5		1	0.5		1	V	LVPECL
V_{CMR}	Common mode range	1		V_{CC}-0.4	1		V_{CC}-0.4	1		V_{CC}-0.4	V	LVPECL
$V_{DIF,OUT}$	Minimum output swing	0.6	0.8		0.6	0.8		0.6	0.8		V	HSTL
V_X	Differential output crosspoint voltage	0.64		0.9	0.68		0.9	0.68		1.0	V	HSTL
$t_{JIT(CC)}$	Cycle-to-cycle jitter											
	f_{VCO} >= 750 MHz			75			75			75	ps	
	f_{VCO} < 750 MHz			125			125			125	ps	
$t_{JIT(PER)}$	Period Jitter VCO_SEL=0			75			75			75	ps	
	VCO_SEL=1			125			125			125	ps	
$t_{JIT(IO)}$	I/O Phase Jitter RMS (1 σ)											
	600 MHz< f_{VCO} <750 MHz			50			50			50	ps	
	750 MHz< f_{VCO} <900 MHz			40			40			40	ps	
	900 MHz< f_{VCO} <1150 MHz			30			30			30	ps	
BW	PLL bandwidth											
	1:1 ratio, ASEL=00		0.6-1.0			0.6-1.0			0.6-1.0		MHz	
	1:2 ratio, ASEL=01		0.6-1.0			0.6-1.0			0.6-1.0		MHz	
	3:4 ratio, ASEL=10		1.0-1.2			1.0-1.2			1.0-1.2		MHz	
	4:5 ratio, ASEL=11		0.6-1.0			0.6-1.0			0.6-1.0		MHz	
t_r, t_f	Output transition rate	0.8		2	0.8		2	0.8		2	V/ns	
t_{Lock}	PLL lock time			10			10			10	ms	

a. Refer to "HSTL Output Termination and AC Test Reference" for AC test conditions.
b. The input frequency for the output configurations are limited by the VCO frequency range and the feedback divider.
c. f_{OUT} at which output-to-output skew, V_X and DC specification are still meet. f_{OUT} is primary a function of f_{IN} and the input-to-output frequency ratio (M:N).
d. Output skew within bank A outputs (QA0-QA6) and output skew within bank B outputs (QB0-QB2).
e. Output skew within all outputs (QA0-QA6, QB0-QB2) running at the same output frequency.
f. Output skew within all outputs (QA0-QA6, QB0-QB2) running at any output frequency.
g. V_{PP} specifies the minimum input differential voltage required for switching.

APPLICATIONS INFORMATION

Using the MPC9990 in zero-delay applications

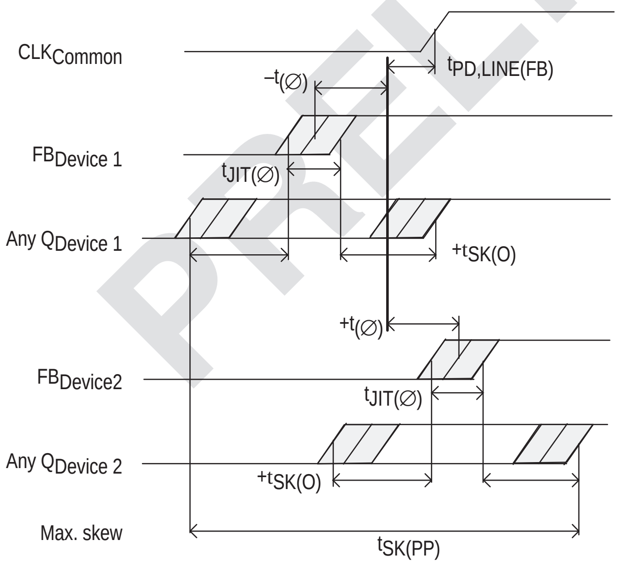
Nested clock trees are typical applications for the MPC9990 Designs using the MPC9990 as PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from static fanout buffers. The external feedback option of the MPC9990 clock driver allows for its use as a zero delay buffer. By using the differential QFB output pair as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input (CLK) and any output. This effective delay consists of the static phase offset (SPO), I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC9990 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9990 are connected together, the maximum overall timing uncertainty from the common CLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset (SPO), output skew, feedback board trace delay and I/O (phase) jitter. The output skew ($t_{SK(O)}$) specification of the MPC9990 is different for single or for dual frequency bank configurations. :



Complementary signals are not shown. Signal references level is the differential voltage crosspoint V_X

Figure 7. MPC9990 max. device-to-device skew

Due to the statistical nature of I/O jitter a rms value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8: Confidence Facter CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) and single frequency configuration is assumed, resulting in a worst case timing uncertainty from input to any output of -420 ps to +170 ps relative to CLK.

$$t_{SK(PP)} = [-200ps...-50ps] + [-100ps...100ps] + [(30ps \cdot -3)...(30ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [-420ps...+170ps] + t_{PD,\ LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 8. "Max. I/O Jitter versus frequency" can be used for a more precise timing performance analysis. The number for the I/O jitter at a specific frequency can be substituted for the more general datasheet specification number:

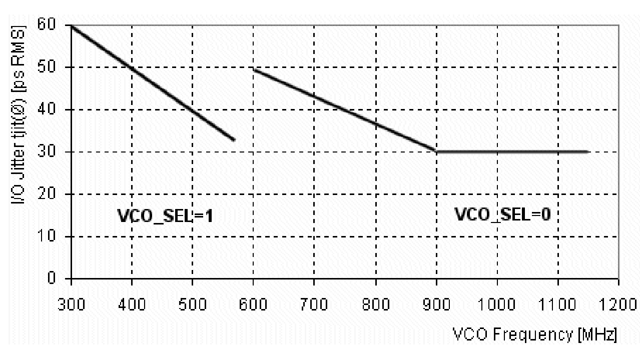
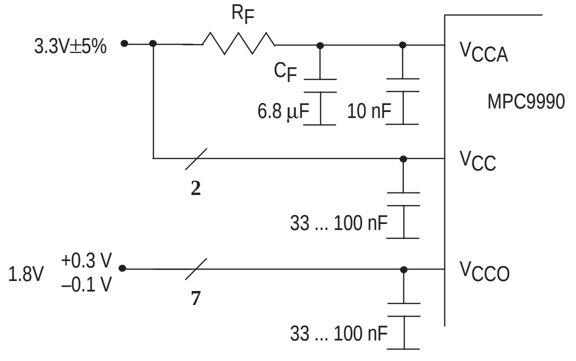


Figure 8. Max. I/O Jitter versus frequency

Power Supply Filtering

The MPC9990 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply. Random noise on the V_{CCA} power supply impacts the device AC characteristics, for instance I/O jitter. The MPC9990 provides separate power supplies for the output buffers (V_{CCO}) and the phase-locked loop (V_{CCA}) of the device.

$R_F \leq 9\ \Omega$ for V_{CC} = 3.3V



Place V_{CCA} filter and V_{CCO}, V_{CC} bypass capacitors as close as possible to the device

Figure 9. Recommended Power Supply Filter

The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is difficult to minimize noise on the power supplies a second level of isolation may be required. A simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9990. Figure 9. illustrates a recommended power supply low-pass frequency filter scheme. The MPC9990 VCO frequency and phase stability is most susceptible to noise with spectral content in the 300 kHz to 3 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. The maximum voltage drop on V_{CCA} that can be tolerated is 135 mV with respect to V_{CC} = 3.3V ± 5%, resulting in a lowest allowable supply voltage for V_{CCA} equal to 2.835 V.

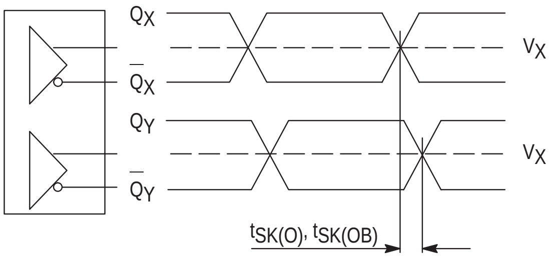
From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 11 mA (15 mA maximum), assuming that the minimum of 3.0V (V_{CC}=3.3V-5%-0.135V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 9. “Recommended Power Supply Filter” should have a maximum resistance of 9 Ω to meet the voltage drop criteria. The minimum resistance for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater 40 dB for noise whose spectral content is above 300 kHz. In the example RC filter shown in Figure 9. “Recommended Power Supply Filter”, the filter cut-off frequency is 16.3 kHz and the noise attenuation at 300 kHz is approximately 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown (6.8 µF || 10 nF) ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9990 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds, internal voltage regulation and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Recommended Power-up Sequence

The MPC9990 does not require any special supply ramp sequence in case the system provides all supply voltages (3.3V and 1.8V) at the same time. The reference clock signal (CLK, $\overline{CLK}$) can be applied any time during or after the power up sequence if V_{IN} is smaller or equal V_{CC} during the voltage transition. Following are guidelines for the MPC9990 power-up sequence in case the 3.3V and 1.8V voltage supply cannot be applied at the same time:

- HSTL output supply voltage V_{CCO} must be powered up to the specified voltage range before or at the same time than V_{CC}. V_{CCA} can be powered up before, at the same time or after V_{CC} and V_{CCO}.
- At the time the power supplies are powered up, the device should be reset (MR=0).
- Apply the clock input signals to the PLL (CLK, $\overline{CLK}$) after all power supplies are stable. Then, MR can be deasserted (MR=1). This will release the internal PLL which will attempt to lock
- The time from $\overline{MR}$ deassertion to PLL lock will be specified by the PLL lock time t_{Lock}. After the PLL achieved lock, the AC characteristics are valid.
- Outputs can be enabled by OE any time. QFB is not affected by OE and the PLL can achieve lock even if OE is tied high (OE = 1, disable).



The pin–to–pin skew is defined as the worst case difference in propagation delay between any two similar delay path within a single device ($t_{SK(O)}$) or within a single output bank ($t_{SK(OB)}$)

Figure 10. Output–to–output Skew $t_{SK(O)}$, $t_{SK(OB)}$

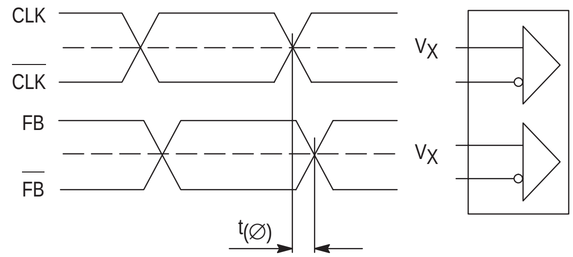
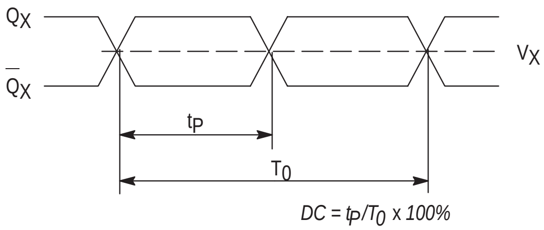
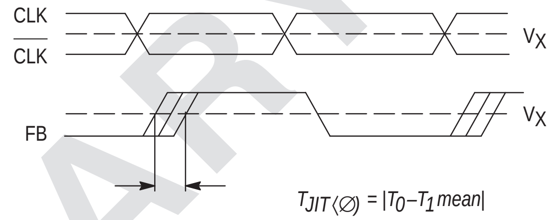


Figure 11. Propagation delay ($t_{\varnothing}$, static phase offset, SPO) test reference



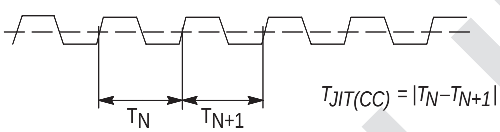
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 12. Output Duty Cycle (DC)



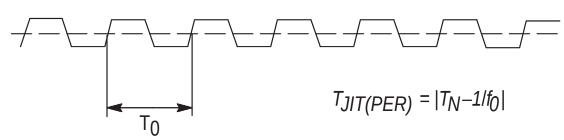
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles, measured at the FB signal (only true signal shown)

Figure 13. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs, measured at an output (only true signal shown)

Figure 14. Cycle–to–cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles (only true signal shown)

Figure 15. Period Jitter

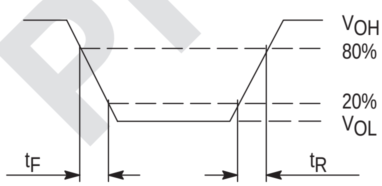
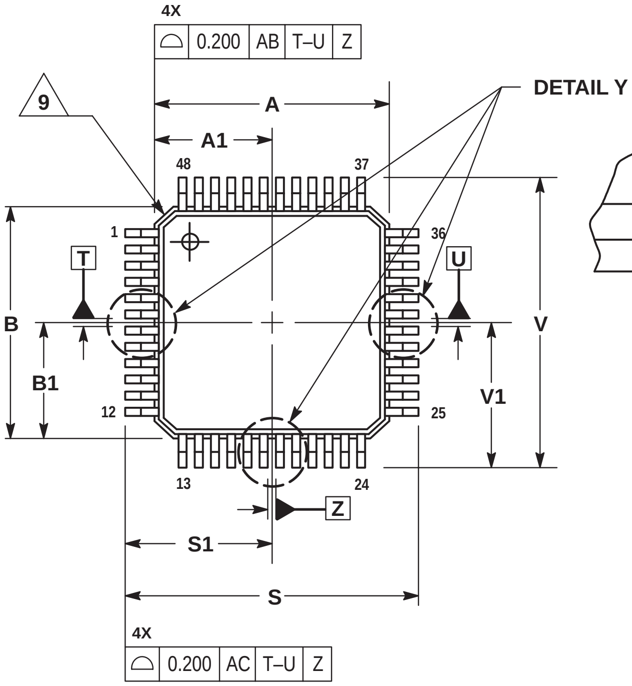
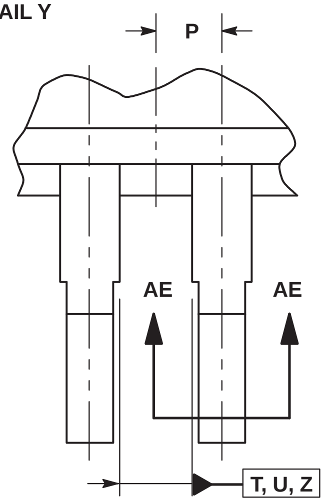


Figure 16. Output Transition Time Test Reference

OUTLINE DIMENSIONS

FA SUFFIX
LQFP PACKAGE
CASE 932-03
ISSUE F

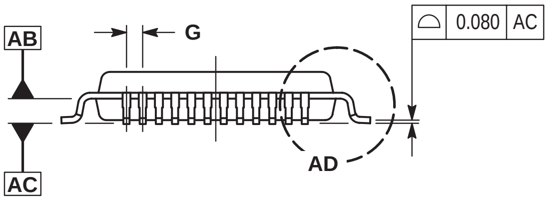


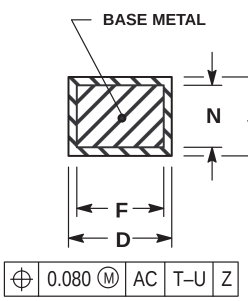


DETAIL Y

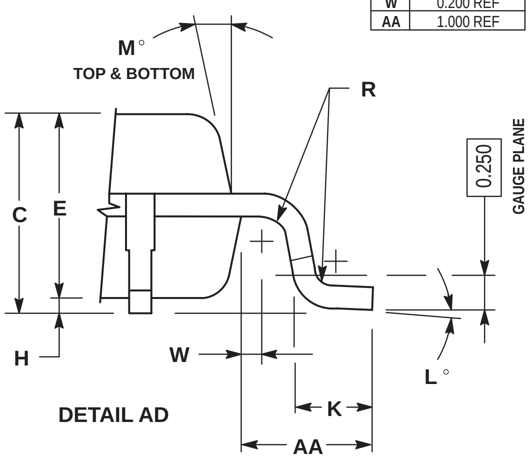
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0 °	7 °
M	12 °REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	





SECTION AE–AE



DETAIL AD

NOTES

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