International
IOR Rectifier

SERIES IRK.170, .230, .250

SCR / SCR and SCR / DIODE **NEW MAGN-A-pak™ Power Modules**

170A
230A
250A

Features

- High voltage.
- Electrically isolated base plate
- 3000 V_{RMS} isolating voltage
- Industrial standard package
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- Beryllium oxide substrate
- Also available with aluminum nitrade substrate

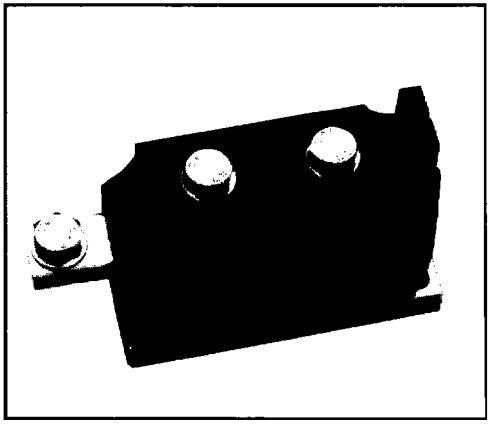
Description

This new IRK serie of MAGN-A-paks modules uses high voltage power thyristor/thyristor and thyristor/diode in seven basic configurations. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase or three phase bridges or as AC-switches when modules are connected in anti-parallel mode.
These modules are intended for general purpose applications such as battery chargers, welders and plating equipment and where high voltage and high current are required (motor drives, U.P.S., etc.).

DATA SHEETS

Major Ratings and Characteristics

Parameters		IRK.170	IRK.230	IRK.250	Units
$I_{T(AV)}$	@ 85°C	170	230	250	A
$I_{T(RMS)}$		377	510	555	A
I_{TSM}	@ 50Hz	5100	7500	8500	A
	@ 60Hz	5350	7850	8900	A
I^2t	@ 50Hz	131	280	361	kA^2s
	@ 60Hz	119	256	330	kA^2s
$I^2\sqrt{t}$		1310	2800	3610	$kA^2\sqrt{s}$
$V_{DRM} - V_{RRM}$		Up to 1600	Up to 2000	Up to 1600	V
T_J		-40 to 130			°C



ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{RRM} V_{DRM}, maximum repetitive peak reverse and off-state blocking voltage V	V_{RSM}, maximum non-repetitive peak reverse voltage V	I_{RRM} I_{DRM} max @ 130°C m A
IRK.170, 230, 250	04	400	500	50
	06	600	700	50
	08	800	900	50
	10	1000	1100	50
	12	1200	1300	50
	14	1400	1500	50
	16	1600	1700	50
IRK.230	18	1800	1900	
	20	2000	2100	50

On-state Conduction

	Parameters	IRK.170	IRK.230	IRK.250	Units	Conditions		
$I_{T(AV)}$	Maximum average on-state current	170	230	250	A	180° conduction, half sine wave		
	@ Case temperature	85	85	85	°C			
$I_{T(RMS)}$	Maximum RMS on-state current	377	510	555	A	as AC switch		
I_{TSM}	Maximum peak, one-cycle on-state, non-repetitive surge current	5100	7500	8500	A	t=10ms	No voltage reapplied	Sinusoidal half wave, Initial $T_J = T_J$ max
		5350	7850	8900	A	t=8.3ms		
		4300	6300	7150	A	t=10ms	100% V_{RRM}	
		4500	6600	7500	A	t=8.3ms	reapplied	
I^2t	Maximum I^2t for fusing	131	280	361	kA^2s	t=10ms	No voltage	Sinusoidal half wave, Initial $T_J = T_J$ max
		119	256	330	kA^2s	t=8.3ms	reapplied	
		92.5	198	255	kA^2s	t=10ms	100% V_{RRM}	
		84.4	181	233	kA^2s	t=8.3ms	reapplied	
$I^2\sqrt{t}$	Maximum $I^2\sqrt{t}$ for fusing	1310	2800	3610	$kA^2\sqrt{s}$	t=0.1 to 10ms, no voltage reapplied		
$V_{T(TO)1}$	Low level value of threshold voltage	0.89	1.03	0.97	V	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ $T_J = T_J$ max.		
$V_{T(TO)2}$	High level value of threshold voltage	1.12	1.07	1.00	V	$(\pi \times I_{T(AV)} < I < 20 \times \pi \times I_{T(AV)})$ $T_J = T_J$ max.		
r_{t1}	Low level on-state slope resistance	1.34	0.77	0.60	mΩ	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ $T_J = T_J$ max.		
r_{t2}	High level on-state slope resistance	0.96	0.73	0.57	mΩ	$(\pi \times I_{T(AV)} < I < 20 \times \pi \times I_{T(AV)})$ $T_J = T_J$ max.		
V_{TM}	Maximum on-state voltage drop	1.60	1.59	1.44	V	$I_{TM} = \pi \times I_{T(AV)}$, $T_J = T_J$ max., 180° conduction Av. power = $V_{T(TO)} \times I_{T(AV)} + r_t \times (I_{T(RMS)})^2$		
I_H	Maximum holding current	500	500	500	mA	Anode supply=12V, initial I_T=30A, T_J=25°C		
I_L	Maximum latching current	1000	1000	1000	mA	Anode supply=12V, resistive load=1Ω gate pulse: 10V, 100µs, T_J=25°C		

Switching

t_d	Typical delay time	1.0	1.0	1.0	µs	T_J= 25°C	Gate Current=1A $di_{g/dt}$=1A/µs
t_r	Typical rise time	2.0	2.0	2.0	µs	T_J= 25°C	Vd = 0,67% V_{DRM}
t_q	Typical turn-off time	50 - 150			µs	I_{TM} = 300 A ; -dI/dt=15 A/µs; $T_J = T_J$ max ; Vr = 50 V; dV/dt = 20 V/µs ; Gate 0 V, 100 ohm	

Blocking

I_{RRM} I_{DRM}	Max. peak reverse and off-state leakage current	50	mA	$T_J = T_J$ max.
V_{INS}	RMS isolation voltage	3000	V	50Hz, circuit to base, all termin. shorted, 25°C, 1s
$dv/_{dt}$	Critical rate of rise of off-state voltage	500	V/µs	$T_J = T_J$ max, linear to 80% rated V_{DRM}
		1000	V/µs	$T_J = T_J$ max, linear to 67% rated V_{DRM}

Triggering

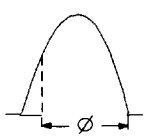
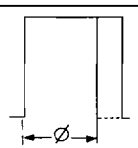
P_{GM}	Maximum peak gate power	10.0	W	tp ≤ 5ms,	$T_J = T_J$ max.
$P_{G(AV)}$	Maximum average gate power	2.0	W	f = 50Hz,	$T_J = T_J$ max.
$+I_{GM}$	Maximum peak gate current	3.0	A	tp ≤ 5ms,	$T_J = T_J$ max.
$-V_{GT}$	Max. peak negative gate voltage	5.0	V	tp ≤ 5ms,	$T_J = T_J$ max.
V_{GT}	Maximum required DC gate voltage to trigger	4.0 3.0 2.0	V V V	T_J = - 40°C T_J = 25°C $T_J = T_J$ max.	Anode supply = 12V, resistive load ; Ra = 1Ω
I_{GT}	Maximum required DC gate current to trigger	350 200 100	mA mA mA	T_J = - 40°C T_J = 25°C $T_J = T_J$ max.	Anode supply = 12V, resistive load ; Ra = 1Ω
V_{GD}	Maximum gate voltage that will not trigger	0.25	V	@ $T_J = T_J$ max., rated V_{DRM} applied	
I_{GD}	Maximum gate current that will not trigger	10.0	mA	@ $T_J = T_J$ max., rated V_{DRM} applied	
$di/_{dt}$	Max rate of rise of turned-on current	500	A/µs	@ $T_J = T_J$ max., I_{TM} = 400 A rated V_{DRM} applied	

Thermal and Mechanical Specifications

T_J	Junction operating temperature	-40 to 130			°C	
T_{stg}	Storage temperature range	-40 to 150			°C	
R_{thJC}	Maximum thermal resistance junction to case	0.17	0.125	0.125	K/W	Per junction, DC operation
R_{thC-S}	Thermal resistance, case to heatsink	0.02	0.02	0.02	K/W	Mounting surface flat, smooth and greased (per module)
T Mounting tourque ±10%	MAGN-A-pak to heatsink	4 to 6			Nm	A mounting compound is recommended and the tourque should be rechecked after a period of about 3 hours to allow for the spread of the compound
	Busbar to MAGN-A-pak	8 to 10			Nm	
wt	Approximate weight	500			g	
		17.8			oz	
	Case style	MAGN-A-pak				

ΔR Conduction (per Junction)

(The following table shows the increment of thermal resistance RthJC when devices operate at different conduction angles than DC)

Conduction angle		IRK.170	IRK.230	IRK.250	Units	Conditions
	180°	0.009	0.009	0.009	K/W	$T_J = T_J$ max.
	120°	0.010	0.010	0.010	K/W	
	90°	0.010	0.010	0.014	K/W	
	60°	0.020	0.020	0.020	K/W	
	30°	0.032	0.032	0.032	K/W	
	180°	0.007	0.007	0.007	K/W	$T_J = T_J$ max.
	120°	0.011	0.011	0.011	K/W	
	90°	0.015	0.015	0.015	K/W	
	60°	0.020	0.020	0.020	K/W	
	30°	0.033	0.033	0.033	K/W	

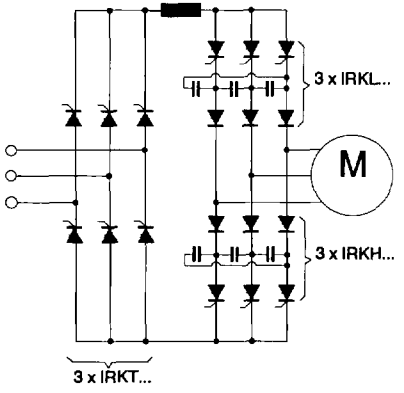
DATA SHEETS

MAGN-A-paks Suitable for Current Source Inverters

Thyristor		Diode	$I_{T(AV)}$ / $I_{F(AV)}$ @ T_C		
V_{DRM}	V_{RSM}	V_{RRM}	170A	230A	250A
V_{RRM}		V_{RSM}	@ 85°C	@ 85°C	@ 85°C
1400	1500	2000	IRKH170-14D20	IRKH230-14D20	IRKH250-14D20
1400	1500	2000	IRKL170-14D20	IRKL230-14D20	IRKL250-14D20
1600	1700	2500	IRKH170-16D25	IRKH230-16D25	IRKH250-16D25
1600	1700	2500	IRKL170-16D25	IRKL230-16D25	IRKL250-16D25
1800	1900	2800	Not Available	IRKH230-18D28	Not Available
1800	1900	2800	Not Available	IRKL230-18D28	Not Available
2000	2100	3200	Not Available	IRKH230-20D32	Not Available
2000	2100	3200	Not Available	IRKL230-20D32	Not Available

For all other parameters and characteristics refer to standard IRKH... and IRKL... modules.

Application Notes



Current Source Inverter using 9 MAGN-A-paks

Current Source Inverters

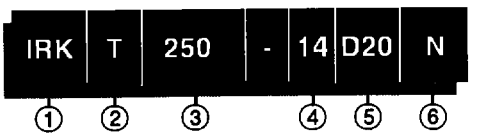
Current-Source Inverters (also known as Sequentially Commutated Inverters) use Phase Control (as opposed to Fast) Thyristors and Diodes.

The advantages of Current Source Inverters lie in their ease control, absence of large commutation inductances and limited fault currents.
Their simple construction, illustrated by the circuit on the left, is further enhanced by the use of MAGN-A-paks which allow the power circuit of an Inverter to be realised with 6 capacitors and 9 MAGN-A-paks all mounted on just one heatsink.

The optimal design of Current Source Inverters requires the use of Diodes with blocking voltages greater than those of the thyristors .
This departure from conventional half-bridge modules is catered for by MAGN-A-pak range with Thyristors up to 2000V and Diodes up to 3200V.

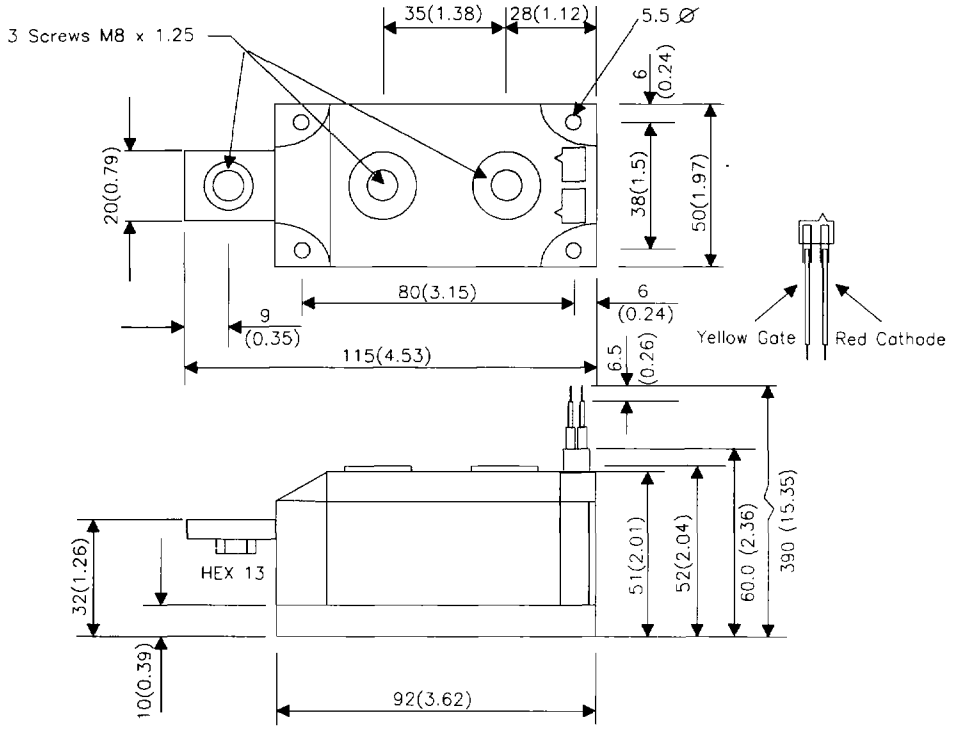
Ordering Information Table

Device Code



1 - Module type
2 - Circuit configuration (See Outline Table)
3 - Current rating
4 - Voltage code: Code x 100 = V_{RRM} (See Voltage Ratings Table)
5 - Current Source Inverters Types
6 - None = Standard devices (beryllium oxide)
N = aluminium nitrade substrate (Contact factory)

Outline Table



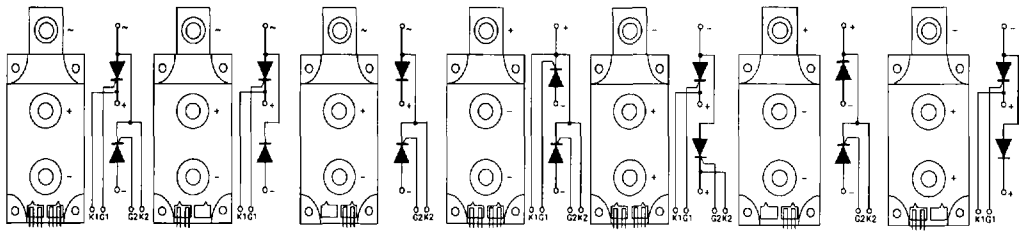
CONTAINS BERYLLIUM OXIDE CERAMIC

- May contain Beryllium Oxide Ceramic, and under normal circumstances is non hazardous.
- Do not open, cut or grind.
- Unserviceable parts must be disposed of as harmful waste.

HARMFUL

- All dimensions in millimeters (inches)
- Dimensions are nominal
- Full engineering drawings are available on request
- UL identification number for gate and cathode wire: UL 1385
- UL identification number for package: UL 94V0

IRKT... IRKH... IRKL... IRKU... IRKV... IRKK... IRKN...



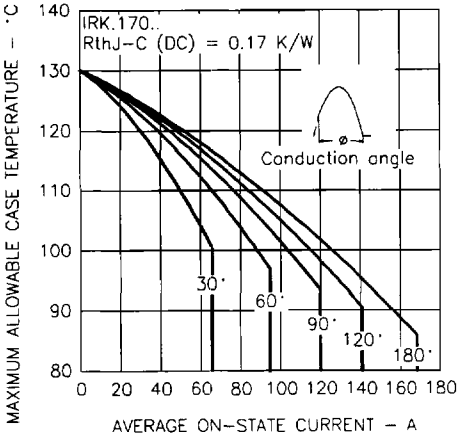


Fig. 1 - Current Ratings Characteristics

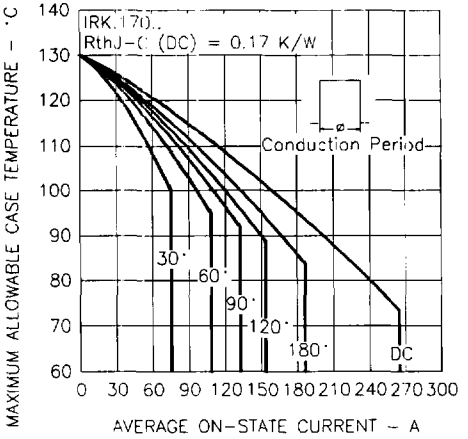


Fig. 2 - Current Ratings Characteristics

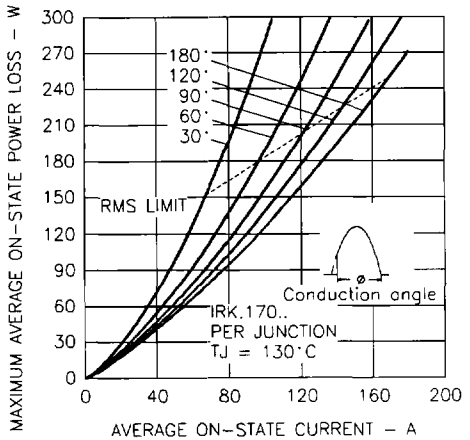


Fig. 3 - On-state Power Loss Characteristics

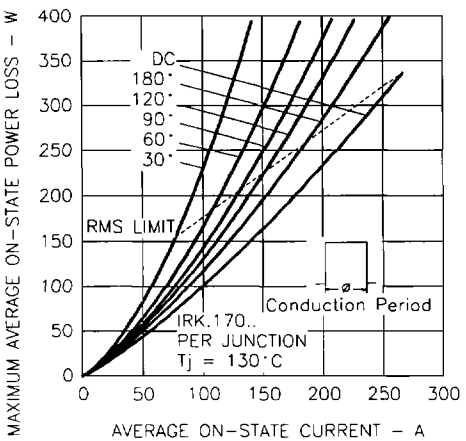


Fig. 4 - On-state Power Loss Characteristics

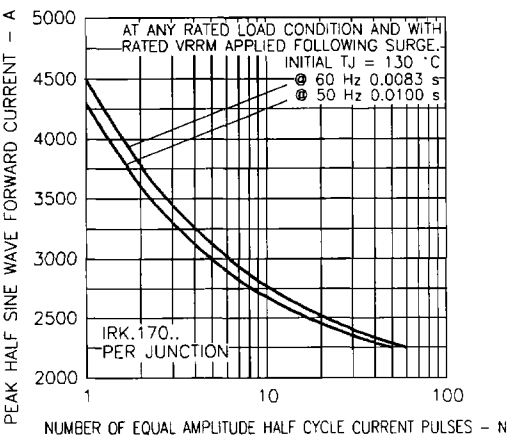


Fig. 5 - Maximum Non-Repetitive Surge Current

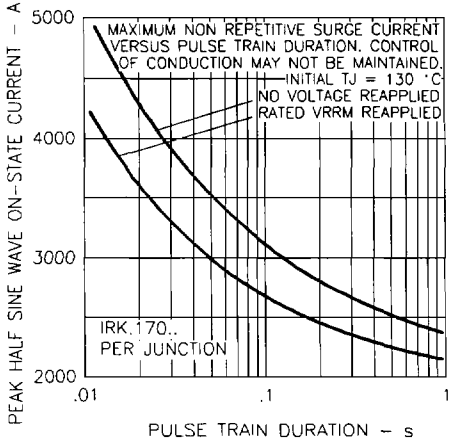


Fig. 6 - Maximum Non-Repetitive Surge Current

DATA SHEETS

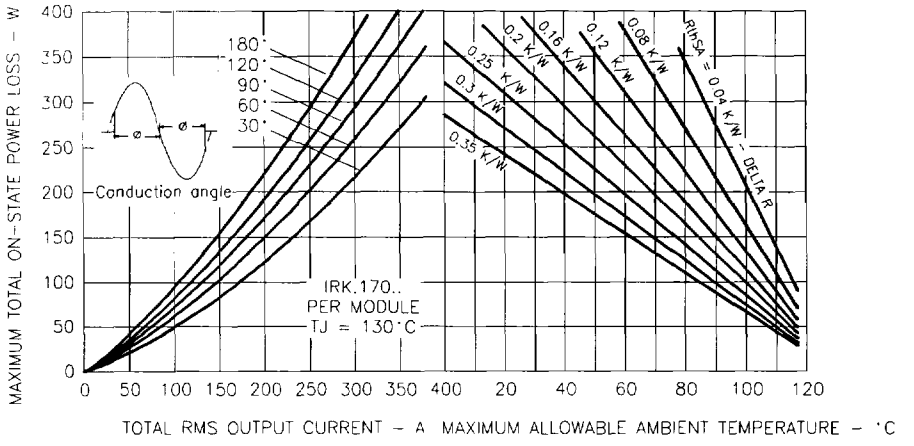


Fig. 7 - On-state Power Loss Characteristics

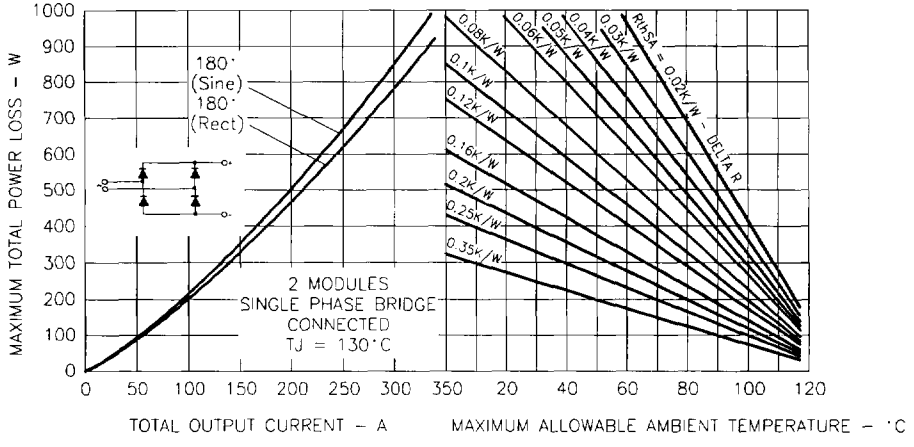


Fig. 8 - On-state Power Loss Characteristics

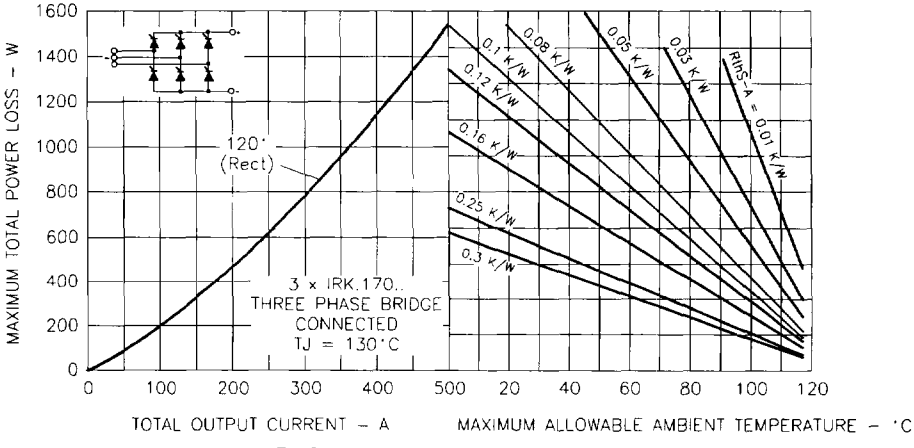


Fig. 9 - On-state Power Loss Characteristics

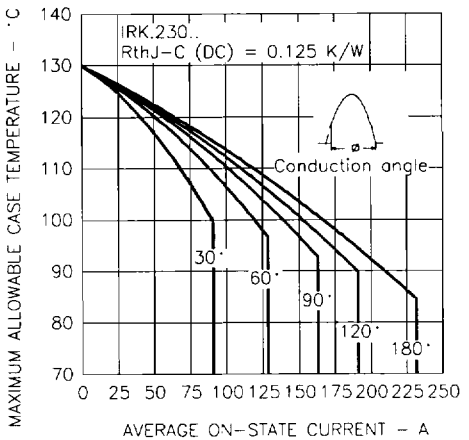


Fig. 10 - Current Ratings Characteristics

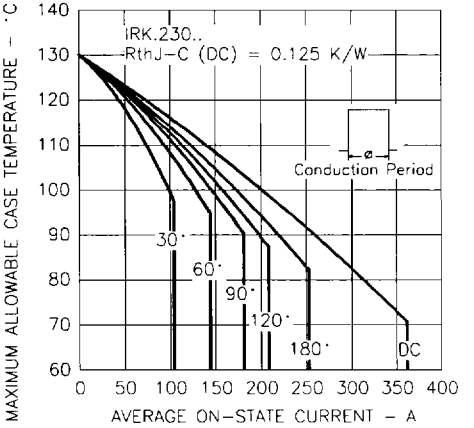


Fig. 11 - Current Ratings Characteristics

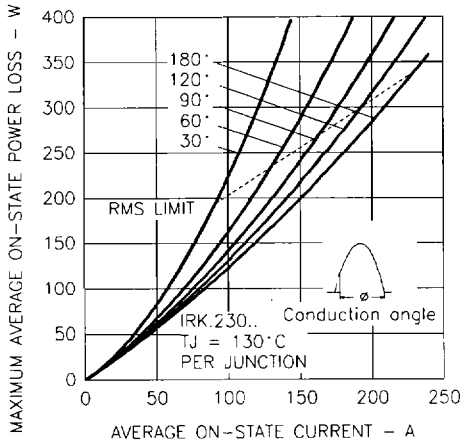


Fig. 12 - On-state Power Loss Characteristics

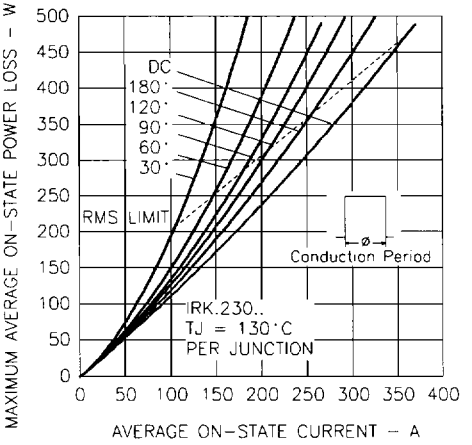


Fig. 13 - On-state Power Loss Characteristics

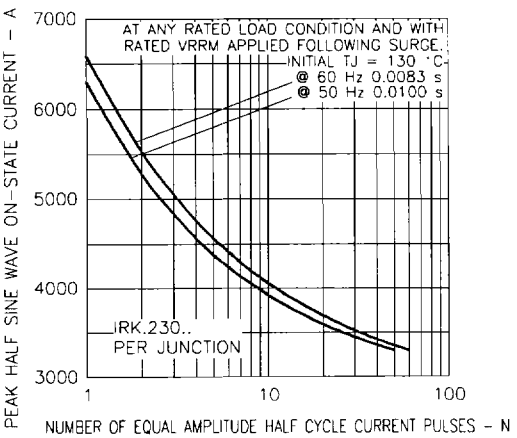


Fig. 14 - Maximum Non-Repetitive Surge Current

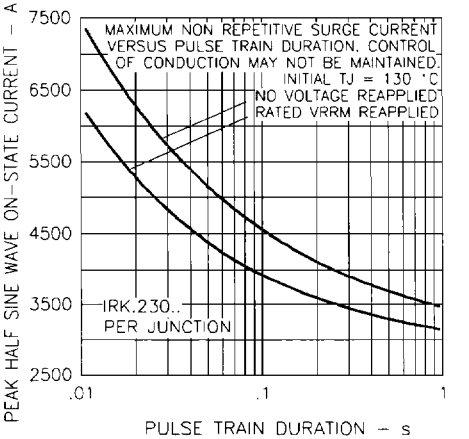


Fig. 15 - Maximum Non-Repetitive Surge Current

DATA SHEETS

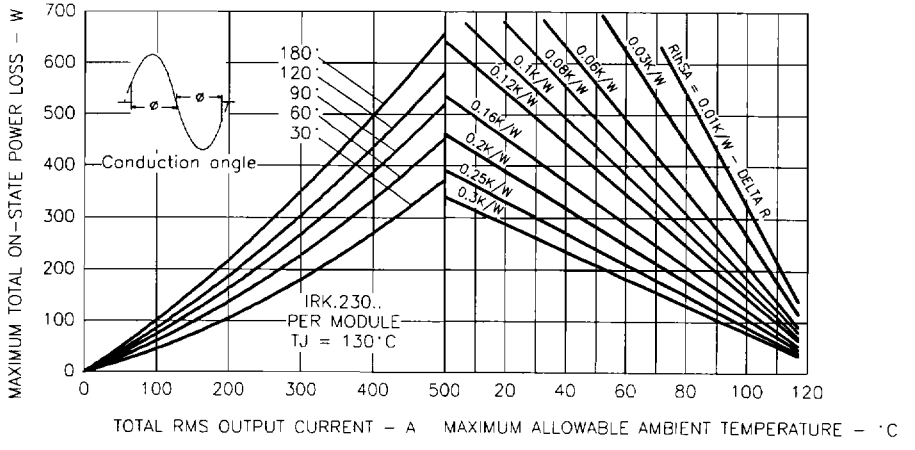


Fig. 16 - On-state Power Loss Characteristics

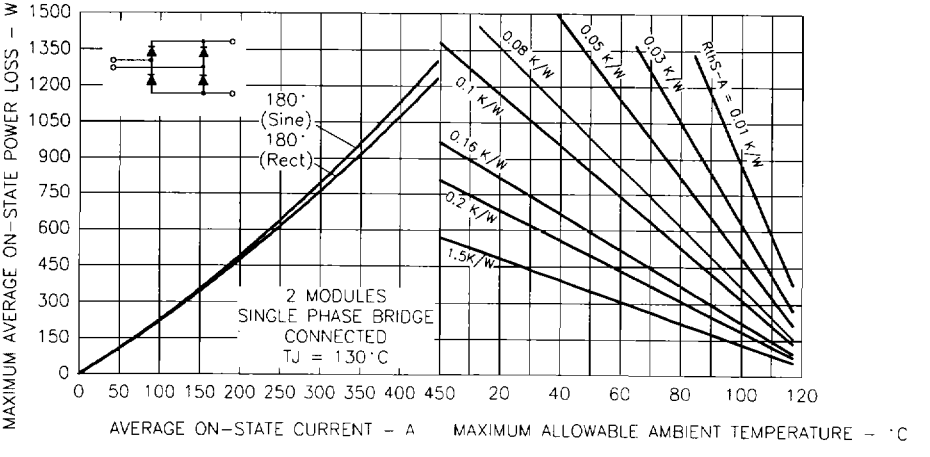


Fig. 17 - On-state Power Loss Characteristics

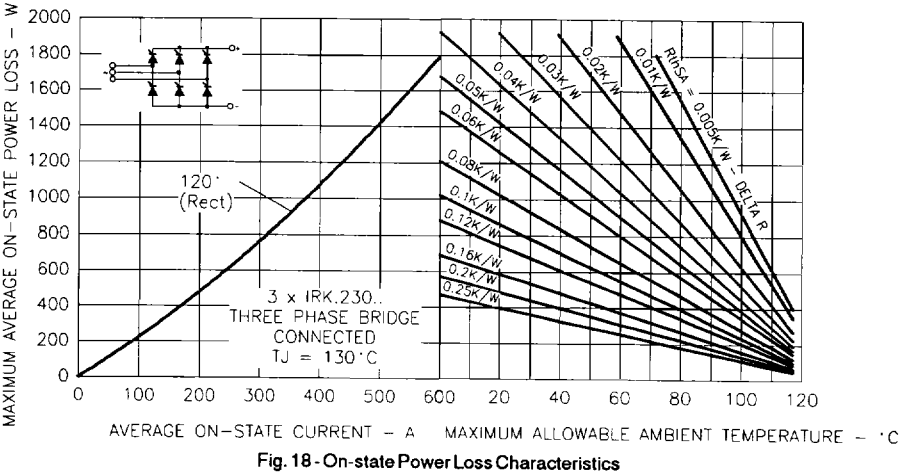


Fig. 18 - On-state Power Loss Characteristics

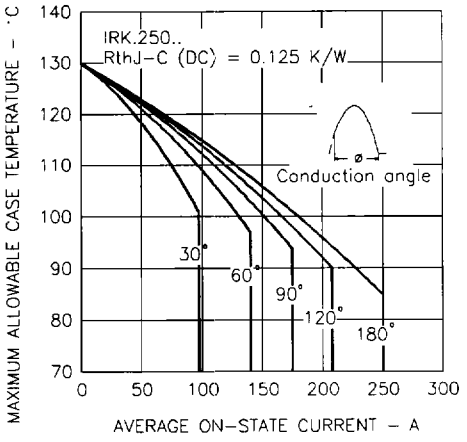


Fig. 19 - Current Ratings Chartacteristics

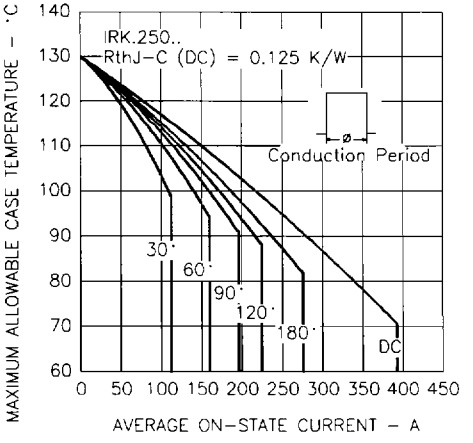


Fig. 20 - Current Ratings Chartacteristics

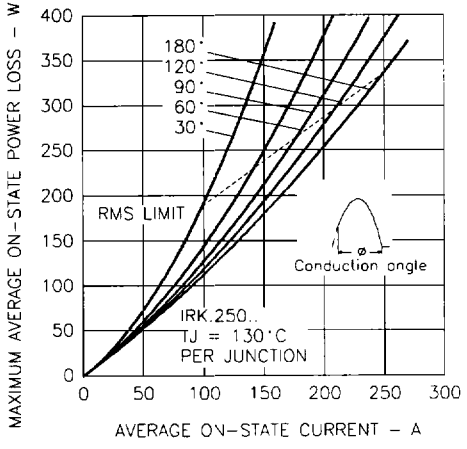


Fig. 21 - On-state Power Loss Characteristics

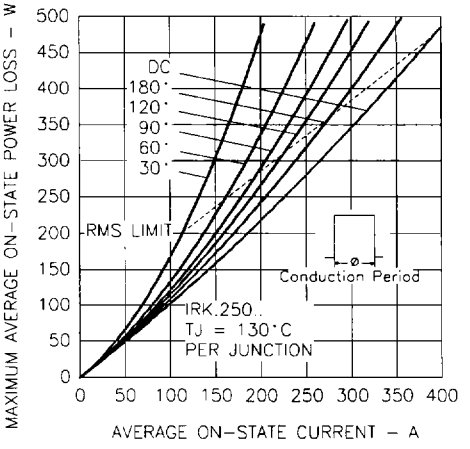


Fig. 22 - On-state Power Loss Characteristics

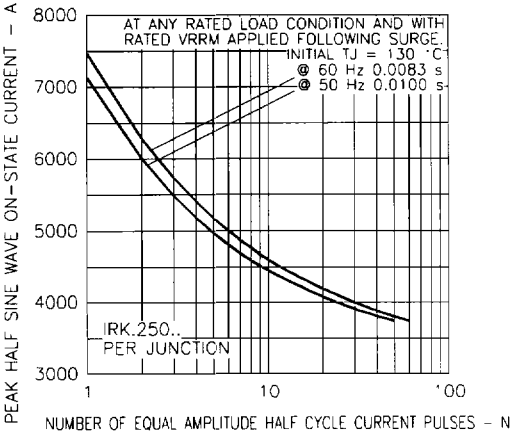


Fig. 23 - Maximum Non-Repetitive Surge Current

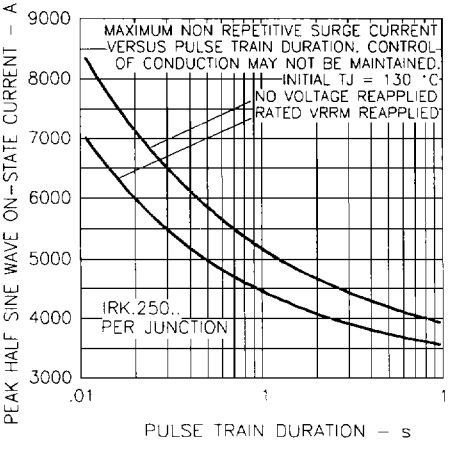


Fig. 24 - Maximum Non-Repetitive Surge Current

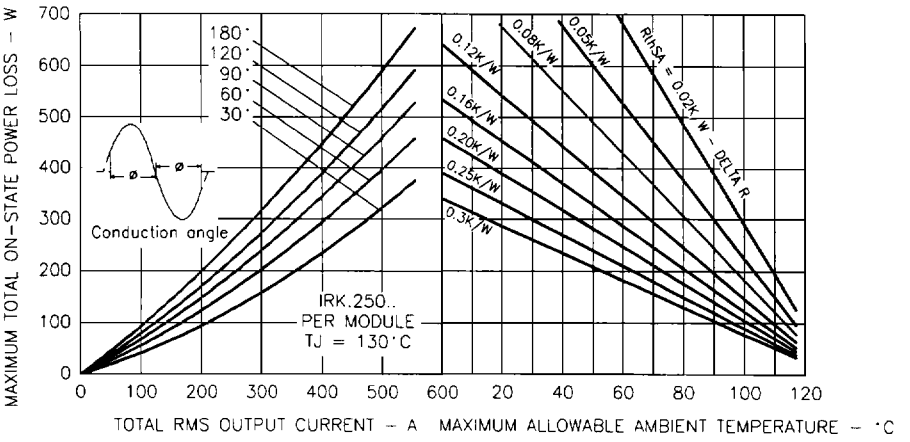


Fig. 25 - On-state Power Loss Characteristics

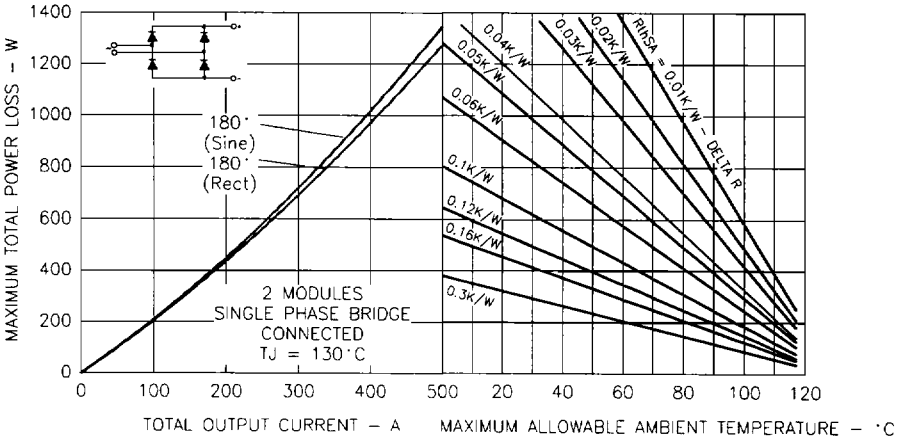


Fig. 26 - On-state Power Loss Characteristics

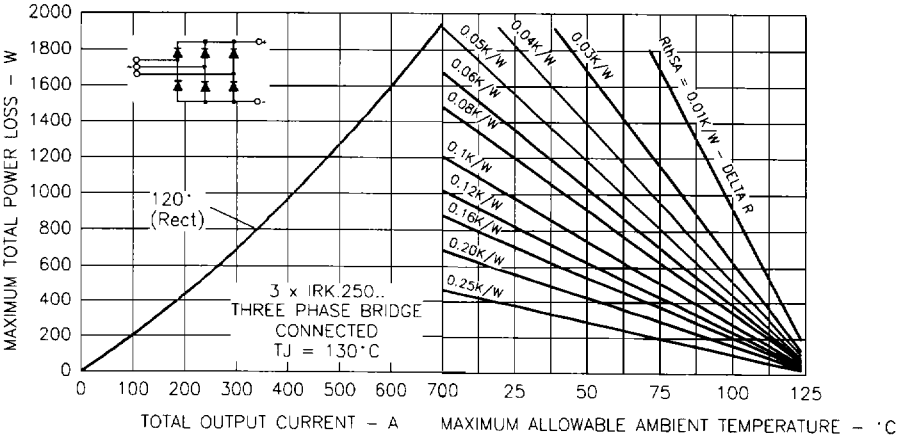


Fig. 27 - On-state Power Loss Characteristics

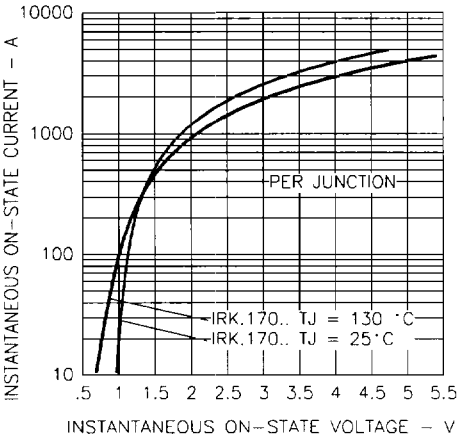


Fig. 28 - On-state Voltage Drop Characteristics

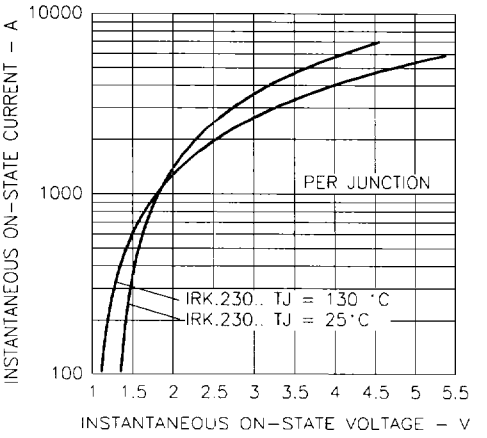


Fig. 29 - On-state Voltage Drop Characteristics

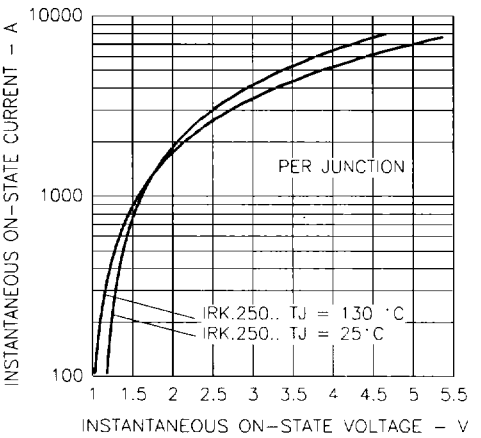


Fig. 30 - On-state Voltage Drop Characteristics

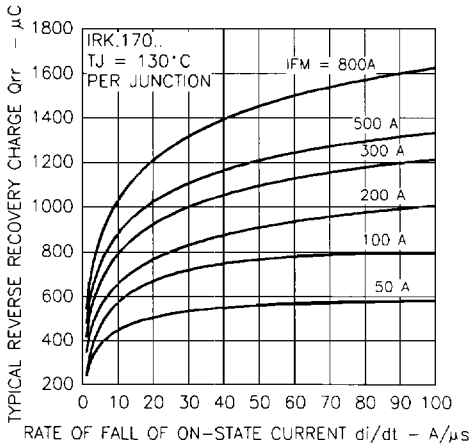


Fig. 31 - Reverse Recovery Charge Characteristics

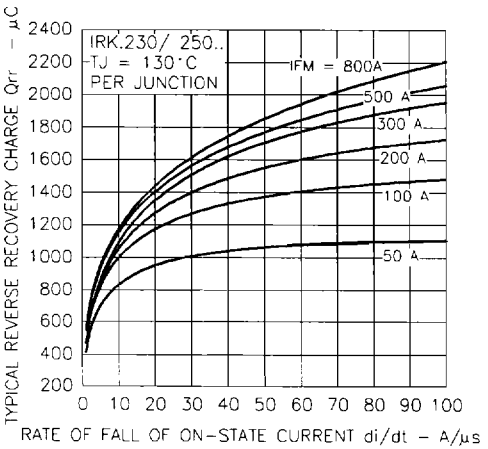


Fig. 30 - Reverse Recovery Charge Characteristics

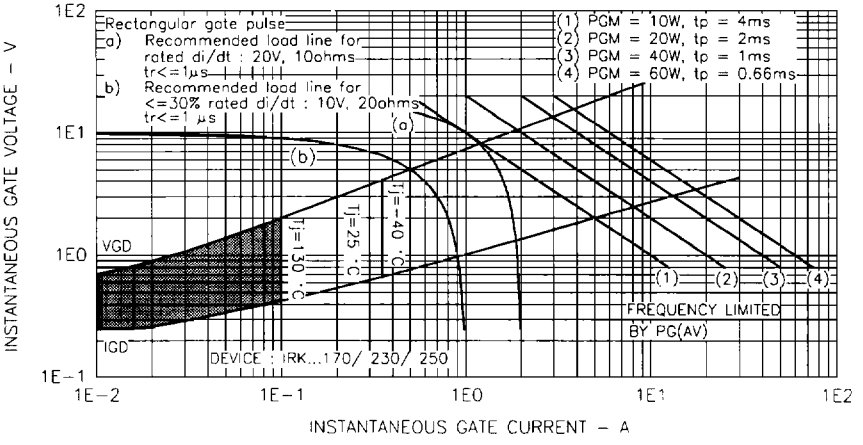


Fig. 33 - Gate Characteristics

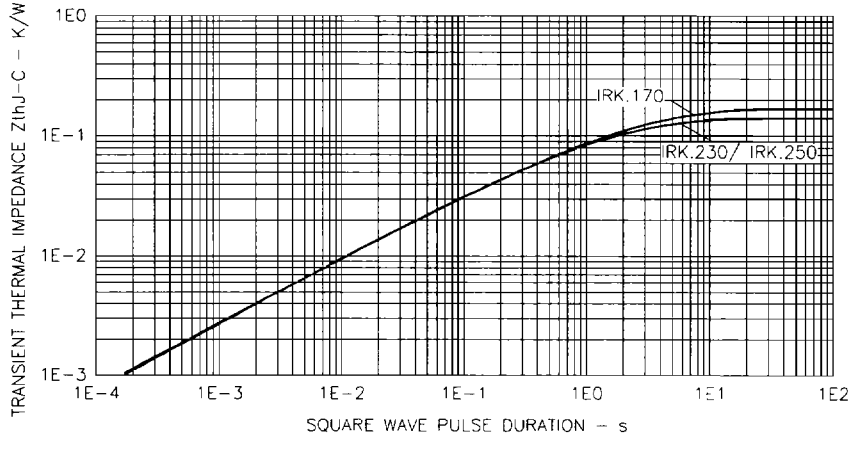


Fig. 34 - Thermal Impedance ZthJC Characteristics