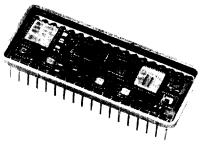


# Synchro (Resolver)-to-Digital Converter 10-bit, 36-pin DDIP Hybrid

#### Features -

- Very high tracking rate (100 rps)
- 21 arc-minute accuracy
- True differential inputs
- TTL and CMOS compatible
- High input impedance
- Analog velocity and error voltage outputs
- MIL-STD-883 Processing is Available



**ACTUAL SIZE** 

### Applications -

2-speed synchro (resolver) systems
Machine tool control systems
Avionics systems
Coordinate conversion
Antenna monitoring
Solar panel control systems

#### Description

Introduced to provide an alternate source for existing designs. Model HSD1510 (HRD1510), a 10-bit sychro (resolver)-to-digital converter, is packaged in a 36-pin DDIP hybrid. Offering very high tracking capability (up to 100 revolutions per second), the 1510 requires only a single +15 V-dc main power supply for its operation and the converter maintains both static and dynamic accuracy over a wide range of power supply voltages. The digital output voltage levels can be controlled independently by a logic voltage input VL. The logic supply voltage V<sub>I</sub> can range from 4.5 V-dc to the main power supply voltage. In addition the converter provides three analog outputs - the ac error voltage, the dc error voltage and the velocity voltage.

Model 1510 is a high gain Type II tracking converter exhibiting zero error for a constant velocity input. The basic conversion process consists of continuously comparing the digital output angle  $(\phi)$  and the Sychro (or Resolver) input angle  $(\theta)$ . An up-down counter, containing the feed-back angle, is changed (increased or decreased) until the feed-back angle equals the input angle.

Once synchronized, the output angle tracks the input angle continuously and the data is always fresh. Output of the up-down counter is buffered to allow independent control of digital output voltage levels. The operation of the Model 1510 is illustrated in the functional diagram of figure 1.

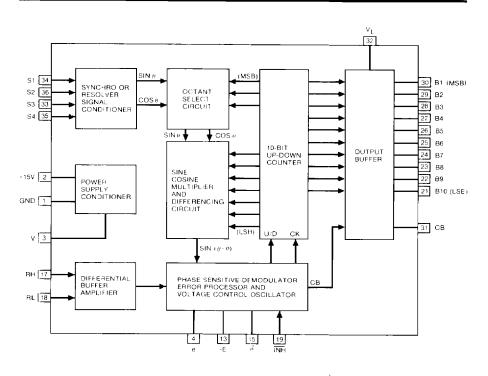


FIGURE 1 1510 Block Diagram

# Synchro/Resolver Connections and Phasing

The connections for synchro and resolver inputs are shown in figure 2. The input signal conditioner of the Model 1510 converter is designed to accept either synchro or resolver inputs. In addition it uses differential amplifiers and matched precision resistors to provide a high common-mode rejection ratio. This eliminates the need for external transformers for most applications. The input signal conditioner performs two functions. For both synchro and resolver format inputs it serves as a precision attenuator reducing the amplitude of high level ac input signals to levels which can be processed by the converter. For a synchro input, this network transforms three wire synchro information into resolver format ( $\sin \theta$  and  $\cos \theta$ ).

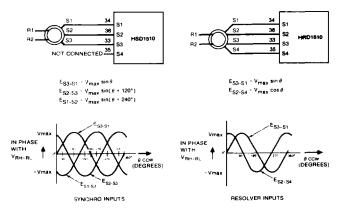


FIGURE 2 Synchro/Resolver Inputs

# Input Protection -

Both signal and reference inputs are true diffential inputs and use precision thin-film resistors for signal attenuation. If input voltages exceed the absolute maximum ratings, the thin-film resistors may be destroyed. To prevent this from happening, it is recommended that transient voltage suppressors be installed on both signal and reference lines. Synchros and resolvers are highly inductive and can generate or couple transients many times greater than their normal

signal voltages and can easily exceed the absolute maximum ratings. This situation is particularly likely to occur in cases where the excitation or source voltage for the synchro (resolver) is switched on or off. Transients can also occur by other equipment being turned on or off. Figures 3 and 4 show recommended methods of connecting synchro and resolver inputs. Transient voltage suppressor given in the tables (or equivalent) must be used to assure input protection.

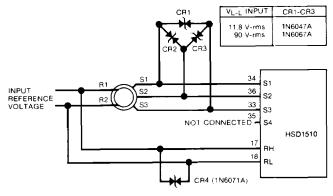


FIGURE 3 HSD1510 Input Protection

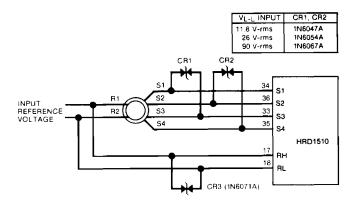


FIGURE 4 HRD1510 Input Protection

### Output Data Transfer -

Digital output data transfer from the 1510 converter is illustrated in timing diagram of figure 5. The digital output of the converter changes in steps of 1 LSB and for every LSB change, a converter busy (CB) pulse of 2 μs is generated. The output data change is initiated by the leading edge of the CB pulse. In order not to transfer data during transition, the converter busy (CB) or inhibit function (INH) should be used. There are two methods available for transferring data. One method is to monitor the CB output and transfer data at the trailing edge of the CB pulse (figure a). The preferred method is on command signal. Set the INH input to logic "low," wait for 2  $\mu$ s and transfer data (figure b). The INH pin should be brought to logic "high" (or open) after data transfer, to allow the converter to keep tracking the input signal. If your application requires the converter to keep tracking even during inhibit, contact a Natel applications engineer.

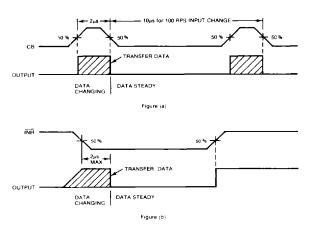


FIGURE 5 Timing Diagram for Data Transfer

# Pin Designations

+15 V	Main Power Supply -					
113 4	11 V-dc to 17 V-dc		GND	1	36	S2
	11 V-dc to 17 V-dc		+15V	2	35	S4
٧L	Logic Voltage -		V	3	34	S1
, r	5 V-dc (For TTL compatible output)		e	4	33	S3
	4.5 V-dc to +15 V supply		NC	5	32	$v_L$
	(For CMOS compatible output)		NC	6	31	СВ
	(1 of omos companies output)		NC	7	30	B1
GND	Power Supply Ground		NC	8	29	B2
	Digital Ground		NC	9	28	B3
	- · <b>g</b> · · · · · · · · · · · · · · · · · · ·		NC	10	27	B4
B1 - B10	Parallel Output Data Bits -		NC	11	26	B5
	B1 is MSB = 180 degrees		NC	12	25	B6
	B10 is LSB = 0.35 degree		-E	13	24	B7
	•		NC	. 14	23	B8
S1, S2, S3, S4	Input Analog Signals -		$\dot{\theta}$	15	22	B9
	Leave S4 unconnected for synchro-input		NC	16	21	B10
	·		RH	17	20	NC
RH, RL	Reference Voltage Input		RL	18	19	ĪNH
$\dot{ heta}$	Velocity Output -					
	dc analog voltage proportional to		FIGURE 6	HSD1510/HR	RD1510 Pin .	Assignment
	rotational speed of the input shaft angle.					
	Output is referenced to bias voltage (V)					
		ĪNĦ		it functio		
V	Bias Voltage -					e tracking process
	Internally regulated reference voltage					olds the digital
	serves as reference ground for all analog		•			ta read-out. For
	outputs.					his pin may be left
	<b>-</b>				Internal	pull-up will apply
е	Error Voltage -		VL to	the pin.		
	ac analog voltage proportional to	C.D.	0			
	instantaneous tracking error of the	СВ		erter bus		
	Converter.					irs for every 1 LSB
	Output is referenced to bias-voltage (V)		cnang	ge in the	output. (	Output data can be

## Analog Outputs: -

-E

The analog outputs available from the 1510 converters are e (pin 4), -E (pin 13),  $\theta$  (pin 15) and are referenced to bias voltage (V). The bias voltage V (pin 3) is equal to  $\frac{1}{2}$  (+15 V - 0.7). For main power supply voltage of +15 V-dc, the bias voltage is 7.15 V-dc.

Amplified, filtered dc null voltage -

Output is referenced to bias voltage (V)

- e is an ac voltage proportional to error voltage  $\sin (\theta \phi)$  where  $\theta$  is input angle and  $\phi$  is the digital output angle. 60 mV-rms error voltage corresponds to an error of +1 LSB (0.35 degree).
- is filtered dc voltage proportional to (θ φ). A -1 V-dc voltage corresponds to an error of +1 LSB (0.35 degree).
- is a dc voltage proportional to the velocity of the input shaft angle (and output digital angle). The voltage goes positive for increasing digital angle and goes negative for decreasing digital angle. A +1 V-dc signal corresponds to +23 rps for 400 Hz models and +4.6 rps for 60 Hz models.

Scaling of all analog outputs is independent of main-power supply voltage between 11 V-dc and 17 V-dc. Also all analog outputs are operational amplifier outputs and have a drive capability of 1 mA.

The analog outputs e, -E and  $\dot{\theta}$  are by-products of the technique used in mechanizing the conversion process and are made available. They are not closely controlled or characterized functions.

transferred at the trailing edge of the CB

pulse. When converter output is not

changing CB is at logic "low."

If a bipolar signal is required for any analog output a difference circuit, as shown in figure 7, may be used. The output can be scaled to a desired value by selecting the gain of the circuit. Also if reverse polarity output is desirable, the bias and signal connections to the difference amplifier should be reversed.

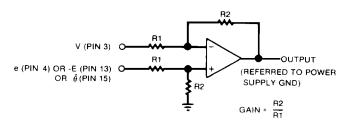


FIGURE 7 Difference Circuit for Bipolar Analog Outputs

# Specifications -

PARAMETER	VALUE		REMARKS		
Digital Output Resolution	10-bits (21 arc-minutes)		MSB = 180 degrees LSB = 0.35 degree		
Accuracy	±21 arc-minutes		Accuracy applies over operating temperature range and includes hysteresis		
Reference Input					
Voltage	4 to 130 V-rms				
Frequency	360 to 1000 Hz 47 to 1000 Hz		400 Hz Models 60 Hz Models		
Input Impedance	200 kΩ Single Ended 400 kΩ Differential				
Common Mode Range	±250 V peak maximum		dc plus recurrent ac peak		
Synchro/Resolver Inputs					
Input Voltages (Line-to-Line)	11.8 V-rms 26 V-rms 90 V-rms		Accuracy of the converter is maintained with $\pm 10\%$ variation in signal voltages		
Input Impedance	Differential 60 k $\Omega$ 150 k $\Omega$ 500 k $\Omega$	Line-to-GND 30 kΩ 75 kΩ 250 kΩ	11.8 V-rms L-L models 26 V-rms L-L models 90 V-rms L-L models		
Impedance Unbalance	0.1% maximum		For all models		
Common Mode Range	± 30 V peak ± 60 V peak ±180 V peak		11 8 V-rms models 26 V-rms models 90 V-rms models		
Common Mode Rejection Ratio	70 dB minimum		dc to 1000 Hz		
Harmonic Distortion	10% maximum		Without degradation in accuracy specification		
INH Function			CMOS transient protected		
Voltage Levels Logic "0" Logic "1"	-0 3 V-dc to 0 8 V-dc 2.4 V-dc		For V <sub>L</sub> = 5 V-dc		
Logic "0" Logic "1"	-0.3 V-dc to 0.3 V <sub>L</sub> 0.7 V <sub>L</sub> to V <sub>L</sub>		For V <sub>L</sub> = 15 V-dc		
Input Current	-15 μA typical, "active ' pui	I-up to power supply (V <sub>L</sub> )	When not used, may be left unconnected		
INH Input Control	Logic "0" Logic "1"		Converter tracking process inhibited Converter tracking analog input signals		
Digital Outputs					
Logic Type	TTL/CMOS compatible		Depends on logic supply voltage (V <sub>L</sub> )		
Drive Capability					
Data Bits (B1-B10) CB	2 Standard TTL Loads 2 Standard TTL Loads		For 5 V-dc logic supply voltage (V <sub>L</sub> )		
Data Bits (B1-B10) Natural Binary Angle		-	Positive Logic		
Logic "0" Logic "1" (2µsec pulse for every LSB change)		3 change)	Output angle not changing Output angle changing (Leading edge initiates output change)		
Analog Outputs			Typical Values unless otherwise specified		
V (Bias Voltage)	(+15 V-0.7)/2		+7.15 V-dc for +15 V-dc main power supply		
e (ac Error)	60mV-rms per +1LSB		ac voltage referenced to V		
-E (dc Error)	-1 V-dc per + 1LSB		dc voltage referenced to V		
$ ilde{ heta}$ (Velocity Output)	43mV-dc per rps 217mV-dc per rps		400 Hz models 60 Hz models		
Drive Capability	1 mA maximum		All analog outputs		

PARAMETER	VALUE	REMARKS		
Dynamic Characteristics		Typical values unless otherwise specified		
Maximum Tracking Rate	±100 rps (36,000° per sec) minimum ± 20 rps ( 7,200° per sec) minimum	400 Hz models 60 Hz models		
Maximum Acceleration	4,000,000°/sec² 175,000°/sec²	400 Hz models 60 Hz models		
Acceleration for 1 LSB error	80,000°/sec² 3,500°/sec²	400 Hz models 60 Hz models		
Settling Time to 1 LSB (for 179° step change)	25 msec 140 msec	400 Hz models 60 Hz models		
Settling Time to 1 LSB (small signal step≤10°)	10 msec 50 msec	400 Hz models 60 Hz models		
Power Supplies				
Main Power Supply (+15 V)				
Voitage 11 V-dc to 17 V-dc		Without degradation in accuracy specification		
Current	15 mA typical 25 mA maximum	For +15 V-dc power supply		
Logic Voltage (V <sub>L</sub> )				
Voltage	4.5 V-dc to main power supply	5 V-dc ± 10% for TTL compatible output		
Current	1 mA maximum 3 mA maximum	For 5 V-dc logic supply For 15 V-dc logic supply		
Physical Characteristics				
Туре	36 PIN Double DIP			
Size	0.78 x 1.9 x 0.21 inch (20 x 48 x 5 3 mm)	3 standoffs are added to the package to insulate it from printed circuit board traces (standoffs included in 0.21 inch height dimension)		
Weight	0.6 oz (17 g) max			

Model 1510 converter uses thin-film resistors (as compared to screened thick-film resistors), thereby allowing flexibility of design changes. Non-standard voltages, frequency, dynamic requirements, etc. can be accommodated with minor modifications, often, without any additional costs.

If your application requires non-standard input or output characteristics, contact a Natel Applications Engineer or sales department.

# Absolute Maximum Ratings -

Signal Inputs	
Reference Input	
Main Power Supply	5 V)
Logic Voltage (V <sub>L</sub> ) .	+4.5 V-dc to +15 V supply
Digital Inputs	0.3 V-dc to V <sub>L</sub>
Storage Temperature	65° C to +135° C

When installing on or removing the converter from printed circuit boards or sockets, it is recommended that the power supplies and input signals be turned off. Decoupling capacitors are recommended on the main power supply (+15 V) as well as logic voltage ( $V_L$ ). A 1  $\mu F$  tantalum capacitor in parallel with 0.01  $\mu F$  ceramic capacitor should be mounted as close to the supply pins (2 and 32) as possible.

# **Dynamic Performance**

The 1510 design incorporates the proven Type II tracking design (KV=∞) and has been configured to provide superior dynamic performance independent of power supply voltage over the range of 11 V-dc to 17 V-dc.

The converter will track the input angles up to specified tracking rates (see specifications, pages 4 and 5) with no lag error. The acceleration constant (KA) for the converter is 265,000°/sec². Both small and large signal response for the Model 1510 are shown in figure 10.

The Large Signal transient response is dependent solely on the maximum velocity ( $\omega$ max) and the maximum acceleration ( $\alpha$ max) of which the converter is capable. The large signal parameters are defined in figure 8. The synchronizing time (tsync) for large signals can be partitioned into three distinct intervals. Acceleration time (tacc) Slew time (tslew) and Overshoot time (tos).

Acceleration time is the time interval from application of the step-input to the point at which the converter reaches its maximum velocity.

Slew time is the time interval from the point at which maximum velocity is obtained to the point at which the output angle is first equal to the input angle.

Overshoot time is the time interval from the point at which the converter output angle first equals the input angle (and applies constant acceleration in the opposite direction) to the point at which the output angle again reaches the input angle.

At the end of overshoot time, the small signal response becomes dominant and the converter will settle to the final value according to its small signal transient response function.

The **Small Signal** settling time (t<sub>S</sub>) is specified for step inputs of less than 10 degrees. For small signal steps, the settling time is a function of the transient response of the converter. The transfer functions for both 60 Hz and 400 Hz models are shown in figure 9.

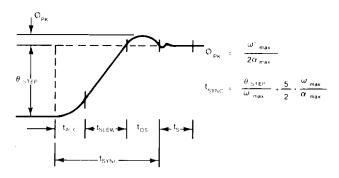


FIGURE 8 Large Signal (≥10°) Response Parameters

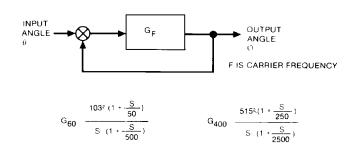


FIGURE 9 Transfer Functions for 1510

# Small Signal Input Step = 5.6 Degrees

# Ontput Angle (Degrees) SMALL SIGNAL STEP RESPONSE 60 Hz Model O 20 40 60 80 100 TIME (ms) SMALL SIGNAL STEP RESPONSE 400 Hz Model O 4 8 12 16 20 TIME (ms)

# Large Signal Input Step = 179 Degrees

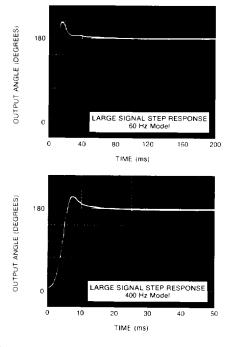


FIGURE 10 Dynamic Characteristics

## Testing Synchro (Resolver)-to-Digital Converters

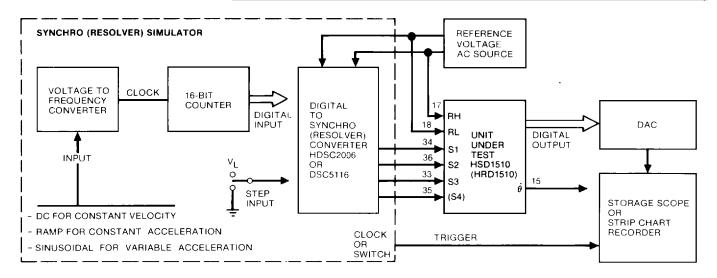


FIGURE 11 Dynamic Characteristics Test Configuration

All Model 1510 converters are guaranteed to meet the specifications described in the data sheet. All converters are 100% tested for their specifications (except for design parameters) at the factory. A copy of the data sheet with a record of the static accuracy test is supplied with each unit. (A test set-up for measuring static accuracy is described in the Natel HSD/HRD1014 data sheet) In addition dynamic testing may be performed by using test set-ups of figures 11 and 12. Figure 11 shows a simple test set-up for measuring settling times, maximum tracking rate, velocity output, maximum acceleration and acceleration constant. The digital-to-synchro (resolver) converter accuracy is not critical and this test set-up requires minimal test equipment for verifying the transfer function of the model 1510. Use of a digital-to-synchro (resolver) converter offers a convenient method for simulating a step input or a constant velocity or a constant acceleration input for analog signals. The digital input for D/S can be a simple ON/OFF switch for step input or a voltageto-frequency converter plus a counter for simulating variable input signals.

Figure 12 shows another test set-up for measuring dynamic characteristics of a Synchro (Resolver)-to-Digital converter. This method is best suited for measuring accuracy of the converter under dynamic conditions. Under static conditions the error output "e" (pin 4 of model

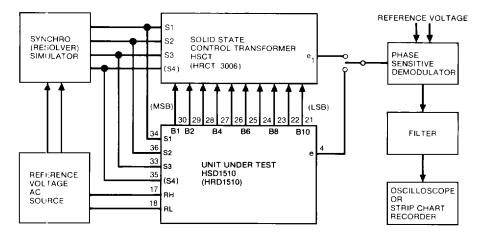
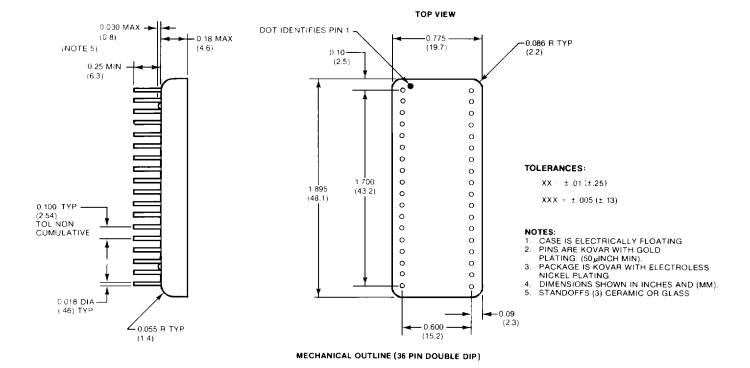


FIGURE 12 Dynamic Lag Test Configuration

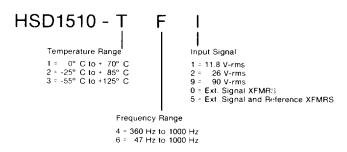
1510) of the converter under test is zero (except for converter hysteresis). Under dynamic conditions the error output is proportional to the dynamic lag of the converter. Note that synchro simulator inaccuracy will affect the measurement of dynamic lag. Therefore, the synchro simulator used must have an accuracy of at least 5 times (preferably 10 times) better than the required accuracy of the parameters being measured.

The synchro (resolver)-to-digital converter error can also be measured by applying synchro (resolver) input signals and digital outputs to a solid state control transformer (SCT) as shown in figure 12. The error output "e<sub>1</sub>", of

the SCT is a measure of the accuracy of the converter under test. The output "e<sub>1</sub>", is proportional to the sum of the static and dynamic errors of the converter under test. Note that with this method, the inaccuracy of the synchro (resolver) simulator is not critical but the accuracy of the SCT is important and must be at least 5 times better than the unit under test. If the required equipment is not available arrangements may be made with Natel for source inspection at our facilities. Also if you require more details for the test circuits contact one of our applications engineers.







SPECIFY HRD 1510 FOR RESOLVER INPUT

# MIL-STD-883 COMPLIANT HYBRIDS AVAILABLE Contact Natel Engineering for Delivery

# Other Hybrid products in 36 pin DDIP size:

- 16-bit microprocessor-compatible synchro/resolver-todigital converter, with 3 state output, operating from a single +5-V power supply (HSRD1006)
- 16-bit microprocessor-compatible digital to synchro/ resolver converter with double buffered inputs and 1 arc-minute accuracy (HDSR2006).
- 14-bit synchro (resolver)-to-digital converters pin-compatible with existing designs, but with superior performance (HSD/HRD1014)
- 14-bit digital-to-synchro/resolver converter that is pin-compatible with existing designs with transformation and angular accuracy improvement of a factor of 2 to 4 (HDSR2504)
- 14/16-bit synchro (resolver) control transformer with 1 arc minute accuracy (HSCT/HRCT3006)

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

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