Version	3.1
Total pages	19
Date	2009/03/18

Product Specification

8″ color TFT-LCD module

MODEL NAME: C080VW02 V0

Part No : 97.08C02.001

( ) Draft Specification
( ) Preliminary Specification
(◆) Final Specification

Note: The content of this specification is subject to change without prior inform

Record of Revision

Version	Revise Date	Page	Content
0.0	2007/08/01	0	First draft.
1.0	2008/03/03	4,5,8	Modified LED driving current
2.0	2008/08/25	3.4.5	Updated Pin assignment Description: modify Pin6 & 42 description, and add Note1~3 description
		7	Update Timing conditions for DCLK frequency, DCLK cycle time, DCLK pulse width, STV setup time, STV hold time, CKV pulse width, Output stable time
		15	Update Fig2. Operation Mode diagram
		18	Update Fig5. Vertical timing (from up to down) diagram
3.0	2008/11/27	4	Modified OEV Pin (Pin52) Description:
		6	Revised LED IL Absolute Maximum rating: 150mA -> 200mA
		7	Update Timing conditions for: STV(R/L) width, Charging time 1&2, OEV cover CKV time 1&2, Time CKV rising to LD fallling, Time OEV rising to LD falling
		17-19	Update Fig4.Vertical timing, Fig5. Vertical shift clock timing, and Fig6.OEV timing diagram
3.1	2009/03/18	13, 14	Revise the outline drawing of LED cable

Contents:

Appendix:

A. Physical specifications

NO	Item	Specification	Remark
1	Display resolution (dot)	800RGB(W)×480(H)	
2	Active area (mm)	175.20(W)×105.12(H)	
3	Screen size (inch)	8.0(Diagonal)	
4	Pixel pitch (mm)	0.073(W)×3x0.219(H)	
5	Color configuration	R. G. B. stripe	
6	Overall dimension (mm)	186.5(W)×117.22(H)×5.3(D)	Note 1
7	Weight (g)	180 +/- 10%	
8	Surface treatment	AG with SWV film	
9	Backlight unit	LED	

Note 1: Refer to Fig.1 outline dimension drawing

B. Electrical specifications

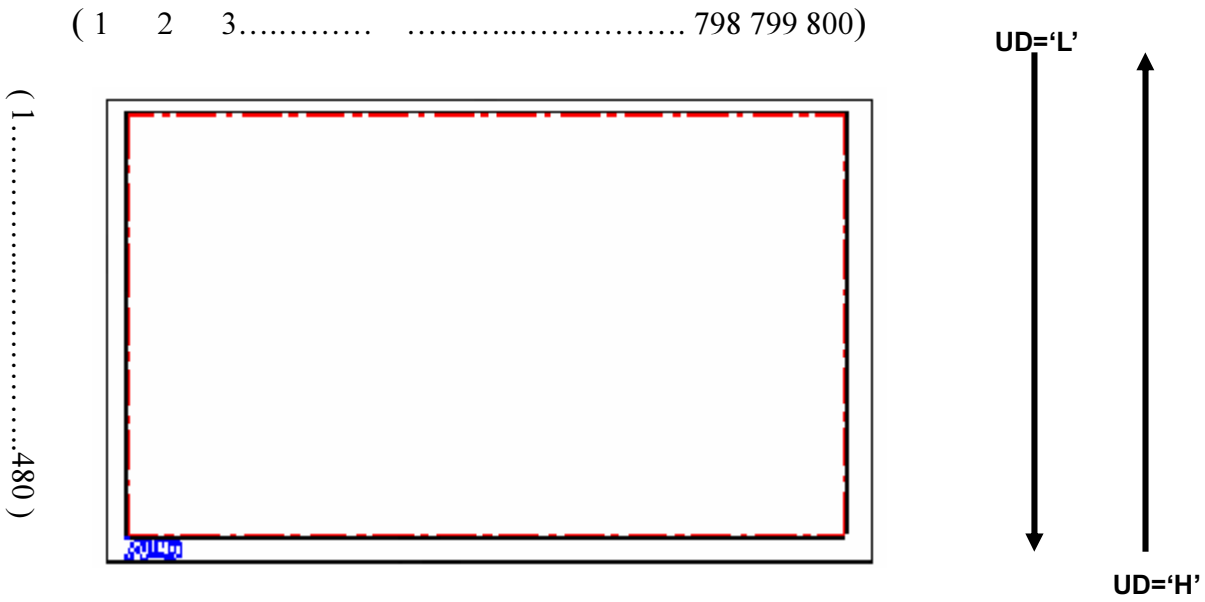
1. Pin assignment

a.) TFT-LCD panel driving section

Pin no	Symbol	I/O	Description	Remark
1	GND	P	Power ground	
2	VCOM	I	Common voltage	
3	DIO1	I/O	Horizontal start pulse signal input or output	Note 1
4	GND	P	Power ground	
5	VCC(DVDD)	P	Voltage for digital circuit	
6	EDGSL	I	Select raising edge or raising/falling edge When EDGSL = "0", Latching source data onto the line latches at the rising edge. When EDGSL = "1", Latching source data onto the line latches at the rising edge and falling edge.	
7	DCLK	I	Pixel clock	
8	LR	I	Right or Left display control	
9	R0	I	Red data	
10	R1	I	Red data	
11	R2	I	Red data	
12	R3	I	Red data	
13	R4	I	Red data	
14	R5	I	Red data	
15	G0	I	Green Data	
16	G1	I	Green Data	
17	G2	I	Green Data	
18	G3	I	Green Data	
19	G4	I	Green Data	
20	G5	I	Green Data	
21	AVDD	P	Analog voltage for source driver	
22	V1	I	Gamma correction reference voltage	
23	V2	I	Gamma correction reference voltage	
24	V3	I	Gamma correction reference voltage	
25	V4	I	Gamma correction reference voltage	
26	V5	I	Gamma correction reference voltage	
27	V6	I	Gamma correction reference voltage	
28	V7	I	Gamma correction reference voltage	
29	V8	I	Gamma correction reference voltage	
30	V9	I	Gamma correction reference voltage	
31	V10	I	Gamma correction reference voltage	
32	V11	I	Gamma correction reference voltage	
33	V12	I	Gamma correction reference voltage	
34	V13	I	Gamma correction reference voltage	
35	V14	I	Gamma correction reference voltage	
36	AVSS	P	Analog ground for source driver	
37	B0	I	Blue Data	
38	B1	I	Blue Data	
39	B2	I	Blue Data	

40	B3	I	Blue Data	
41	B4	I	Blue Data	
42	B5	I	Blue Data	Note 1
43	LD	I	Latch and switch data to output	Note 2
44	REV	I	Control Whether RGB data are inverted or not When “REV” = 1 these data will be inverted. Ex. “00”→”3F”, “07”→”38”, and so on.	
45	POL	I	Polarity selection	Note 3
46	VCC(DVDD)	P	Voltage for digital circuit	
47	GND	P	Power ground	
48	CHNSL	I	Select source channel output number (Must set to High)	
49	AVDD	P	Analog voltage for source driver	
50	DIO2	I/O	Horizontal start pulse signal input or output	Note 1
51	VCOM	I	Common voltage	
52	OEV	I	Output enable, active low. The gate driver outputs are disable when OEV = “H”.	
53	UD	I	Up or Down display control	
54	CKV	I	CLK (Vertical)	
55	STVU	I/O	Start pulse signal input/output (Vertical)	Note 1
56	STVD	I/O	Start pulse signal input/output (Vertical)	Note 1
57	VGH	P	TFT high voltage	
58	VGL	P	TFT low voltage	
59	VCC(DVDD)	P	Voltage for digital circuit	
60	GND	P	Power ground	

Note 1:



UD	STVU	STVD	Direction
L	Input	Output	U→D
H	Output	Input	D→U

LR	DIO1	DIO2	Direction
H	Input	Output	L→R
L	Output	Input	R→L

Note 2: LD

Latches the polarity of outputs and switches the new data to outputs.

1. At the rising edge, latches the "POL" signal to control the polarity of the outputs.
2. The pin also controls the switch of the line registers that switches the new incoming data to outputs.

Note 3: POL

"POL" value is latched at the rising edge of "LD" to control the polarity of the even or odd outputs.

POL=1: Even outputs range from V1 ~ V7, and Odd outputs range from V8 ~ V14

POL=0: Even outputs range from V8 ~ V14, and Odd outputs range from V1 ~ V7

b). Backlight driving section

No.	Symbol	I/O	Description	Remark
1	HI	I	Power supply for backlight unit (High voltage)	--
2	GND	-	Ground for backlight unit	--

2. Absolute Maximum Ratings

Items	Symbol	Product Specification			Unit
		Min.	Typ.	Max.	
Power Voltage	Vcc	-0.5		5	V
	AVDD	-0.5		12	V
	VGH	-0.3		18	V
	VGL	-15		0.3	V
	VGH-VGL			33	V
Input Signal Voltage	Vi	-0.3		Vcc+0.3	V
	Vref(V1~V7)	0.4AVDD		AVDD+0.3	V
	Vref(V8~V14)	-0.3		0.6AVDD	V
	VCOM		4.16		V
Operating Temperature	Topa	-30		85	□
Storage Temperature	Tstg	-40		85	□
LED	VL			--	V
	IL			200	mA

Note 1 : The LED Tj temperature should never exceed 125°C if the IL is larger than 150mA

Note 2 : The lifetime(10,000 hours continuous use) is base on IL=150mA(Typical) under +25°C room temperature.

3. Typical operating conditions (GND=AVSS=0V)

Items	Symbol	Product Specification			Unit
		Min.	Typ.	Max.	
Power Voltage	VCC	3.0	3.3	3.6	V
	AVDD	9.7	9.8	9.9	V
	VGH	14.0	15.0	16.0	V
	VCOM	4.0	4.2	4.4	V
	VGL	-11	-10	-9	V
Input Reference Voltage	V1~V7	0.4AVDD	—	AVDD-0.1	V
	V8~V14	0.1	—	0.6AVDD	V
Input H/L level Voltage	VIH	0.8VCC	—	VCC	V
	VIL	0	—	0.2VCC	V

4. Current consumption conditions(GND=AVSS=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current For Driver	IGH	VGH=15V		100	150	uA
	IGL	VGL=-10V		-100	-150	uA
	ICC	VCC=3.3V		3.5	5	mA
	IDD	AVDD=9.8 V		20	30	mA

5. Backlight driving conditions

Parameter	Symb	Min.	Typ.	Max.	Unit	Remark
LED current	I_L		150		mA	Single
LED voltage	V_L		20	22	V	Single
LED LifeTime	L_L	10000			Hrs	

6. Timing conditions

AC Electrical Characteristics (VCC=3.3V, AVDD=9.8V, AVSS=GND=0V, TA=25□)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency (EDGSL = '0')	Fclk		33	40	MHz
DCLK frequency (EDGSL = '1')	Fclk		16.5	20	MHz
DCLK cycle time	Tcph	25	30		ns
DCLK pulse width	Tcw	30%		70%	Tcph
Data set-up time	Tsu	4			ns
Data hold time	Thd	2			ns
Propagation delay of DIO2/1	Tphl	6	10	15	ns
Time that the last data to LD	Tld	1			Tcph
Pulse width of LD	Twld	2			Tcph
Time that LD to DIO1/2	Tlds	5			Tcph
POL set-up time	Tpsu	6			ns
POL hold time	Tphd	6			ns
STV setup time	T_{SUV}	400			ns
STV hold time	T_{HDV}	400			ns
CKV pulse width	T_{CKV}	500			ns
Output stable time	Tst			15	us
STV(R/L) width (Note.2)	Tstv	-	1	-	Tpckv
Charging time1 (Note.3)	Tch1	20			us
Charging time2 (Note.3)	Tch2	20			us
OEV cover CKV time1	TOEV1	1			Tcph
OEV cover CKV time2	TOEV2	1			Tcph
Time CKV rising to LD falling	TCTL	2			us
Time OEV rising to LD falling	TOTL	2			us

Note 1: Due to panel is a passive component and no leakage current allowed for better performance, it may need extra circuit to make sure the TFT LCD panel storage

capacitor‘s shorter discharge time when system power off. Customers should study the discharge circuit according to system design.

Note.2: Pulse width of STV(R/L) should be set 1 Tpckv (Time period of CKV).

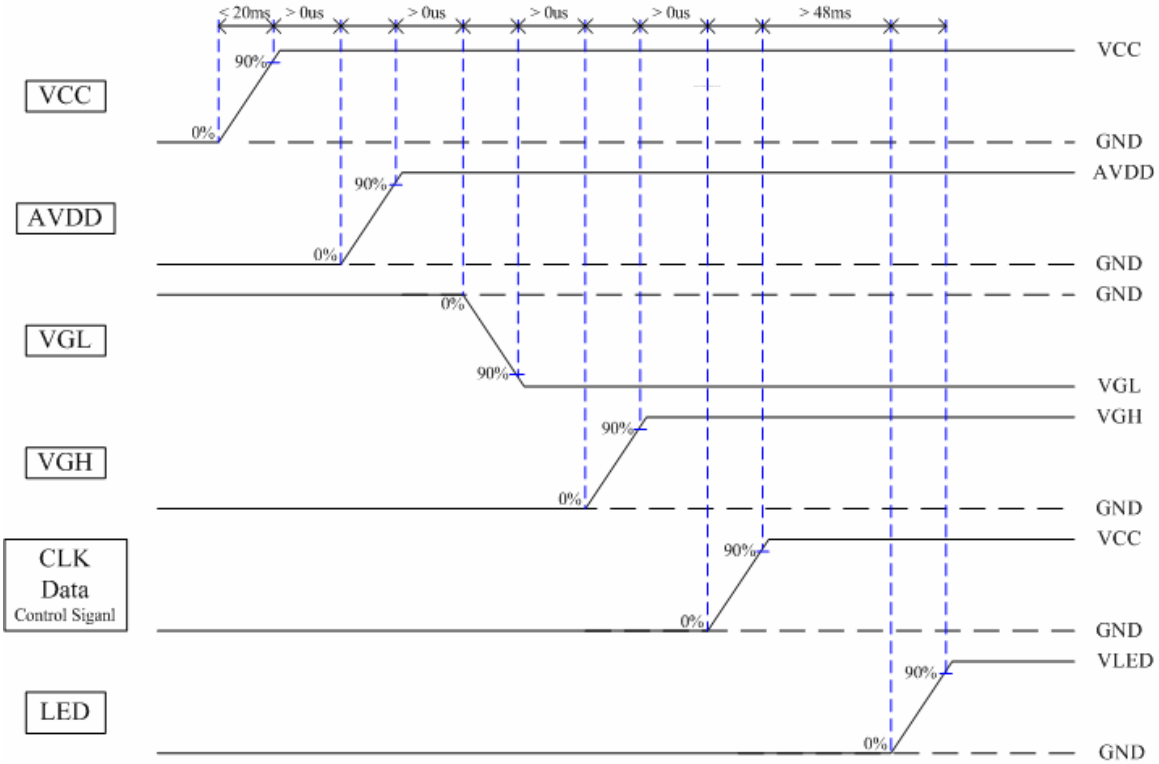
Note.3: If OEV is used, charging time must be followed to Tch1 setting, at least 20 us. Otherwise, if OEV is unused, charging time must be followed to Tch2 setting, at least 20 us.

Note.4: If OEV is used, TOTL(time from OEV rising edge to LD falling edge) should be set more than 2us to prevent panel from displaying wrong data.
If OEV is unused, TCTL(time from CKV rising edge to LD falling edge) should be set more than 2us to prevent panel from displaying wrong data.

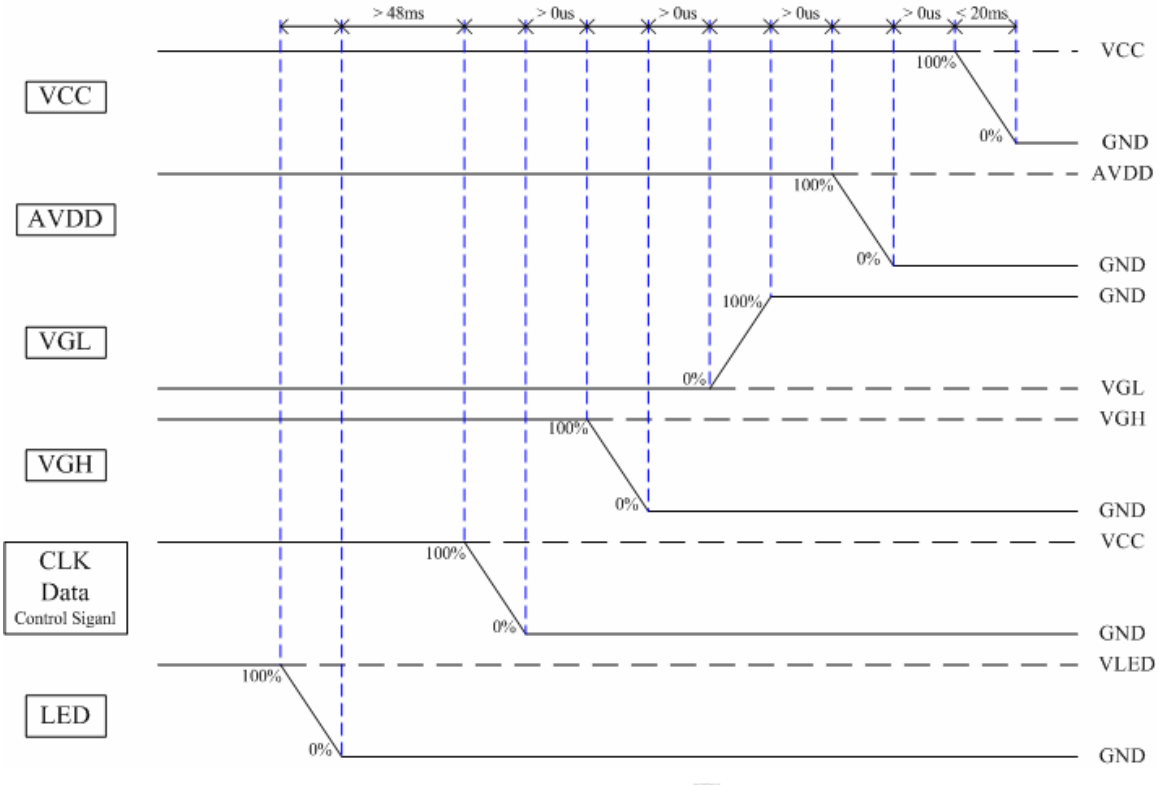
Note.5: If OEV is used, pulse of OEV must cover the rising area of CKV. Therefore, TOEV1 and TOEV2 must be more than 1 Tcph.

7. Power On/Off Sequence

Power On



Power Off



C. Optical specification (Note 1, Note 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise Fall	Tr Tf	θ=0°	- -	15 20	50 60	ms ms	Note 3
Contrast ratio		CR	At optimized Viewing angle	200	300	-		Note 4
Viewing angle	Top Bottom Left Right		CR□10	30 50 50 50	40 60 60 60	- - - -	deg.	Note 4
Brightness		Y_L	I_L=150mA, 25□	400		-	nit	Note 5
White chromaticity		x	θ=0°	0.26	0.31	0.36		Note 5
		y	θ=0°	0.28	0.33	0.38		

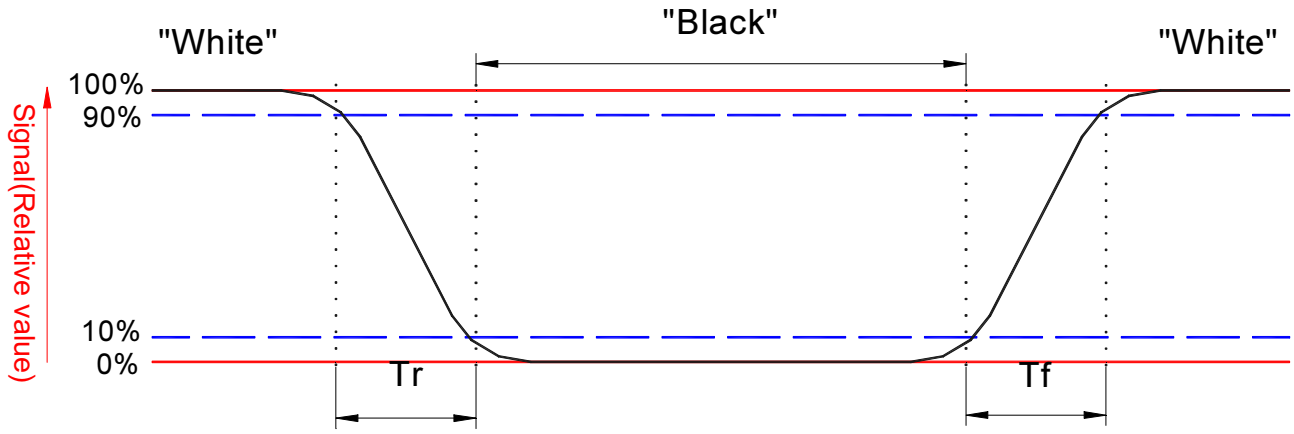
Note 1 : Ambient temperature =25□, and LED current I = 150 mArms. To be measured in the dark room.

Note 2 :To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 3. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

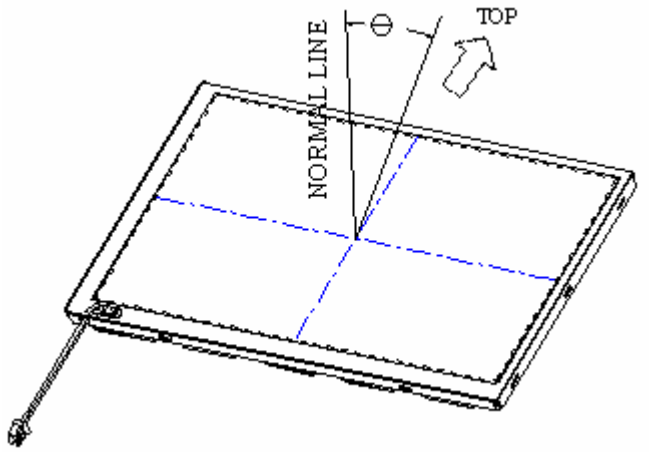


Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 5. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.



D. Reliability test items(Note 2):

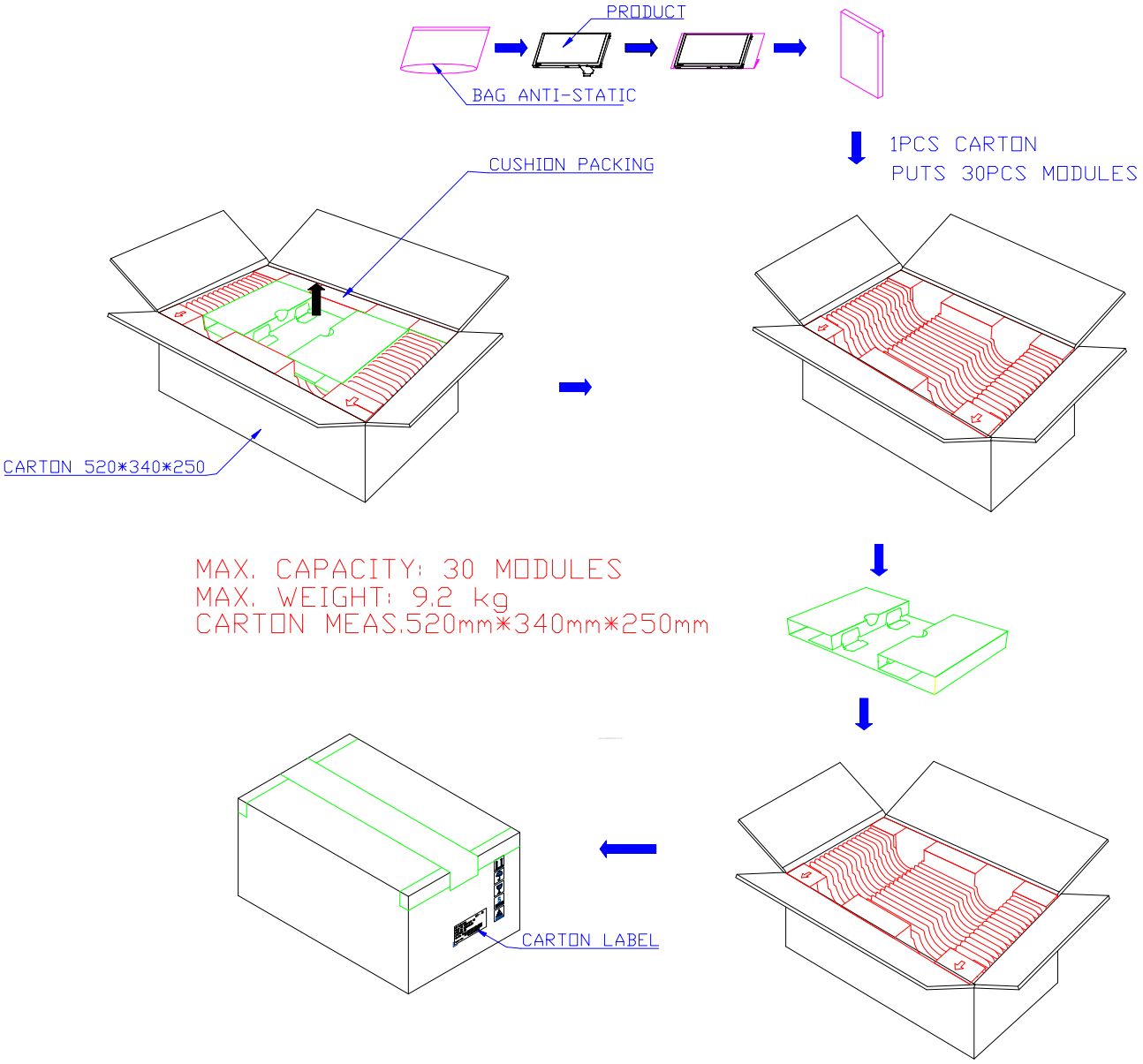
No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 95□ 240Hrs	
2	Low temperature storage	Ta= -40□ 240Hrs	
3	High temperature operation	Tp= 85□ 240Hrs	
4	Low temperature operation	Ta= -30□ 240Hrs	
5	High temperature and high humidity	Tp= 60□, 90% RH 240Hrs	Operation
6	Heat shock	-30□~85□/200 cycles 1Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 8~33.3Hz Stoke : 1.3mm Sweep : 2.9G, 33.3 ~ Cycle : 15 minutes 2 hours for each direction of X,Z 4 hours for Y direction	JIS C7021, A-10 Condition A
9	Mechanical shock	100G, 6ms, ±X,±Y,±Z 3 times for each direction	JIS C7021, A-7 Condition C
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	JIS Z0202

Note1: Ta: Ambient Temperature.

Note2: Tp: Panel Surface Temperature

Note3: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

E. Packing form



Appendix:

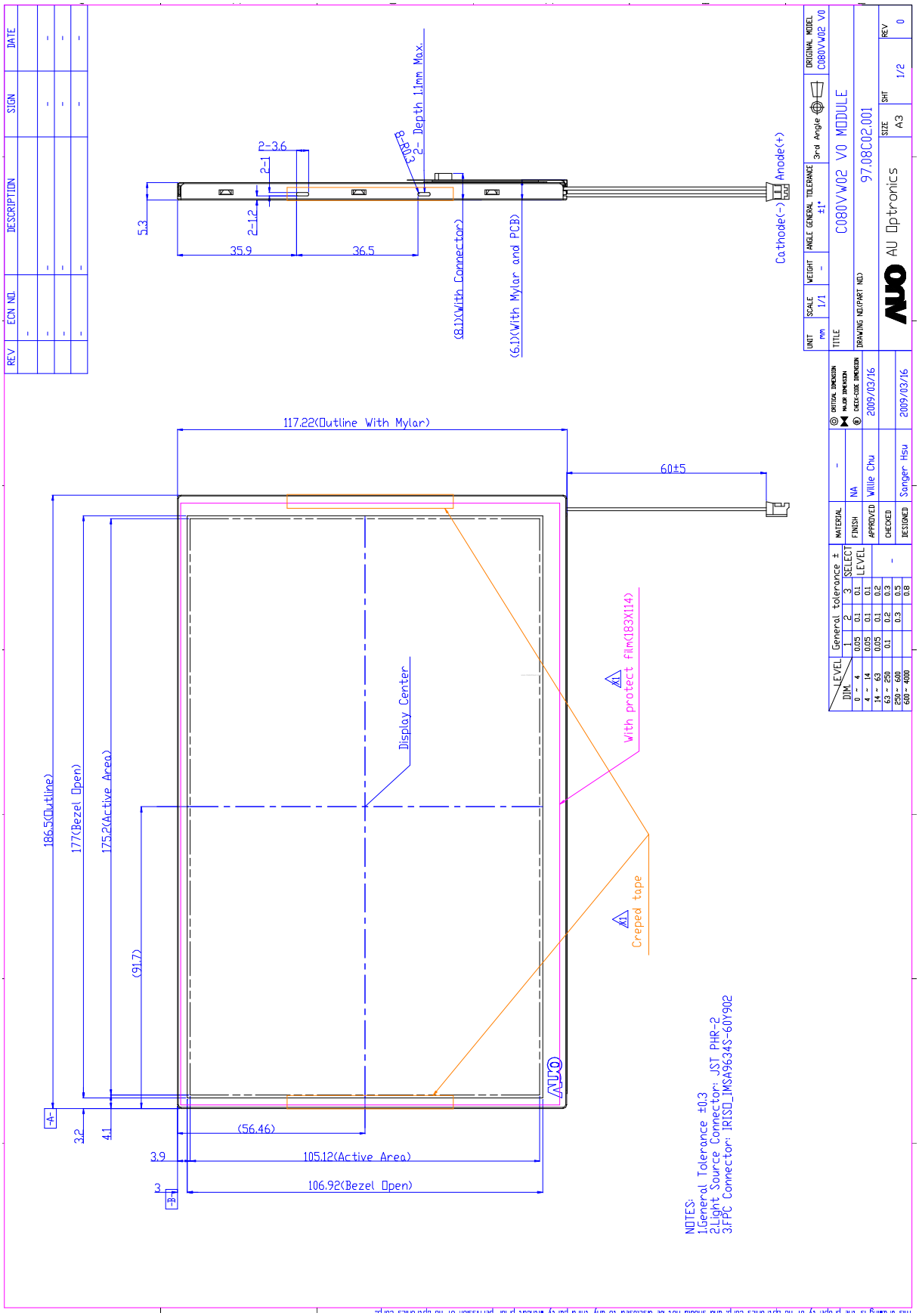


Fig 1-a Outline dimension of TFT-LCD module (Front View)

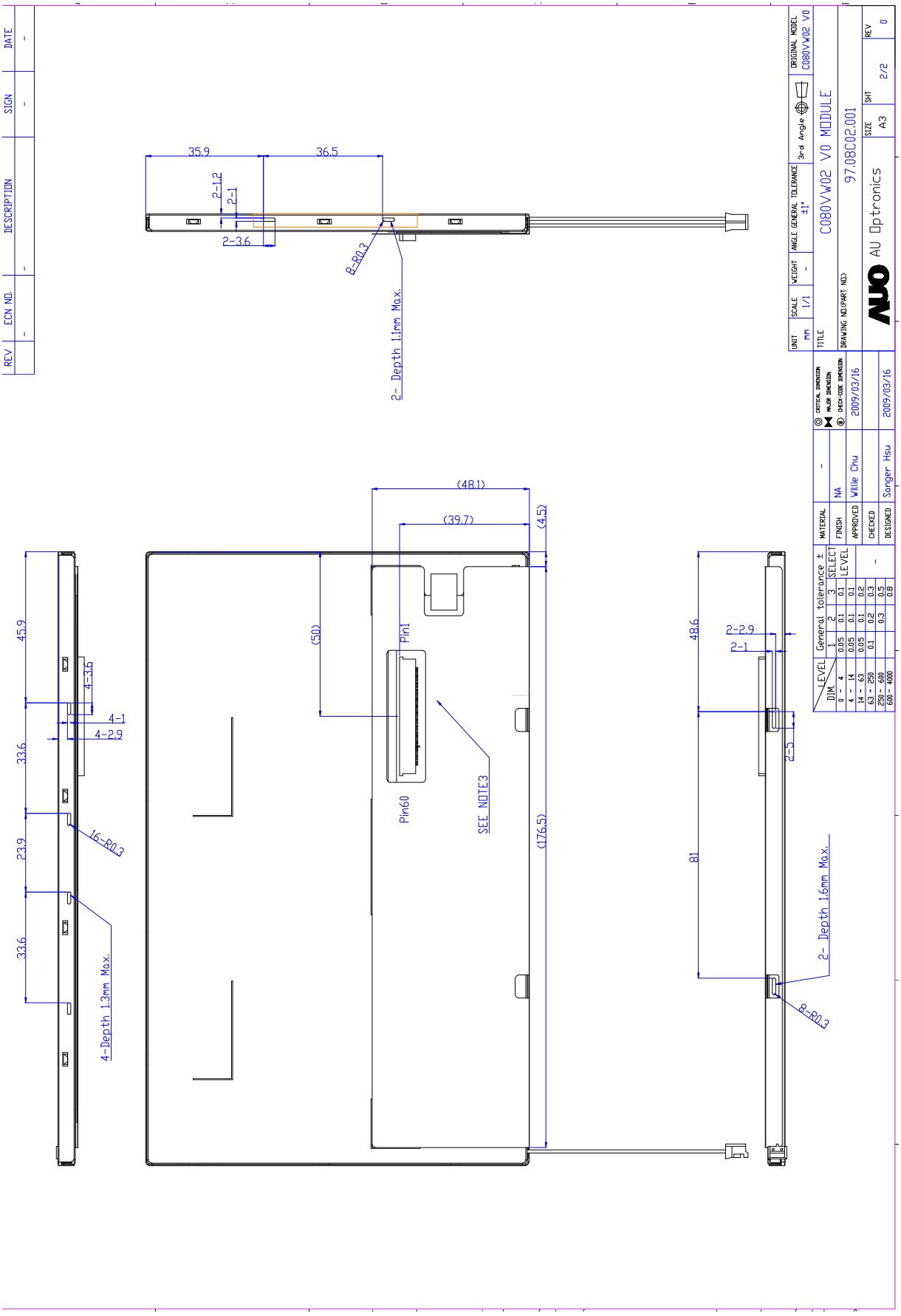


Fig 1-b Outline dimension of TFT-LCD module (Rear View)

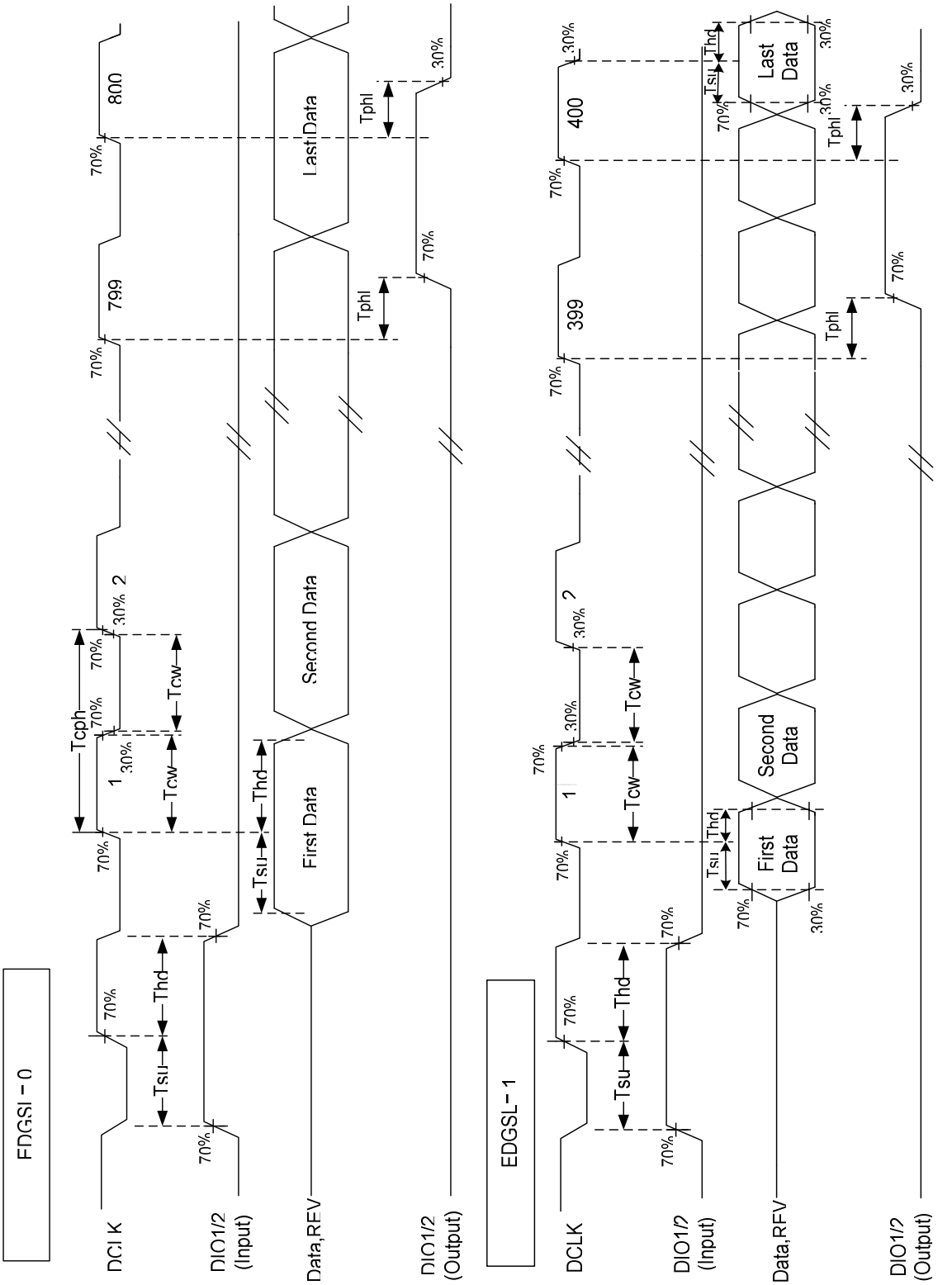


Fig.2 Operation Mode

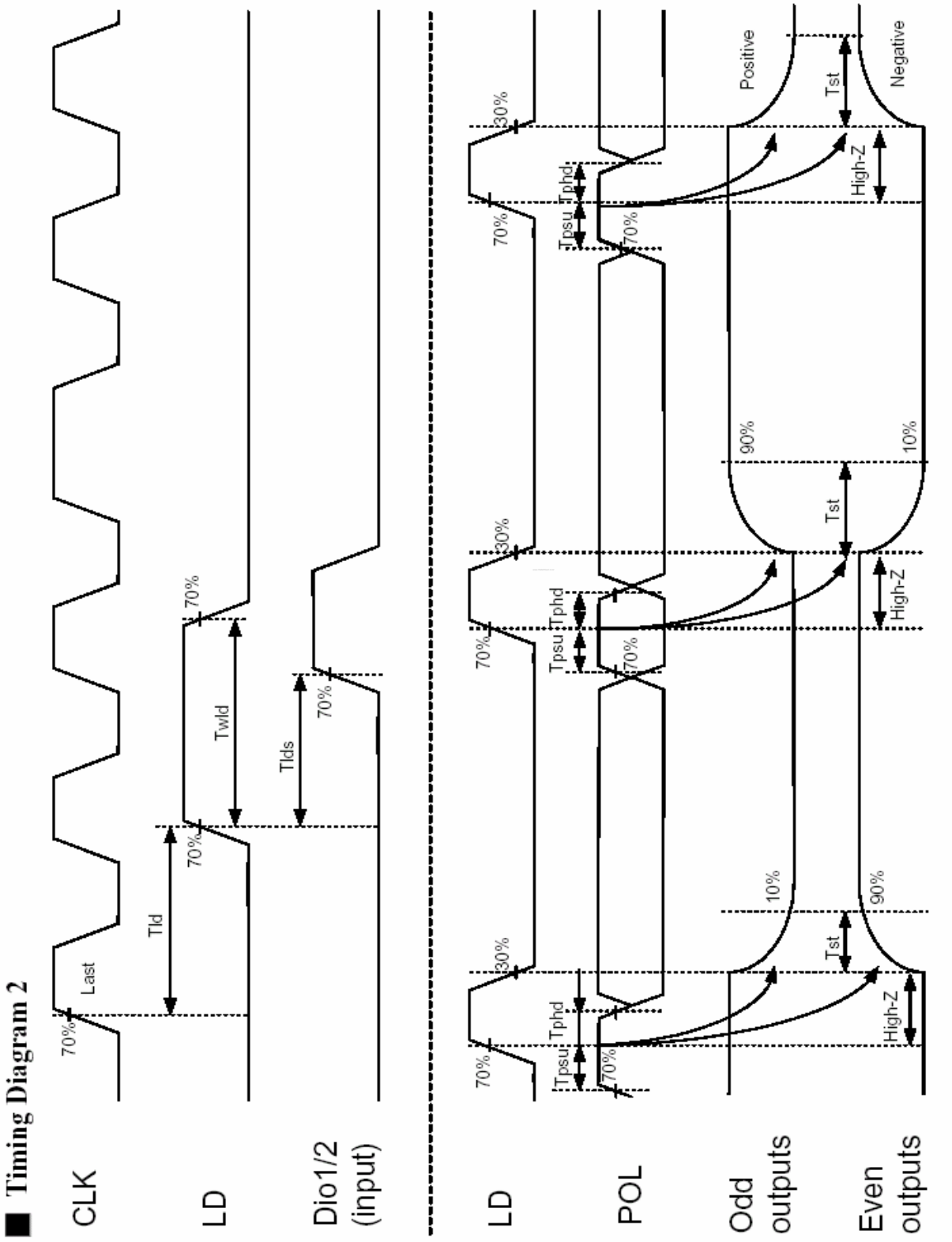


Fig.3 Horizontal timing

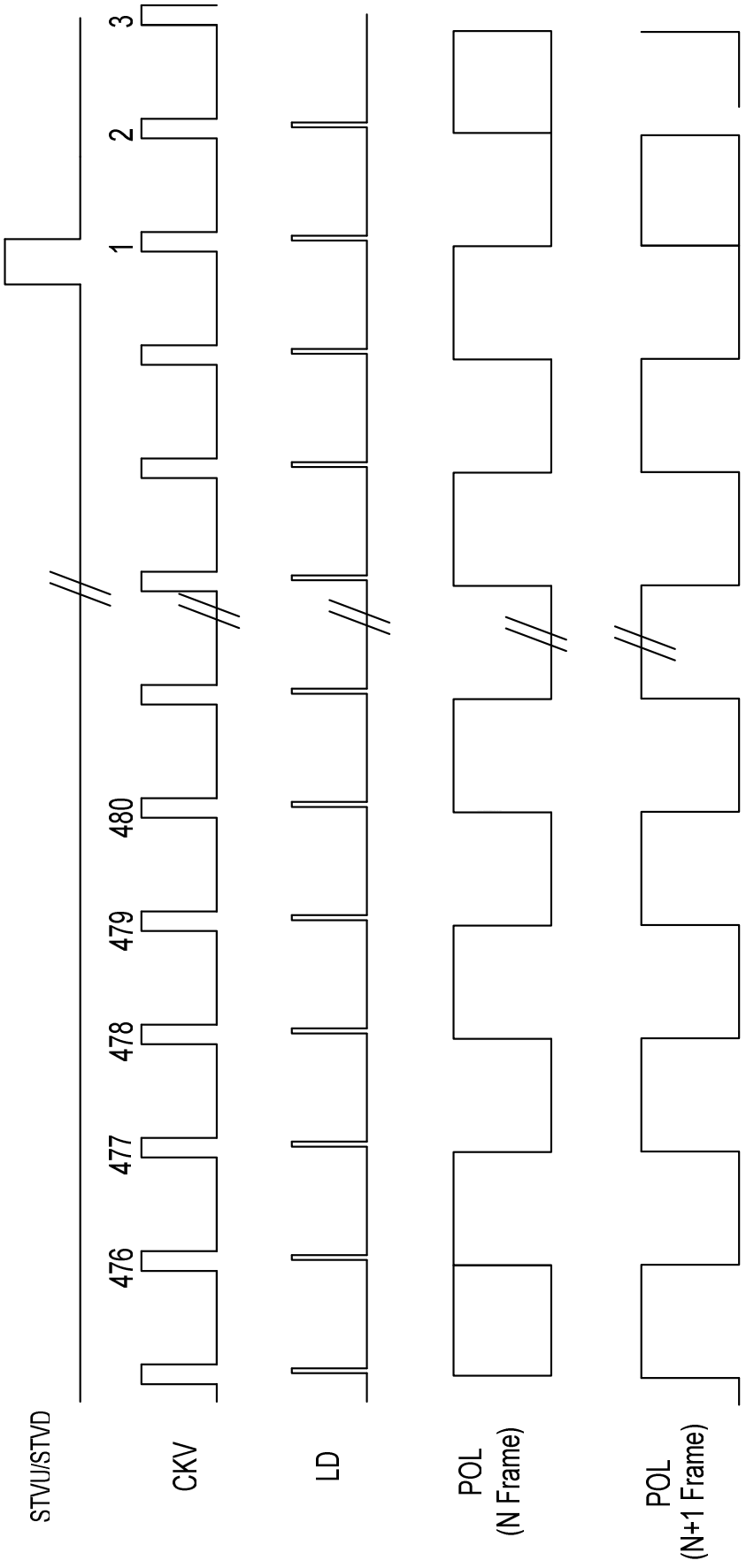


Fig.4 Vertical timing (from up to down)

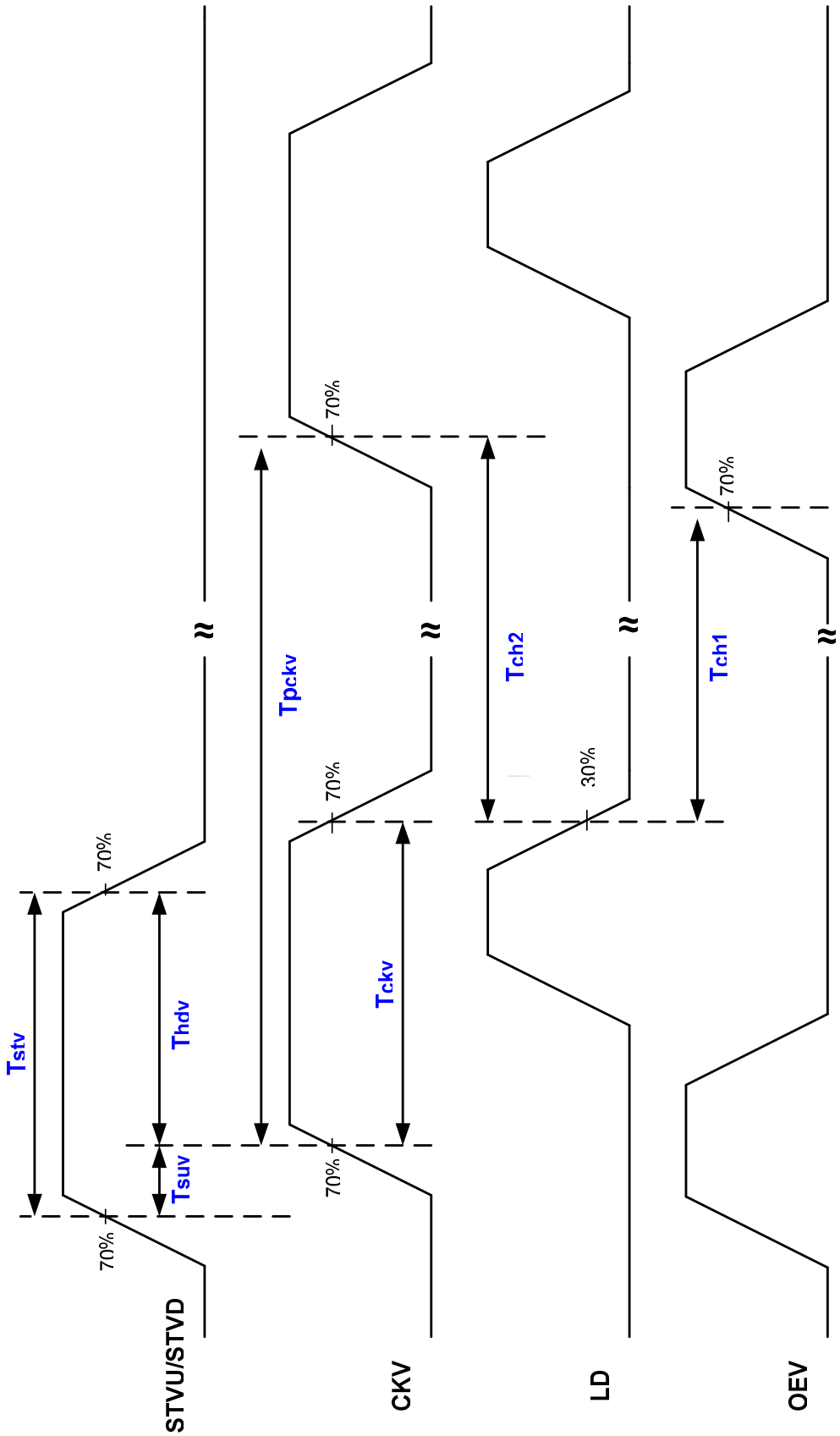


Fig.5 Vertical shift clock timing

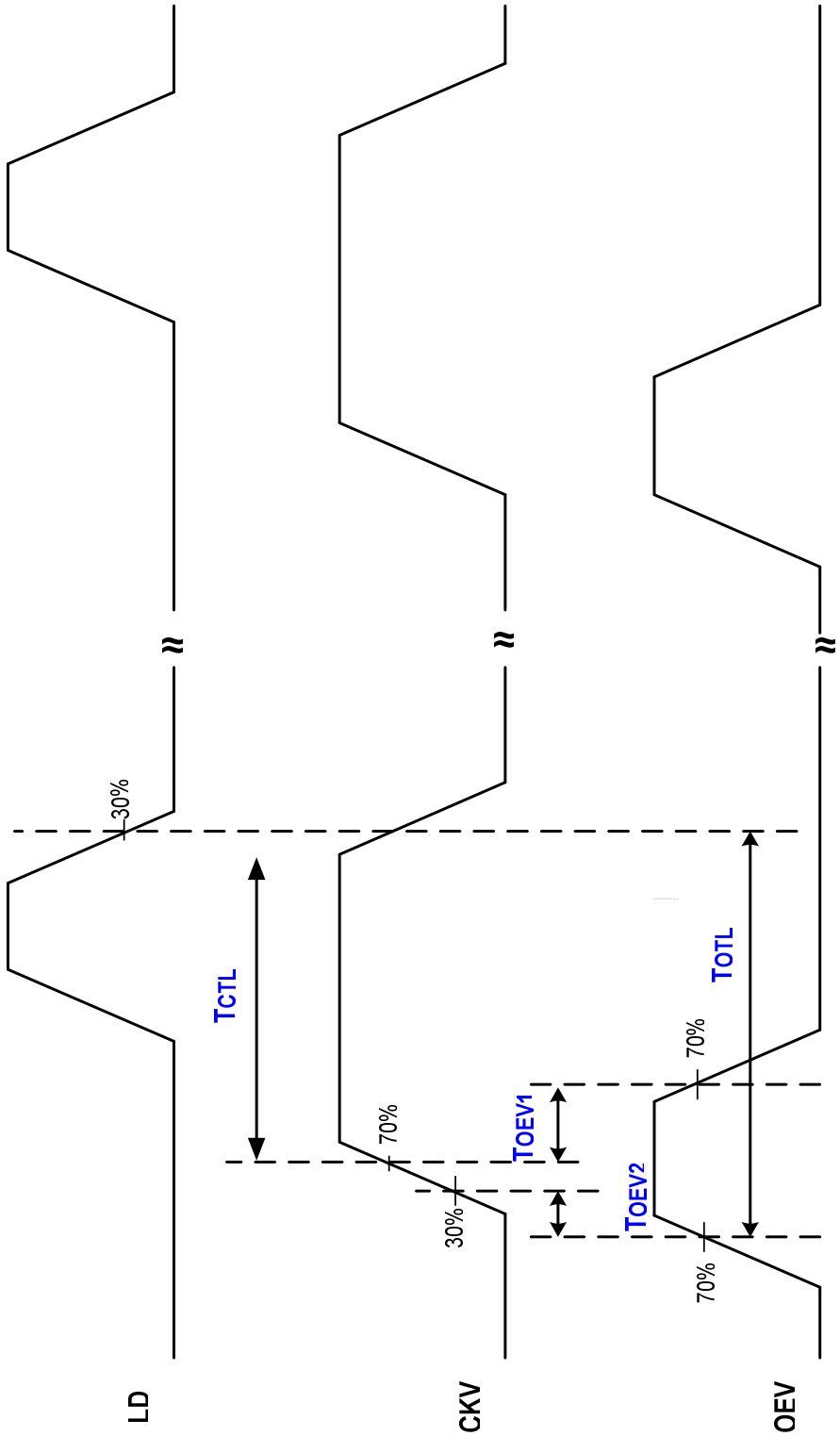


Fig.6 OEV timing

Recommended Gamma Voltage

Gamma 2.2		
	AVDD	9.80
00H	V1	9.7
01H	V2	9.24
10H	V3	7.76
20H	V4	7.37
30H	V5	7.01
3EH	V6	6.30
3FH	V7	5.99
3FH	V8	4.46
3EH	V9	4.08
30H	V10	3.16
20H	V11	2.78
10H	V12	2.29
01H	V13	0.65
00H	V14	0.1