

# DATA SHEET

**74AC38/74ACT38**

Quad 2-input NAND buffer (open drain)

Product specification

1997 Sep 03

# Quad 2-input NAND buffer (open drain)

**74AC38**  
**74ACT38**

## FEATURES

- 74ACT38 has TTL-compatible inputs
- 74AC38 has CMOS-compatible inputs
- Meets or exceeds JEDEC standard standard for 74AC(T)XX family
- Superior ground bounce noise immunity
- Output source/sink 24mA

## DESCRIPTION

The 74AC/T38 provides the 2-inputs NAND function..

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL			UNIT
			AC		ACT	
			V <sub>CC</sub> = 3.3V	V <sub>CC</sub> = 5.0V	V <sub>CC</sub> = 5.0V	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay nA to nY	C <sub>L</sub> = 50pF	3.2	2.2	3.4	ns
C <sub>I</sub>	Input capacitance		4.5			pF
C <sub>PD</sub>	Power dissipation capacitance per gate	V <sub>I</sub> = GND to V <sub>CC</sub> <sup>1</sup>	11		13	pF

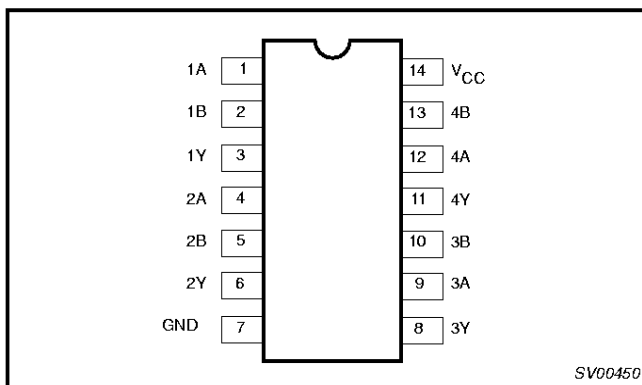
### NOTE:

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz; C<sub>L</sub> = output load capacity in pF;  
 f<sub>o</sub> = output frequency in MHz; V<sub>CC</sub> = supply voltage in V;  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

## ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
14-Pin Plastic SO	-40°C to +85°C	74AC38D 74ACT38D	74AC38D 74ACT38D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to +85°C	74AC38DB 74ACT38DB	74AC38DB 74ACT38DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to +85°C	74AC38PW 74ACT38PW	74AC38PW DH 74ACT38PW DH	SOT402-1

## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data inputs
2, 5, 10, 13	1B to 4B	
3, 6, 8, 11	1Y to 4Y	Data outputs
7	GND	Ground (0 V)
14	V <sub>CC</sub>	Positive supply voltage

# Quad 2-input NAND buffer (open drain)

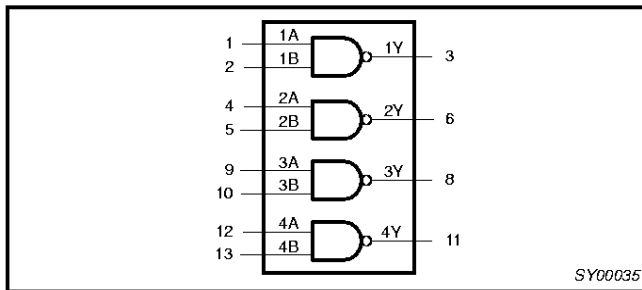
74AC38  
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## FUNCTION TABLE

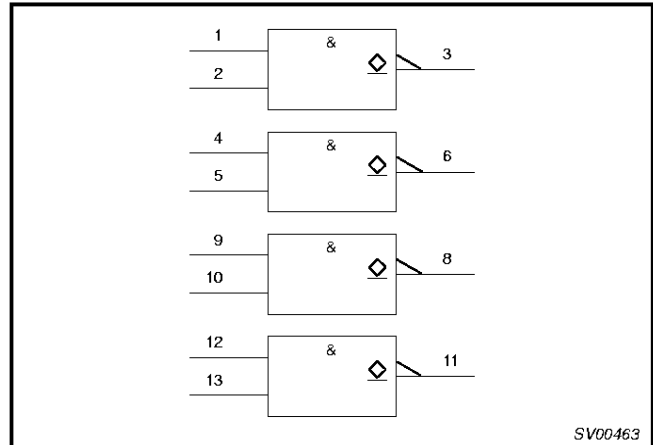
INPUTS		OUTPUT
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

H = HIGH voltage level  
L = LOW voltage level  
Z = High impedance OFF-state

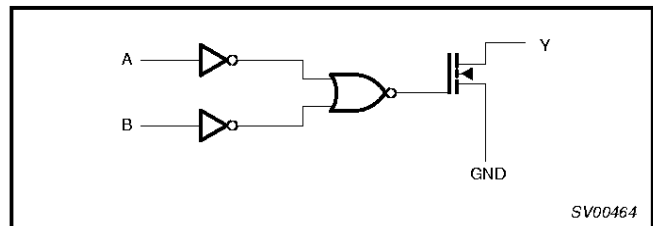
## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM



## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage for 'AC	2.0	6.0	V
$V_{CC}$	DC supply voltage for 'ACT	4.5	5.5	V
$V_{IN}$	DC input voltage range	0	$V_{CC}$	V
$V_O$	DC output voltage range	0	$V_{CC}$	V
$T_{amb}$	Operating in free-air temperature range	-40	+85	°C
$\Delta V/\Delta t$	Minimum input edge rate — AC devices $V_{IN}$ from 30% to 70% of $V_{CC}$ $V_{CC}$ @ 3.3V, 4.5V, 5.5V	125		mV/ns
	— ACT devices $V_{IN}$ from 0.8V to 2.0V $V_{CC}$ @ 4.5V, 5.5V	125		

## Quad 2-input NAND buffer (open drain)

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74ACT38**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

in accordance with the Absolute Maximum Rating System (IEC134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_{IN} = -0.5V$	-20	mA
		$V_{IN} = V_{CC} + 0.5V$	+20	
$V_{IN}$	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
$I_{OK}$	DC output diode current	$V_O = -0.5V$	-20	mA
		$V_O = V_{CC} + 0.5V$	+20	
$V_O$	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current		$\pm 50$	mA
$I_{CC}, I_{GND}$	DC $V_{CC}$ or GND current per output		$\pm 50$	mA
$I_{CC}, I_{GND}$	DC $V_{CC}$ or GND current		$\pm 200$	mA
$T_{stg}$	Storage temperature range		-65 to +150	$^{\circ}C$
$P_{TOT}$	Power dissipation per package - plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	above +70 $^{\circ}C$ derate linearly with 8 mW/K	500	mW
		above +60 $^{\circ}C$ derate linearly with 5.5 mW/K	500	

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## Quad 2-input NAND buffer (open drain)

74AC38  
74ACT38**DC CHARACTERISTICS FOR THE AC FAMILY**

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>OUT</sub> = 0.1V or (V <sub>CC</sub> - 0.1V)	3.0	2.1	1.5		V
			4.5	3.15	2.25		
			5.5	3.85	2.75		
V <sub>IL</sub>	LOW level Input voltage	V <sub>OUT</sub> = 0.1V or (V <sub>CC</sub> - 0.1V)	3.0		1.5	0.9	V
			4.5		2.25	1.35	
			5.5		2.75	1.65	
V <sub>OH</sub>	HIGH level output voltage	I <sub>OUT</sub> = -50 μA	3.0	2.9	2.99		V
			4.5	4.4	4.49		
			5.5	5.4	5.49		
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -12mA <sup>1</sup>	3.0	2.46			
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA <sup>1</sup>	4.5	3.76			
V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA <sup>1</sup>	5.5	4.76					
V <sub>OL</sub>	LOW level output voltage	I <sub>OUT</sub> = 50 μA	3.0		0.01	0.1	V
			4.5		0.01	0.1	
			5.5		0.01	0.1	
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 12mA <sup>1</sup>	3.0			0.44	
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>1</sup>	4.5			0.44	
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>1</sup>	5.5			0.44	
I <sub>IN</sub>	Input leakage current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			± 1.0	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IN</sub> = V <sub>CC</sub> or GND V <sub>OUT</sub> = V <sub>CC</sub> or GND	5.5			± 2.5	μA
I <sub>OLD</sub>	Dynamic output current <sup>2</sup>	V <sub>OLD</sub> = 1.65V max	5.5	75			mA
I <sub>OHD</sub>	Dynamic output current <sup>2</sup>	V <sub>OHD</sub> = 3.85V min	5.5			-75	mA
I <sub>CC</sub>	Quiescent supply current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			40	μA

**NOTES:**

- All outputs loaded
- Maximum test duration 2.0 ms; one output loaded at a time

## Quad 2-input NAND buffer (open drain)

74AC38  
74ACT38**DC CHARACTERISTICS FOR THE ACT FAMILY**

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>OUT</sub> = 0.1V or (V <sub>CC</sub> - 0.1V)	4.5	2.0	1.5		V
			5.5	2.0	1.5		
V <sub>IL</sub>	LOW level Input voltage	V <sub>OUT</sub> = 0.1V or (V <sub>CC</sub> - 0.1V)	4.5		1.5	0.8	V
			5.5		1.5	0.8	
V <sub>OH</sub>	HIGH level output voltage	I <sub>OUT</sub> = -50 μA	4.5	4.4	4.49		V
			5.5	5.4	5.49		
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA <sup>1</sup>	4.5	3.76			
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA <sup>1</sup>	5.5	4.76			
V <sub>OL</sub>	LOW level output voltage	I <sub>OUT</sub> = 50 μA	4.5		0.01	0.1	V
			5.5		0.01	0.1	
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>1</sup>	4.5			0.44	
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>1</sup>	5.5			0.44	
I <sub>IN</sub>	Input leakage current	V <sub>IN</sub> = V <sub>CC</sub> , GND	5.5			± 1.0	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IN</sub> = V <sub>CC</sub> or GND V <sub>OUT</sub> = V <sub>CC</sub> or GND	5.5			± 2.5	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per input pin	V <sub>IN</sub> = V <sub>CC</sub> - 2.1V Other inputs at V <sub>CC</sub> or GND; I <sub>OUT</sub> = 0	5.5			1.5	mA
I <sub>OLD</sub>	Dynamic output current <sup>2</sup>	V <sub>OLD</sub> = 1.65V max	5.5	75			mA
I <sub>OHD</sub>	Dynamic output current <sup>2</sup>	V <sub>OHD</sub> = 3.85V min	5.5			-75	mA
I <sub>CC</sub>	Quiescent supply current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			40	μA

**NOTES:**

1. All outputs loaded
2. Maximum test duration 2.0ms, one output loaded at a time

## Quad 2-input NAND buffer (open drain)

74AC38  
74ACT38**AC CHARACTERISTICS FOR 74AC38**GND = 0V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ; .

SYMBOL	PARAMETER	$V_{CC}^1$	LIMITS					UNIT	WAVEFORM
			$T_{amb} = +25^\circ\text{C}$			$T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$			
			MIN	TYP	MAX	MIN	MAX		
$t_{PLH}$	Propagation delay nA, nB to nY	3.3 5.0	2.0 1.5	3.3 2.0	6.5 4.5	1.5 1.0	7.0 5.0	ns	1, 2
$t_{PHL}$	Propagation delay nA, nB to nY	3.3 5.0	2.0 1.5	3.0 2.2	6.5 4.5	1.5 1.0	7.0 5.0	ns	

**NOTE:**

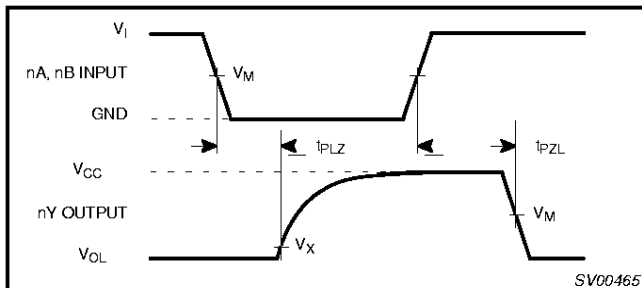
1. Voltage range 3.3V is  $V_{CC} = 3.3V \pm 0.3V$   
Voltage range 5.0V is  $V_{CC} = 5.0V \pm 0.5V$

**AC CHARACTERISTICS FOR 74ACT38**GND = 0V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ; .

SYMBOL	PARAMETER	$V_{CC}^1$	LIMITS					UNIT	WAVEFORM
			$T_{amb} = +25^\circ\text{C}$			$T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$			
			MIN	TYP	MAX	MIN	MAX		
$t_{PLH}$	Propagation delay nA, nB to nY	5.0	2.0	3.2	6.0	1.5	7.0	ns	1, 2
$t_{PHL}$	Propagation delay nA, nB to nY	5.0	2.0	3.5	6.0	1.5	7.0	ns	

**NOTE:**

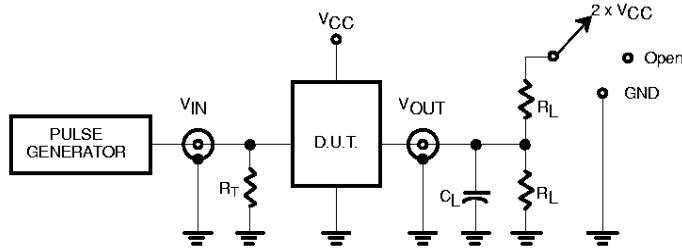
1. Voltage range 5.0V is  $V_{CC} = 5.0V \pm 0.5V$

**AC WAVEFORMS****Waveform 1. Inputs (nA, nB) to output (nY) propagation delays**

Quad 2-input NAND buffer (open drain)

74AC38  
74ACT38

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open

FAMILY	$V_{IN}$ Input Requirements	$V_m$ Input	$V_m$ Output
AC	GND to $V_{CC}$	50% $V_{CC}$	50% $V_{CC}$
ACT	GND to 3.0V	1.5V	50% $V_{CC}$

DEFINITIONS

- $R_L$  = Load resistor; see AC characteristics for value.
- $C_L$  = Load capacitance, see AC characteristics
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

SV00451

Waveform 2. Load circuitry for switching times

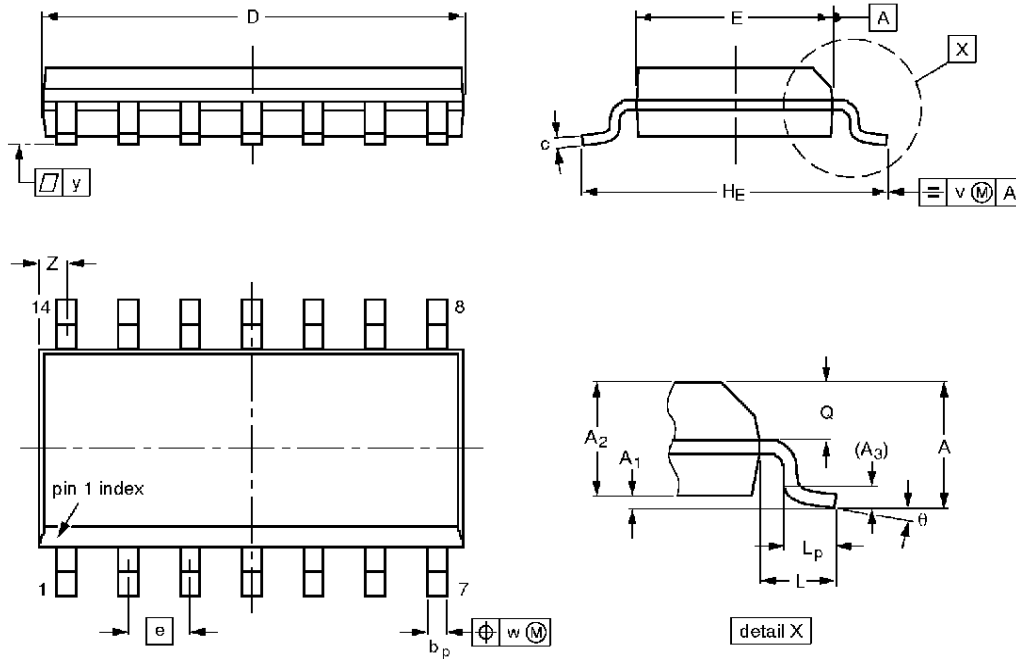


Quad 2-input NAND buffer (open drain)

74AC38  
74ACT38

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

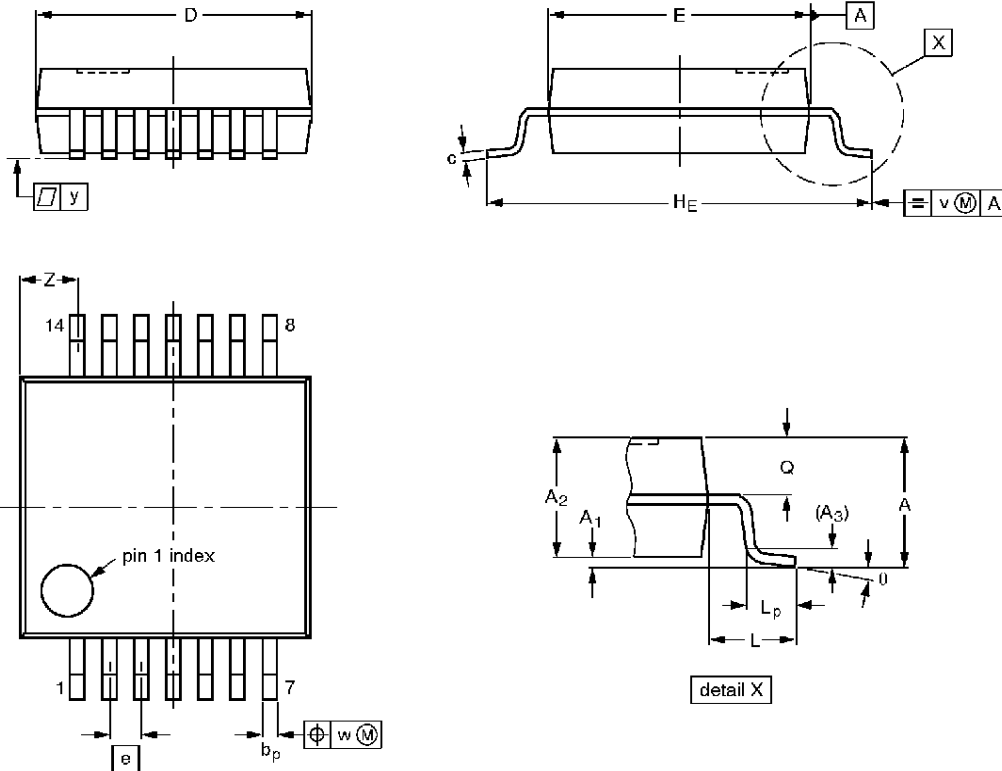
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				91-08-10 95-01-23

Quad 2-input NAND buffer (open drain)

74AC38  
74ACT38

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

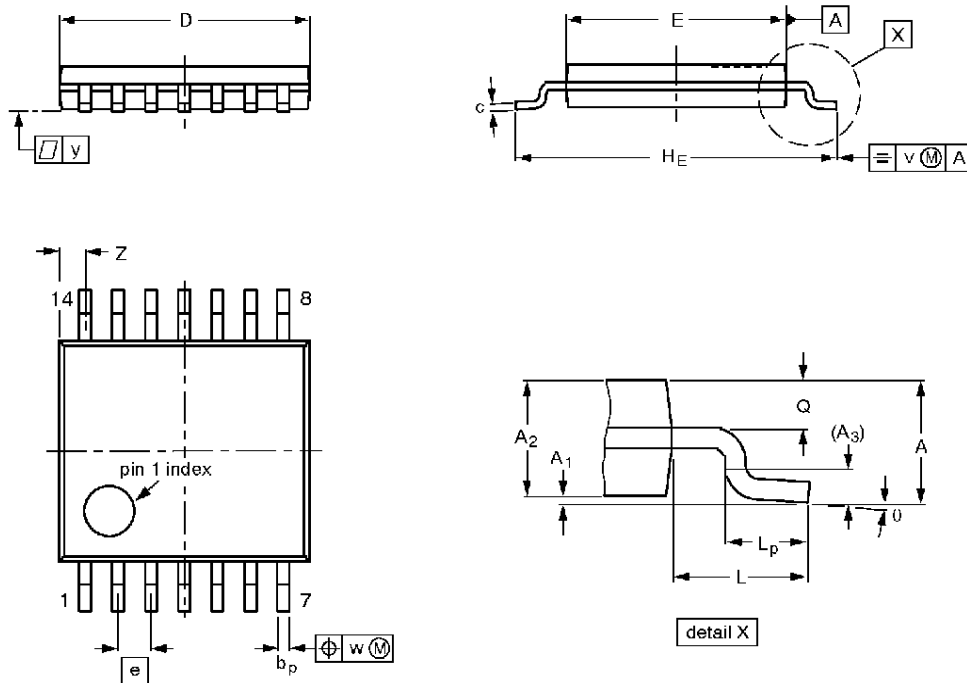
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT337-1		MO-150AB			<del>95-02-04</del> 96-01-18

Quad 2-input NAND buffer (open drain)

74AC38  
74ACT38

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				94-07-12 95-04-04

Quad 2-input NAND buffer (open drain)

74AC38  
74ACT38

**DEFINITIONS**

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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