MIC23156

1.5A, 3MHz Synchronous Buck Regulator with HyperLight Load® and I²C Control for Dynamic Voltage Scaling

General Description

The MIC23156 is a high-efficiency 1.5A synchronous buck regulator with HyperLight Load® mode and dynamic voltage scaling control through I²C. HyperLight Load provides very high efficiency at light loads and ultra-fast transient response. The ability to dynamically change the output voltage and maintain high output voltage accuracy make the MIC23156 perfectly suited for supplying processor core voltages. An additional benefit of this proprietary architecture is very low output ripple voltage throughout the entire load range with the use of small output capacitors. Fast mode plus I²C provides output voltage and chip enable/disable control from standard I²C bus with I²C clock rates of 100kHz, 400kHz, and 1MHz.

The MIC23156 is designed for use with 1µH, and an output capacitor as small as 2.2µF that enables a total solution size, less than 1mm in height.

The MIC23156 is available in both 16-ball, 0.4mm Pitch, 1.81mm x 1.71mm wafer level chip scale (WLCSP), and 17-pin 2.8mm x 2.5mm MLF® packages with an operating junction temperature range of –40°C to +125°C.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Features

- Input voltage: 2.7V to 5.5V
- Up to 1.5A output current
- 1MHz I²C-controlled adjustable output
  - V_{OUT} = 0.7 to 2.4V in 10mV steps
- High output voltage accuracy (±1.5% over temperature)
- Fast pin–selectable output voltage
- Programmable soft-start using external capacitor
- Ultra-low quiescent current of 30µA when not switching
- Thermal-shutdown and current-limit protection
- Safe startup in to pre-biased output
- Stable with 1µH output inductor and 2.2µF ceramic capacitor
- Up to 93% peak efficiency
- –40°C to +125°C junction temperature range

Applications

- Mobile handsets
- Solid state drives (SSD)
- WiFi/WiMx/WiBro modules
- Portable applications

Typical Application
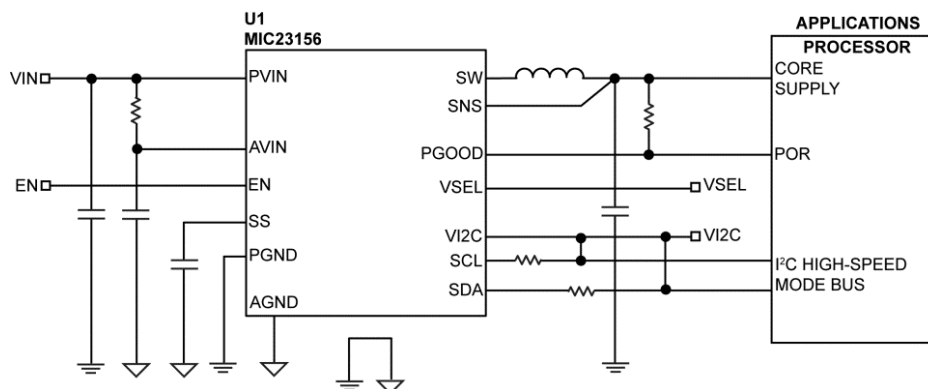
HyperLight Load is a registered trademark of Micrel, Inc.

MLF and *Micro*Lead Frame are registered trademarks of Amkor Technology, Inc.

Ordering Information

| Part Number	Marking Code	Default Output Voltage		Junction Temperature Range	Package
		VSEL = LOW	VSEL = HIGH		
MIC23156-0YCS	JA	1.0V	0.8V	−40°C to +125°C	16-Ball 1.81mm × 1.71mm WLCSP
MIC23156-0YML	JQA				17-Pin 2.8mm × 2.5mm MLF[1]

Note:

1. MLF is a Green, RoHS-compliant package. Lead finish is NiPdAu. Mold is Halogen free..

Pin Configuration
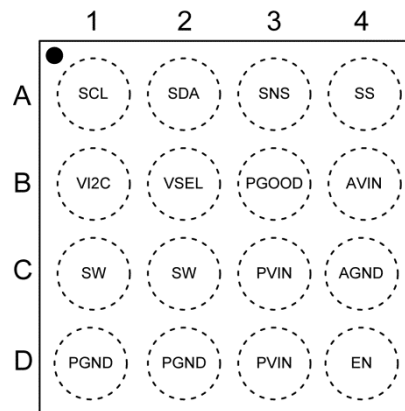
1.81mm × 1.71mm WLCSP (CS) Adjustable Output Voltage
(Top View)
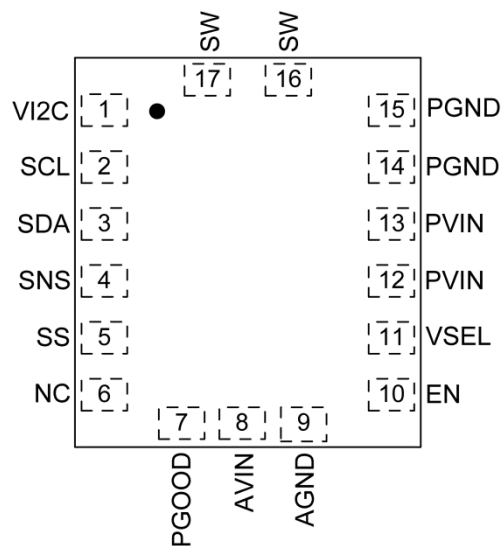
2.8mm × 2.5mm MLF (ML) Adjustable Output Voltage
(Top View)

Pin Description

Ball Number	Pin Number	Pin Name	Pin Function
WLCSP	MLF		
A1	2	SCL	Fast-Mode Plus 1MHz I²C Clock Input Pin.
A2	3	SDA	Fast-Mode Plus 1MHz I²C Data Input/Output Pin.
A3	4	SNS	Sense: Connect to V_{OUT}, close to output cap to sense V_{OUT}.
A4	5	SS	Programmable Soft Start: Connect capacitor to AGND.
B1	1	VI2C	Power Connection for I²C Bus Voltage: Connect this pin to the voltage domain of the I²C bus supply. Do not leave floating.
B2	11	VSEL	Pin Selectable: Output voltage of either of two I²C voltage registers. Do not leave floating.
B3	7	PGOOD	Power Good Indicator: Use an external pull-up resistor to supply.
B4	8	AVIN	Input Voltage to Power Analog Functions: Connect decoupling capacitor to ground.
C1, C2	16, 17	SW	Switch Connection: Internal power MOSFET output switches.
C3, D3	12, 13	PVIN	Input Voltage to Power Switches: Connect decoupling capacitor to ground.
C4	9	AGND	Analog Ground: Connect to central ground point where all high-current paths meet (C_{IN}, C_{OUT}, and PGND) for best operation.
D1, D2	14, 15	PGND	Power Ground Connection.
D4	10	EN	Enable: Logic high enables operation of voltage regulator. Logic low shuts down the device. Do not leave floating.
–	6	NC	No Connect.

Absolute Maximum Ratings[1]

Input Supply Voltage (AVIN, PVIN, VI2C)....... −0.3V to +6V
Switch Voltage (SW) .... −0.3V to AVIN
Logic Voltage (EN, PGOOD)........................ −0.3V to AVIN
Logic Voltage (VSEL, SCL, SDA) ....−0.3V to VI2C
Analog Input Voltage (SNS, SS) .... −0.3V to AVIN
Power Dissipation (T_A = +70°C) ....Internally Limited
Storage Temperature (T_S).........................−65°C to +150°C
Lead Temperature (soldering, 10s).........................+260°C
ESD Rating[3] 2kV

Operating Ratings[2]

Input Supply Voltage (AVIN, PVIN, VI2C).... +2.7V to +5.5V
Switch Voltage (SW) .... 0V to AVIN
Logic Voltage (EN, PGOOD) .... 0V to AVIN
Logic Voltage (VSEL, SCL, SDA) ....0V to VI2C
Analog Input Voltage (SNS, SS) .... 0V to AVIN
Junction Temperature Range (T_J).......−40°C ≤ T_J ≤ +125°C
Thermal Resistance
    1.81mm × 1.71mm WLCSP-16 (θ_{JA}) ....150°C/W
    2.8mm × 2.5mm MLF-17 (θ_{JA}) ....89°C/W

Electrical Characteristics[4]

T_A = 25°C, AVIN = PVIN = V_{EN} = V_{VI2C} = 3.6V; L = 1.0µH; C_{OUT} = 2.2µF, unless otherwise specified.

Bold values indicate −40°C ≤ T_J ≤ +125°C, unless noted.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage Range		**2.7**		**5.5**	V
Enable Logic Pin Low Threshold	Logic Low			**0.5**	V
Enable Logic Pin High Threshold	Logic High	**1.2**			V
VSEL Logic Pin Low Threshold	Logic Low			**0.3 × VI2C**	V
VSEL Logic Pin High Threshold	Logic High	**0.7 × VI2C**			V
Logic Pin Input Current	Pins: EN and VSEL		0.1	**2**	µA
Undervoltage Lockout Threshold	Rising	**2.45**	2.55	**2.65**	V
Undervoltage Lockout Hysteresis	Falling		75		mV
Shutdown Temperature			160		°C
Shutdown Temperature Hysteresis			20		°C
Shutdown Current	V_{EN} = 0V		0.1	5	µA
DC-to-DC Converter					
Output Voltage Accuracy	V_{OUT} = 1V, I_{OUT} = 10mA	−1.5		+1.5	%
Quiescent Current	I_{OUT} = 0mA, V_{FB} > 1.2*V_{OUT}		30	50	µA
Output Voltage Range		0.7		2.4	V
Output Voltage Line Regulation	3.0V < V_{AVIN} < 4.5, I_{LOAD} = 10mA		0.02		%/V
Output Voltage Load Regulation	20mA < I_{OUT} < 1A		0.04		%

Notes:

1. Exceeding the absolute maximum ratings may damage the device.

2. The device is not guaranteed to function outside its operating ratings.

3. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5k in series with 100pF.

4. Specification for packaged product only.

# Electrical Characteristics[4] (Continued)

T_A = 25°C, AVIN = PVIN = V_{EN} = V_{VI2C} = 3.6V; L = 1.0µH; C_{OUT} = 2.2µF, unless otherwise specified.

Bold values indicate −40°C ≤ T_J ≤ +125°C, unless noted.

| Parameter	Condition	Min.	Typ.	Max.	Units
Switch On-Resistance	I_{SW} = +100mA, High-Side Switch PMOS (MLF)		0.17		Ω
	I_{SW} = +100mA, High-Side Switch PMOS (WLCSP)		0.15		
	I_{SW} = −100mA, Low-Side Switch NMOS (MLF)		0.15		
	I_{SW} = −100mA, Low-Side Switch NMOS (WLCSP)		0.13		
Current Limit (DC Value)	V_{OUT} = 1V	1.7	2.9	5.1	A
Frequency			3		MHz
Maximum Duty Cycle	Frequency = 3MHz	80			%
DVS Step Size			10		mV
Soft-Start Time	V_{OUT} = 90%, C_{SS} = 120pF		250		µs
I²C Interface (Assuming 550pF Total Bus Capacitance)					
I²C Address	Read (Binary, Hex)		10110111, 0xB7		
	Write (Binary, Hex)		10110110, 0xB6		
LOW-Level Input Voltage	SCL, SDA			**0.3 × VI2C**	V
HIGH-Level Input Voltage	SCL, SDA	**0.7 × VI2C**			V
SDA Pull-Down Resistance	Open drain pull-down on SDA during read back, I_{SDA} = 500µA		20		Ω
Power Good					
PGOOD Output Low	V_{OUT} < 80% V_{NOM}, I_{PGOOD} = −500µA		100		mV
PGOOD Output Leakage	V_{OUT} = V_{NOM}			**5**	µA
PGOOD Threshold % of V_{OUT} < V_{NOM}	V_{OUT} ramping up	86		96	%
PGOOD hysteresis			5		%

Typical Characteristics

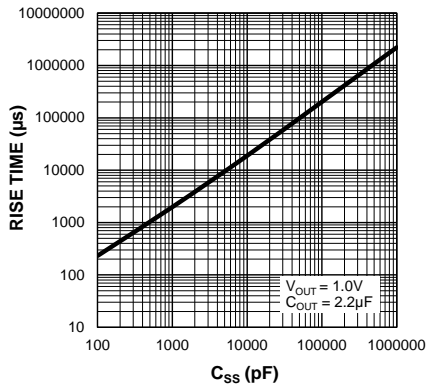**Efficiency (V_{OUT} = 2.4V) vs. Output Current**
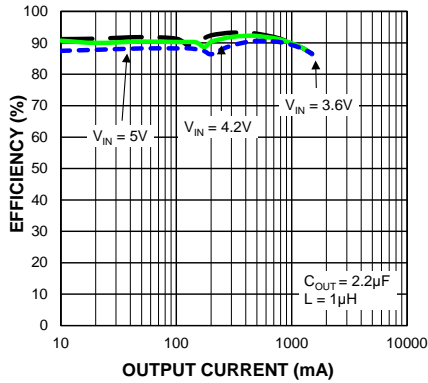
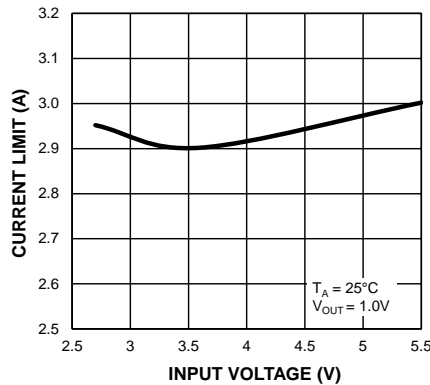**Efficiency (V_{OUT} = 1.8V) vs. Output Current**
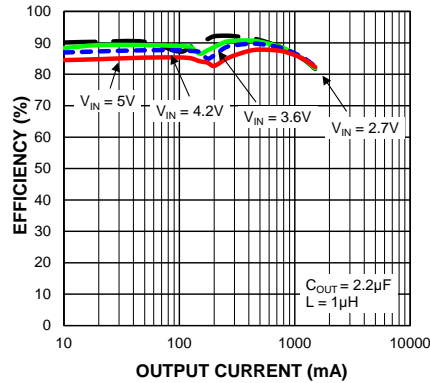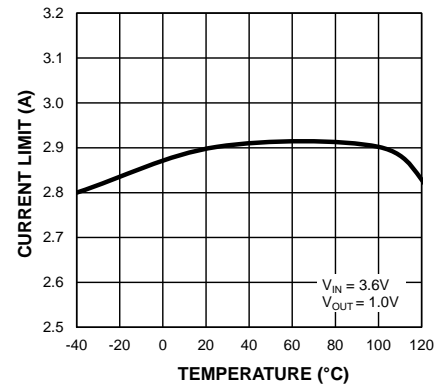
Efficiency (V_{OUT} = 1.0V) vs. Output Current
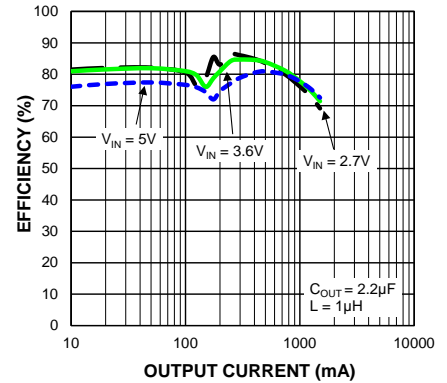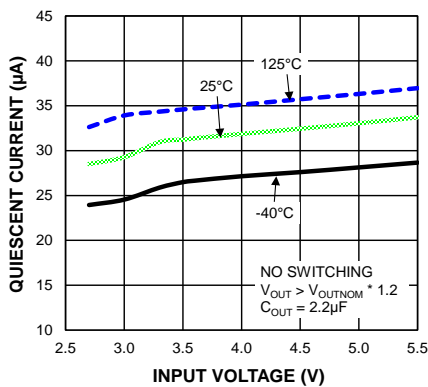
V_{OUT} Rise Time vs. C_{SS}
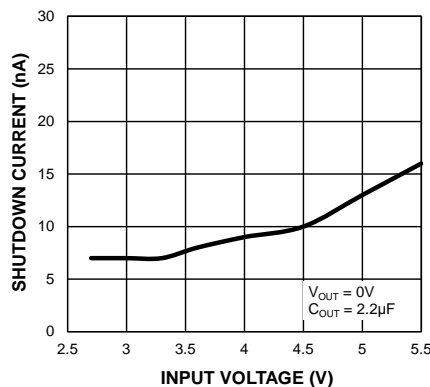
Current Limit vs. Input Voltage
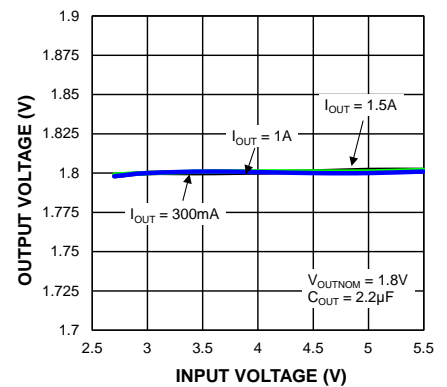
Current Limit vs. Temperature

Quiescent Current vs. Input Voltage

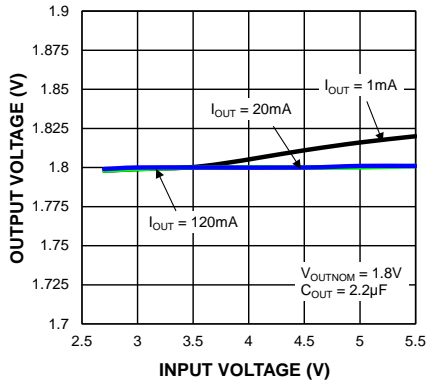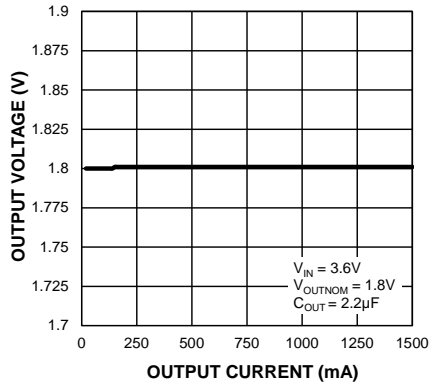**Shutdown Current vs. Input Voltage**

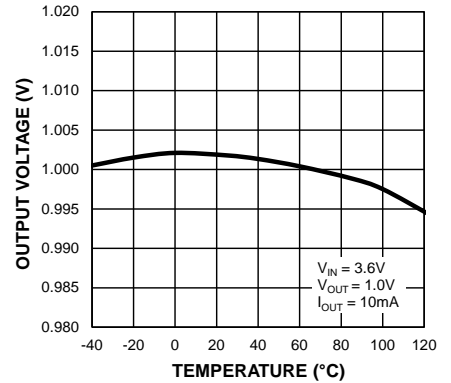**Line Regulation (CCM)**

Typical Characteristics (Continued)
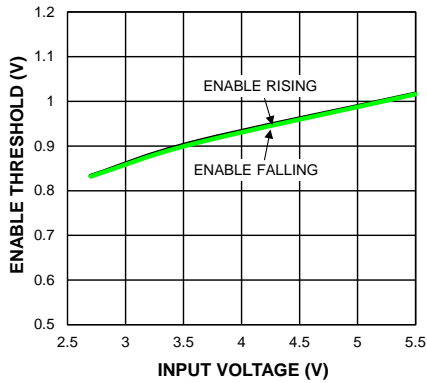
Line Regulation (HLL)
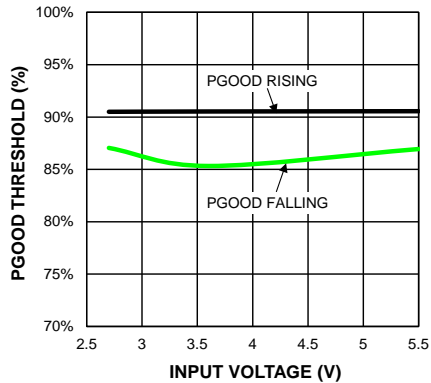

Load Regulation

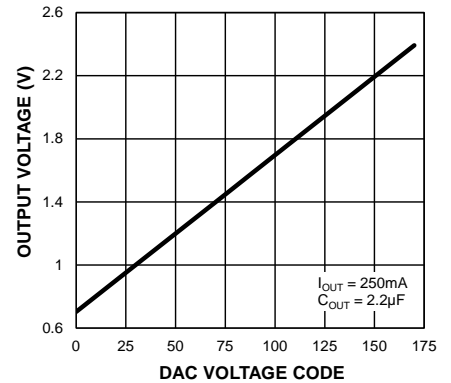**Output Voltage vs. Temperature**
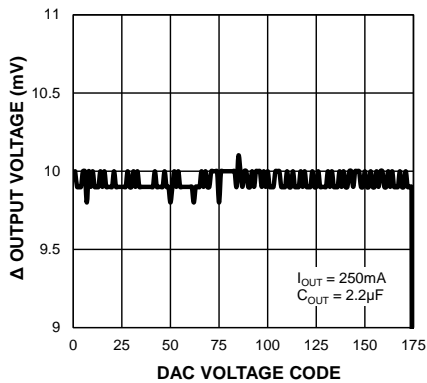

Enable Threshold vs. Input Voltage

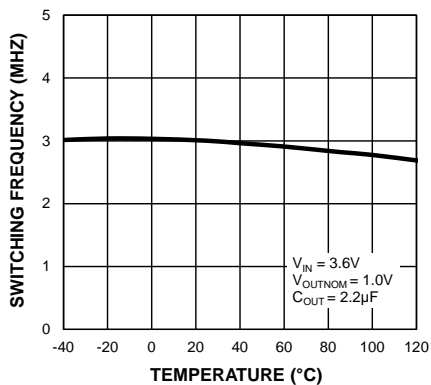**PGOOD Threshold vs. Input Voltage**

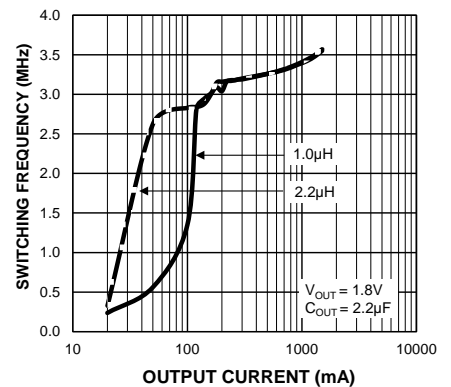**Output Voltage vs. DAC Linearity**

Δ Output Voltage vs. DAC DNL
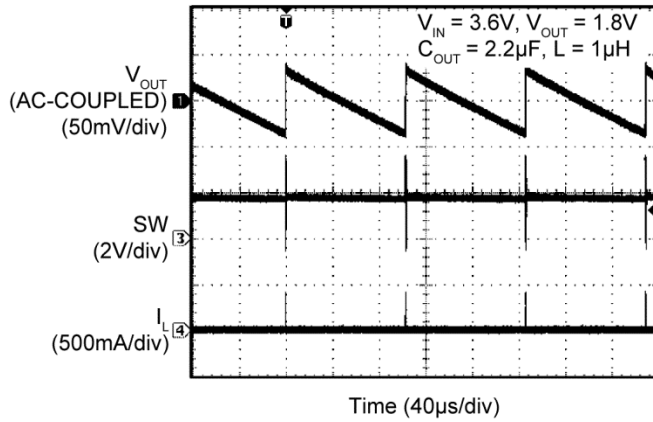

Switching Frequency vs. Temperature

Switching Frequency vs. Output Current

Functional Characteristics

Switching Waveform
Discontinuous Mode (1mA)
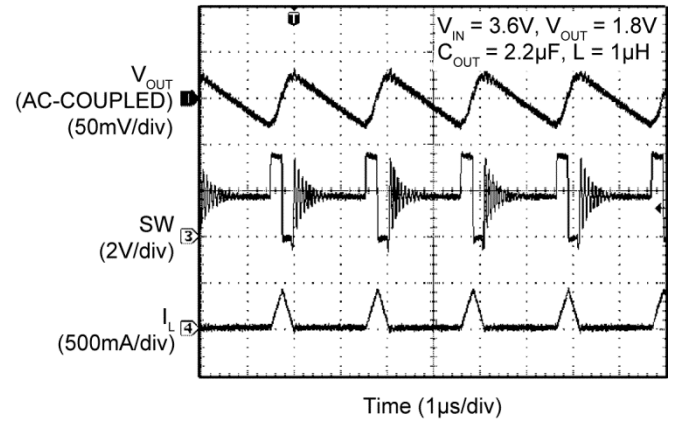
V_{IN} = 3.6V, V_{OUT} = 1.8V
C_{OUT} = 2.2µF, L = 1µH

V_{OUT}
(AC-COUPLED)
(50mV/div)

SW
(2V/div)

I_L
(500mA/div)

Time (40µs/div)

Switching Waveform
Discontinuous Mode (50mA)

V_{IN} = 3.6V, V_{OUT} = 1.8V
C_{OUT} = 2.2µF, L = 1µH

V_{OUT}
(AC-COUPLED)
(50mV/div)

SW
(2V/div)

I_L
(500mA/div)

Time (1µs/div)

Switching Waveform
Continuous Mode (500mA)

V_{OUT}
(AC-COUPLED)
(10mV/div)

SW
(2V/div)

I_L
(500mA/div)

V_{IN} = 3.6V, V_{OUT} = 1.8V
C_{OUT} = 2.2µF, L = 1µH

Time (100ns/div)

Switching Waveform
Continuous Mode (1.5A)

V_{OUT}
(AC-COUPLED)
(10mV/div)

SW
(2V/div)

I_L
(1A/div)

V_{IN} = 3.6V, V_{OUT} = 1.8V
C_{OUT} = 2.2µF, L = 1µH

Time (100ns/div)

Load Transient
(50mA to 750mA)

V_{OUT}
(AC-COUPLED)
(50mV/div)

I_{OUT}
(200mA/div)

V_{IN} = 3.6V
V_{OUT} = 1.8V
C_{OUT} = 2.2µF
L = 1µH

Time (40µs/div)

Load Transient
(50mA to 1A)

V_{OUT}
(AC-COUPLED)
(50mV/div)

V_{IN} = 3.6V
V_{OUT} = 1.8V
C_{OUT} = 2.2µF
L = 1µH

I_{OUT}
(500mA/div)

Time (40µs/div)
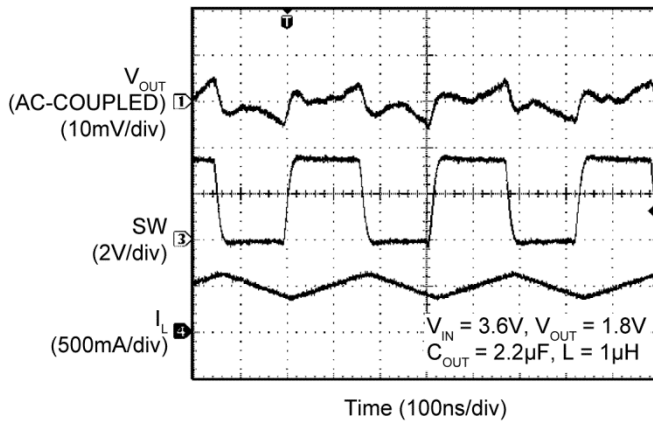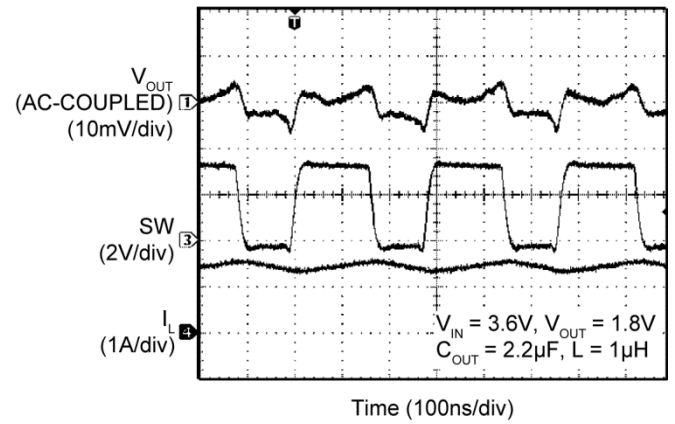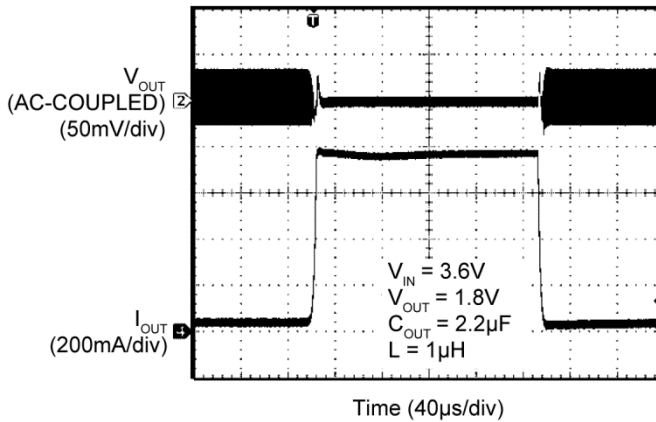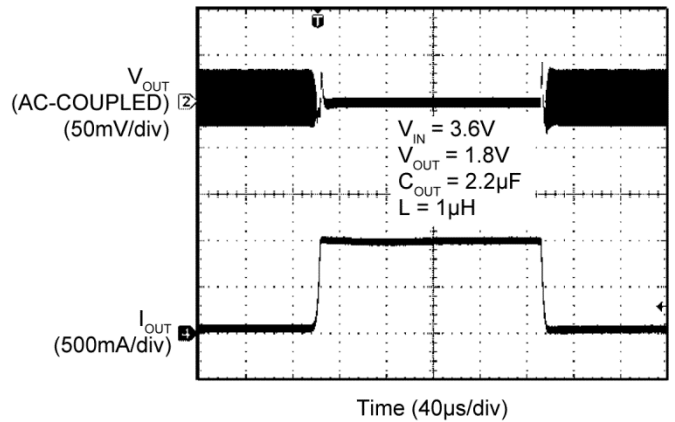
Functional Characteristics (Continued)

**Load Transient
(200mA to 600mA)**
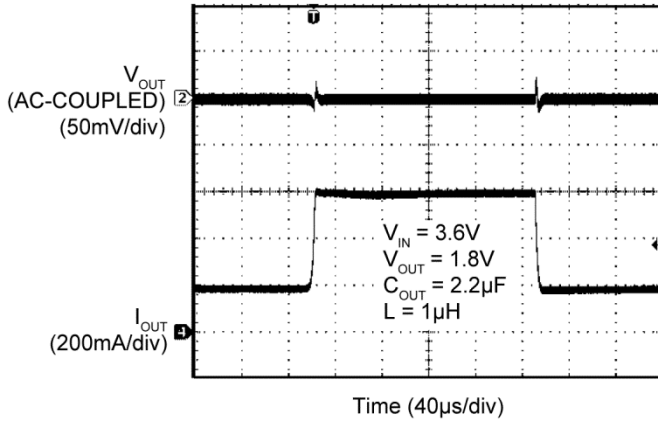
V$_{OUT}$
(AC-COUPLED)
(50mV/div)

I$_{OUT}$
(200mA/div)

V$_{IN}$ = 3.6V
V$_{OUT}$ = 1.8V
C$_{OUT}$ = 2.2µF
L = 1µH

Time (40µs/div)

**Load Transient
(200mA to 1.5A)**

V$_{OUT}$
(AC-COUPLED)
(50mV/div)

I$_{OUT}$
(500mA/div)

V$_{IN}$ = 3.6V
V$_{OUT}$ = 1.8V
C$_{OUT}$ = 2.2µF
L = 1µH

Time (40µs/div)

**Load Transient
(200mA to 1.5A)**

V$_{OUT}$
(AC-COUPLED)
(50mV/div)

I$_{OUT}$
(500mA/div)

V$_{IN}$ = 3.6V
V$_{OUT}$ = 1.8V
C$_{OUT}$ = 2.2µF
L = 1µH

Time (40µs/div)

**Line Transient
(3.6V to 5.5V @ 1.5A)**

V$_{IN}$
(2V/div)

V$_{OUT}$
(AC-COUPLED)
(50mV/div)

V$_{IN}$ = 3.6V TO 5.5V
V$_{OUT}$ = 1.8V
C$_{OUT}$ = 2.2µF
L = 1µH

Time (100µs/div)
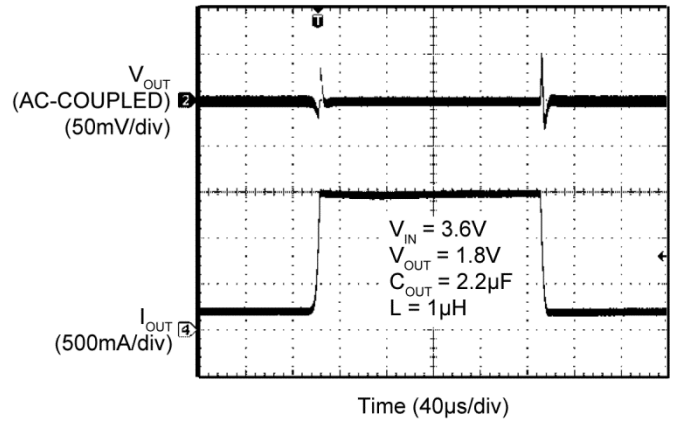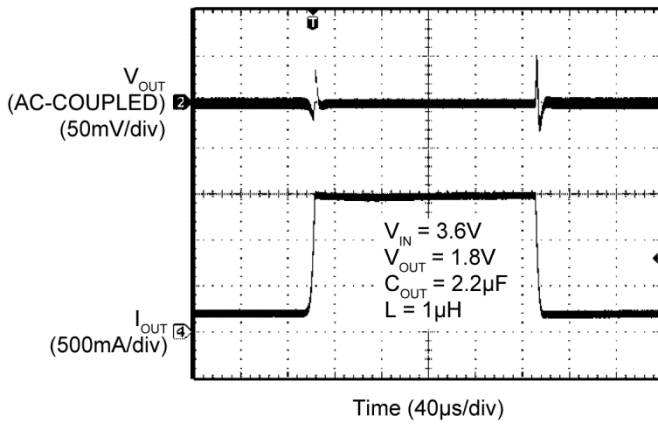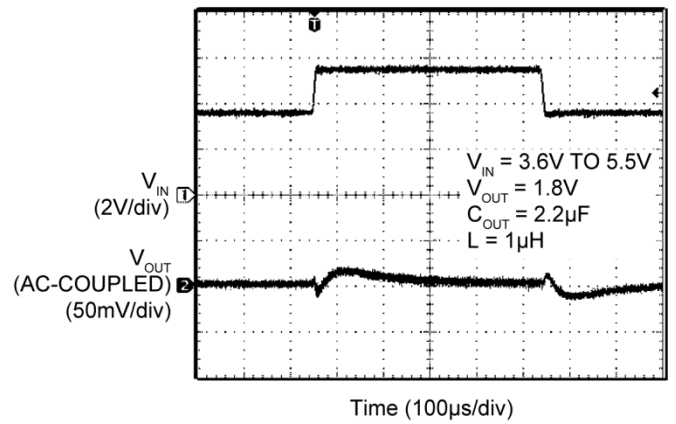
**Power Good during Load Transient
(200mA to 1.5A)**

V$_{OUT}$
(AC-COUPLED)
(100mV/div)

PGOOD
(500mV/div)
I$_{OUT}$
(500mA/div)

V$_{IN}$ = 3.6V
V$_{OUT}$ = 1.8V
C$_{OUT}$ = 2.2µF
L = 1µH

Time (100µs/div)
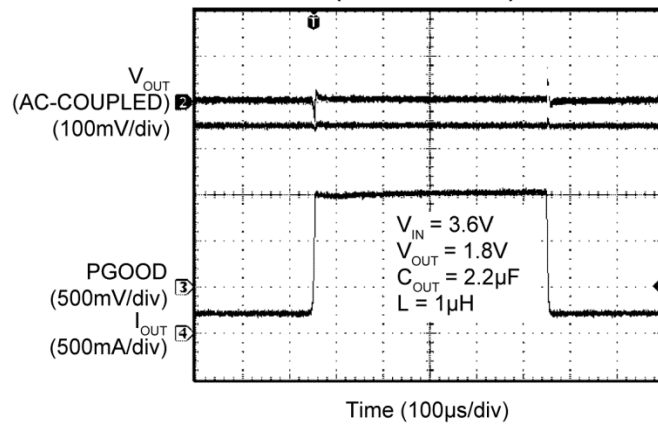
**Power Good during Line Transient
(3.6V to 5.5V @ 1.5A)**

V$_{IN}$
(2V/div)

V$_{OUT}$
(AC-COUPLED)
(50mV/div)

PGOOD
(2V/div)

V$_{IN}$ = 3.6V TO 5.5V
V$_{OUT}$ = 1.8V
C$_{OUT}$ = 2.2µF
L = 1µH

Time (100µs/div)
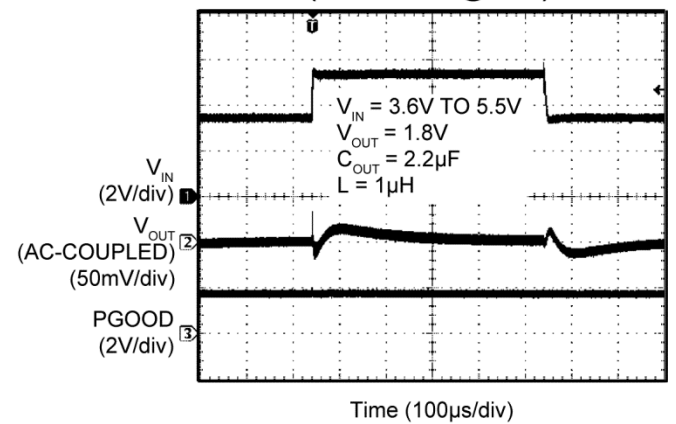
Functional Characteristics (Continued)

Power Good during Startup

V_{EN} (2V/div)

V_{OUT} (500mV/div)

PGOOD (500mV/div)

V_{IN} = 3.6V , V_{OUT} = 1.0V
C_{OUT} = 2.2μF, I_{OUT} = 20mA
C_{SS} = 120pF

Time (200μs/div)
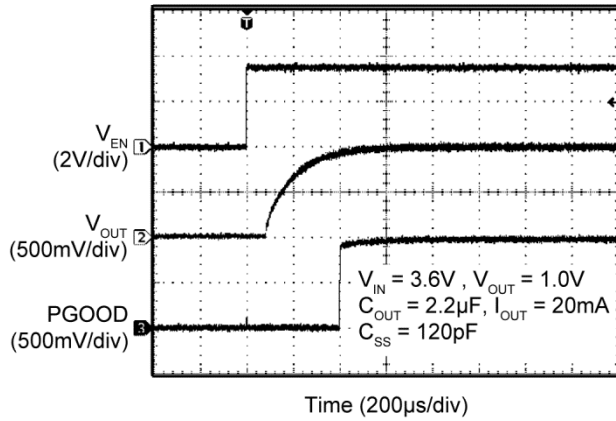
Power Good during Shutdown

V_{IN} = 3.6V , V_{OUT} = 1.0V
C_{OUT} = 2.2μF, I_{OUT} = 20mA
C_{SS} = 120pF

V_{EN} (2V/div)

V_{OUT} (500mV/div)

PGOOD (500mV/div)

Time (20μs/div)
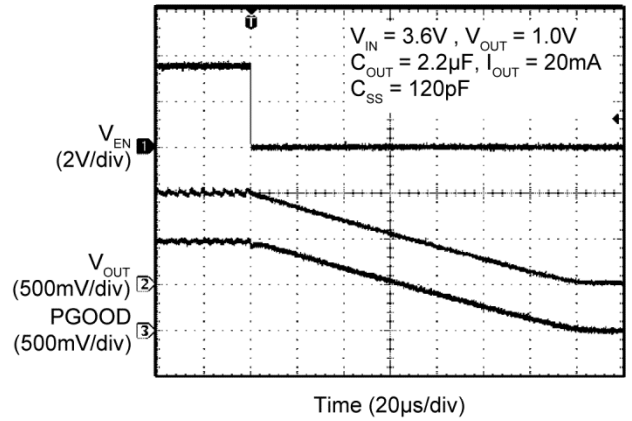
V_{OUT} during VSEL Transition

VSEL (5V/div)

V_{OUT} (400mV/div)

PGOOD (400mV/div)

I_{IN} (50mA/div)

V_{IN} = VI2C = 3.6V
C_{OUT} = 2.2μF, I_{OUT} = 250mA
C_{SS} = 120pF

Time (1ms/div)
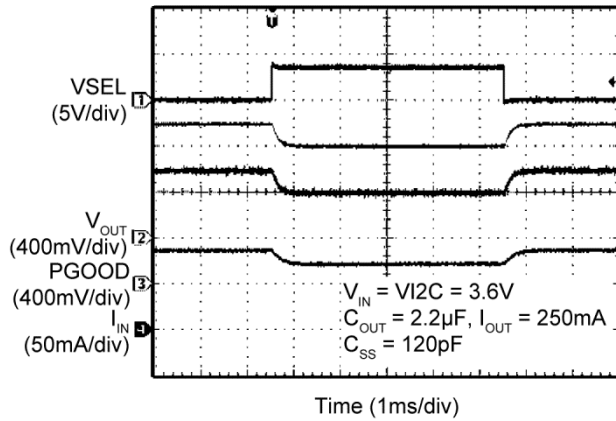
Functional Block Diagram

Figure 1. Simplified MIC23156 Functional Block Diagram

Functional Description

PVIN

The input supply (PVIN) provides power to the internal MOSFETs for the switch mode regulator section. The PVIN operating range is 2.7V to 5.5V so an input capacitor with a minimum voltage rating of 6.3V is recommended. Due to the high switching speed, a minimum 2.2µF bypass capacitor placed close to PVIN and the power ground (PGND) pin is required. Refer to PCB Layout Recommendations (MLF Package) for more details.

AVIN

Analog VIN (AVIN) provides power to the internal control and analog supply circuitry. AVIN must be tied to PVIN through a 10Ω RC filter. Careful layout should be considered to ensure that any high-frequency switching noise caused by PVIN is reduce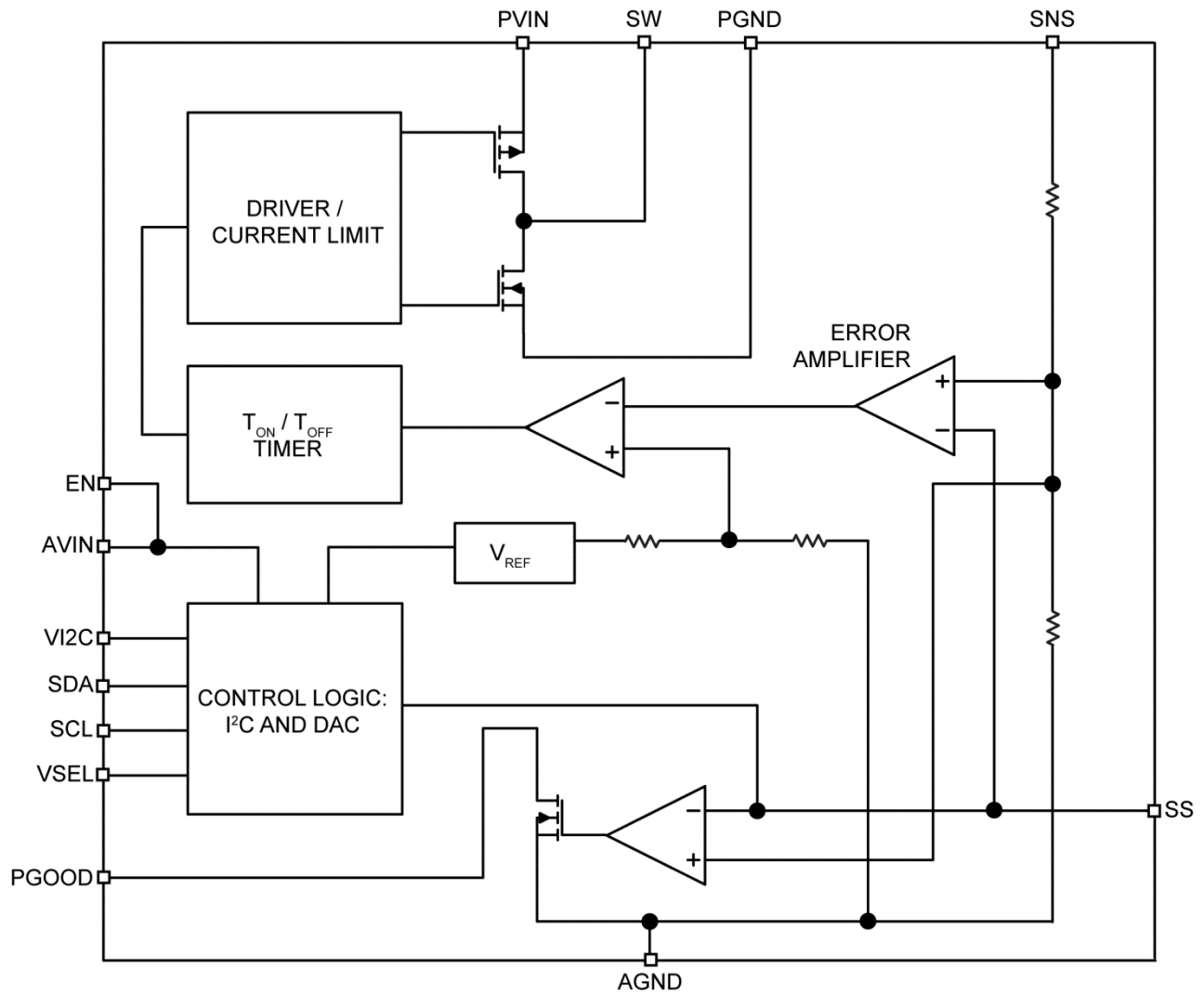d before reaching AVIN. A 2.2µF capacitor as close to AVIN as possible is recommended. Refer to PCB Layout Recommendations (MLF Package) for more details.

EN

A logic high signal on the enable pin activates the output voltage of the device. A logic low signal on the enable pin deactivates the output and reduces supply current to 0.1µA. Do not leave the EN pin floating. MIC23156 features external soft-start circuitry via the soft start (SS) pin that reduces in-rush current and prevents the output voltage from overshooting when EN is driven logic high. Do not leave the EN pin floating.

SW

The switch (SW) connects directly to one end of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the SNS pin, output capacitor and the load. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes whenever possible.

SNS

The sense (SNS) pin is connected to the output of the device to provide feedback to the control circuitry. The SNS connection should be placed close to the output capacitor. Refer to PCB Layout Recommendations (MLF Package) for more details.

AGND

The analog ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the power ground

(PGND) loop. Refer to PCB Layout Recommendations (MLF Package) for more details.

PGND

The power ground (PGND) pin is the ground path for the high current in PWM mode. The current loop for the power ground should be as small as possible and separate from the analog ground (AGND) loop as applicable. Refer to PCB Layout Recommendations (MLF Package) for more details.

PGOOD

The power good (PGOOD) pin is an open drain output which indicates logic high when the output voltage is typically above 90% of its steady state voltage. A pull-up resistor of more than 5kΩ should be connected from PGOOD to VOUT.

SS

The soft-start (SS) pin is used to control the output voltage ramp up time. The approximate equation for the ramp time in seconds is $820 \times 103 \times \ln(10) \times C_{SS}$. For example, for a C_{SS} = 120pF, $T_{RISE} \approx$ 230µs. Refer to the "V_{OUT} Rise Time vs. C^{SS}" graph in the Typical Characteristics section. The minimum recommended value for C_{SS} is 120pF.

VI2C

Power connection for I^{2}C bus voltage. Connect this pin to the voltage domain of the I^{2}C bus supply.

VSEL

Selectable output voltage of either of two I2C voltage registers. A logic low selects buck register 1 and logic high selects buck register 2. If no I^{2}C programming is used the output voltages will be as per the default voltage register values. Do not leave floating.

SCL

The I^{2}C clock input pin provides a reference clock for clocking in the data signal. This is a fast-mode plus 1MHz input pin, and requires a 4.7KΩ pull-up resistor.

SDA

The I^{2}C data input/output pin allows for data to be written to and read from the MIC23156. This is a fast-mode plus 1MHz I^{2}C pin, and requires a 4.7KΩ pull-up resistor.

Application Information

The MIC23156 is a high-performance DC-to-DC step-down regulator offering a small solution size and supporting up to 1.5A in a 2.8mm × 2.5mm MLF and 1.81mm × 1.71mm WLCSP package. Using the HyperLight Load switching scheme, the MIC23156 is able to maintain high efficiency and exceptional voltage accuracy throughout the entire load range while providing ultra-fast load transient response. Another beneficial feature is the ability to dynamically change the output voltage in steps of 10mV. The following subsections provide additional device application information.

Input Capacitor

A 2.2µF (or larger) ceramic capacitor should be placed as close as possible to the PVIN and AVIN pins with short trace for good noise performance. X5R or X7R type ceramic capacitors are recommended for better tolerance over temperature. The Y5V and Z5U type temperature rating ceramic capacitors are not recommended due to their large reduction in capacitance over temperature and increased resistance at high frequencies. These reduce their ability to filter out high-frequency noise. The rated voltage of the input capacitor should be at least 20% higher than the maximum operating input voltage over the operating temperature range.

Output Capacitor

Output capacitor selection is also a trade-off between performance, size, and cost. Increasing output capacitor will lead to an improved transient response, however, the size and cost also increase. The MIC23156 is designed for use with a 2.2µF or greater ceramic output capacitor. A low equivalent series resistance (ESR) ceramic output capacitor is recommended based upon performance, size and cost. Both the X7R or X5R temperature rating capacitors are recommended. Refer to Table 1 for additional information.

Inductor Selection

Inductor selection is a balance between efficiency, stability, cost, size, and rated current. Since the MIC23156 is compensated internally, the recommended inductance of L is limited from 0.47µH to 2.2µH to ensure system stability.

For faster transient response, a 0.47µH inductor will yield the best result. For lower output ripple, a 2.2µH inductor is recommended.

Maximum current ratings of the inductor are generally given in two methods; permissible DC current, and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 30% loss in inductance.

Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so that the peak current does not cause the inductor to saturate. Peak current can be calculated as noted in Equation 1:

$$I_{PEAK} = \left[I_{OUT} + V_{OUT}\left(\frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L} \right) \right]$$

Eq. 1

As shown by Equation 1, the peak inductor current is inversely proportional to the switching frequency and the inductance. The lower the switching frequency or the inductance, the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends upon the requirements of the application. Refer to the Typical Application and Bill of Materials for details.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to Efficiency Considerations.

The transition between continuous-conduction mode (CCM) to HyperLight Load mode is determined by the inductor ripple current and the load current.

Figure 2 shows the signals for high-side switch drive (HSD) for T_{ON} control, the Inductor current and the low side switch drive (LSD) for T_{OFF} control.
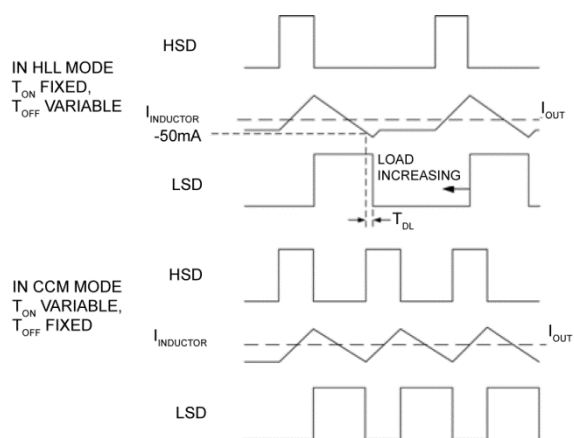

Figure 2. HSD Signals for T_{ON} Control, Inductor Current, and LSD for T_{OFF} Control

In HLL mode, the inductor is charged with a fixed Ton pulse on the high-side switch (HSD). After this, the LDS is switched on and current falls at a rate V_{OUT}/L. The controller remains in HLL mode while the inductor falling current is detected to cross approximately 200mA. When the LSD (or T_{OFF}) time reaches its minimum and the inductor falling current is no longer able to reach this 200mA threshold, the part is in CCM mode and switching at a virtually constant frequency.

Table 1 optimizes the inductor to output capacitor combination for maintaining a minimum phase margin of 45°.

Table 1. Maximum C_{OUT} vs. Inductor

Inductor	Minimum C_{OUT}	Recommended C_{OUT}	Maximum C_{OUT}
0.47µH	2.2µF	4.7µF	25µF
1.0µH	2.2µF	2.2µF	15µF
2.2µH	2.2µF	2.2µF	6.8µF

Duty Cycle

The typical maximum duty cycle of the MIC23156 is 80%.

Thermal Shutdown

When the internal die temperature of MIC23156 reaches 160°C, the internal driver is disabled until the die temperature falls below 140°C.

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied, as shown in Equation 2:

$$\text{Efficiency\%} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Eq. 2

There are two types of losses in switching converters: DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high-side switch during the on cycle. Power loss is equal to the high side MOSFET R_{DSON} multiplied by the switch current squared. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required driving the gates on and off at a constant 3MHz frequency and the switching transitions make up the switching losses.
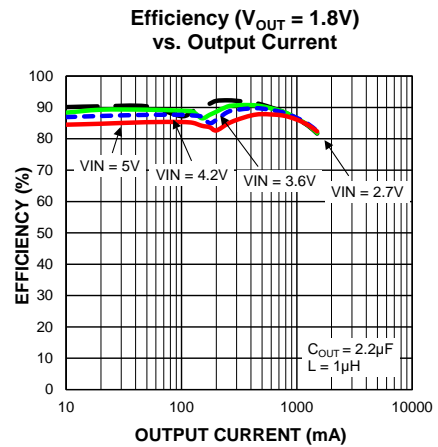

Figure 3. Efficiency under Load

Figure 3 shows an efficiency curve. From 10mA load to 1.5A, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By using the HyperLight Load mode, the MIC23156 is able to maintain high efficiency at low output currents.

Over 200mA, efficiency loss is dominated by MOSFET R_{DSON} and inductor losses. Higher input supply voltages will increase the gate-to-source threshold on the internal MOSFETs, thereby reducing the internal R_{DSON}. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as in Equation 3:

$$P_{DCR} = I_{OUT}^2 \times DCR$$

Eq. 3

From that, the loss in efficiency due to inductor resistance can be calculated as in Equation 4:

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} \times P_{DCR}} \right) \right] \times 100$$

Eq. 4

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a tradeoff between efficiency and size in this case.

HyperLight Load Mode

The MIC23156 uses a minimum on and off time proprietary control loop (patented by Micrel). When the output voltage falls below the regulation threshold, the error comparator begins a switching cycle that turns the PMOS on and keeps it on for the duration of the minimum-on-time. This increases the output voltage. If the output voltage is over the regulation threshold, then the error comparator turns the PMOS off for a minimum-off-time until the output drops below the threshold. The NMOS acts as an ideal rectifier that conducts when the PMOS is off. Using an NMOS switch instead of a diode allows for lower voltage drop across the switching device when it is on. The synchronous switching combination between the PMOS and the NMOS allows the control loop to work in discontinuous mode for light load operations. In discontinuous mode, the MIC23156 works in HyperLight Load to regulate the output. As the output current increases, the off time decreases, thus providing more energy to the output. This switching scheme improves the efficiency of MIC23156 during light load currents by only switching when it is needed. As the load current increases, the MIC23156 goes into continuous conduction mode (CCM) and switches at a frequency centered at 3MHz. The equation to calculate the load when the MIC23156 goes into continuous conduction mode may be approximated by Equation 5:

$$I_{LOAD} > \left(\frac{(V_{IN} - V_{OUT}) \times D}{2L \times f} \right)$$

Eq. 5

As shown in Equation 5, the load at which the MIC23156 transitions from HyperLight Load mode to PWM mode is a function of the input voltage (V_{IN}), output voltage (V_{OUT}), duty cycle (D), inductance (L) and frequency (f). As shown in Figure 4, as the output current increases, the switching frequency also increases until the MIC23156 goes from HyperLight Load mode to PWM mode at approximately 200mA. The MIC23156 will switch at a relatively constant frequency around 3MHz once the output current is over 200mA.
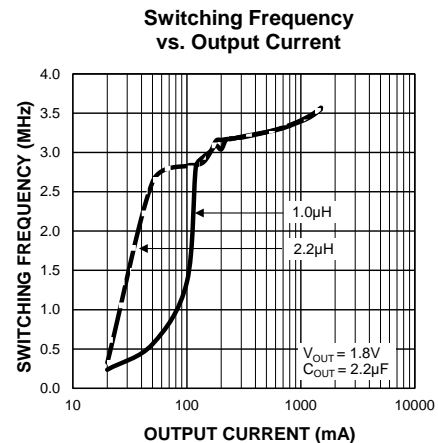

Figure 4. SW Frequency vs. Output Current

Output Voltage Setting

The MIC23156 features dynamic voltage scaling and setting hardware that allow the output voltage of the buck regulator to be changed on the fly in increments of 10mV. The output voltage is set according to one of two registers that behave identically; BUCK_OUT1 when VSEL = 0 and BUCK_OUT2 when VSEL = 1. If the BUCK_OUT value is changed while the VSEL is selected and regulator is enabled, then the output voltage will immediately change to the new value using dynamic voltage scaling (DVS). Equation 6 describes the relationship between the register value and the output voltage:

$$V_{OUT} = 0.7 + (0.01 \times REG_{BUCK\_OUT})$$

Eq. 6

Note that the maximum output voltage is 2.4V corresponding to a register setting of 170 (0b10101010, 0XAA). An example of this calculation is demonstrated in the Calculating DAC Voltage Code sub-section.
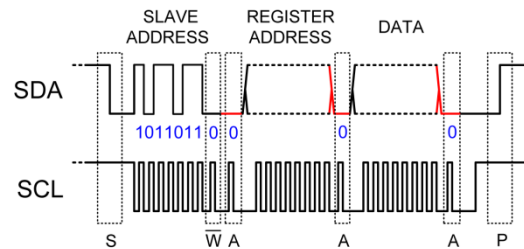
I²C Interface

Figure 5 shows the communications required for write and read operations via the I²C interface. The black lines show master communications and the red lines show the slave communications. During a write operation, the master must drive SDA and SCL for all stages except the acknowledgement (A) shown in red, which are provided by the slave (MIC23156).

The read operation begins first with a data-less write to select the register address from which to read. A restart sequence is issued followed by a read command and a data read.
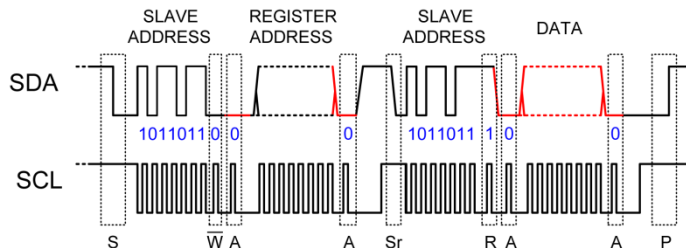
The MIC23156 responds to a slave address of hex 0xB6 and 0xB7 for write and read operations respectively, or binary 1011011X (where X is the read/write bit, 0 = write, 1 = read).

The register address is eight bits wide and carries the address of the MIC23156 register to be operated upon. Only the lower three bits are used.

WRITE PROTOCOL

READ PROTOCOL

S = START   Sr = RESTART
W̄ = WRITE   R = READ
A = ACKNOWLEDGE   P = STOP

Figure 5. Required Communications for Read/Write Operations via I²C Interface

I²C Register Summary

There are three I²C read/write registers of 8-bit length. All registers are reset to a zero state whenever EN ≤ 0.5V and set (reset) to their default values on the transition of EN ≥ 1.5V. All registers are accessible by I²C.

Table 2. Register Bit Field Map

Reg.	D7	D6	D5	D4
1		TSD	UVLO	PGOOD
2	BUCK_OUT1			
3	BUCK_OUT2			
Reg.	**D3**	**D2**	**D1**	**D0**
1			SSL	BUCK_EN
2	BUCK_OUT1			
3	BUCK_OUT2			

Enable/Status Register (001b/01h)

Enable/Status register is written to enable the output regulator (BUCK_EN) and soft start extension mode (SSL). It is read to interrogate the status of thermal shutdown (TSD), undervoltage lockout (UVLO), and power good (PGOOD) status of the regulator. See Table 3 for additional information.

Buck Register 1 (010b/02h) and Buck Register 2 (011b/03h)

These registers are written to set the output voltage to any one of 170 levels in 10mV steps. Values above decimal 170 are equivalent to setting the register to 170. The two registers correspond to one of two states, which is selectable by the VSEL input pin, which allow the regulator to be quickly switched between two voltage levels (e.g. enabled and standby). When VSEL = 0, the output voltage is controlled by BUCK_OUT1 (REG2). When VSEL = 1, then the output voltage is controlled by BUCK_OUT2 (REG3). See Table 4 and Table 5 for additional information.

Table 3. Enable and Status Register (REG1) Bit Field Description

Bits	Name	R/W	POR	Description
7	Reserved	R	0	
6	TSD	R	0	Thermal shutdown status bit. This register bit will be set by internal hardware if a thermal shutdown event is triggered by the die temperature exceeding shutdown temperature.
5	UVLO	R	0	Undervoltage lockout status bit. This register bit will be set by internal hardware when the under voltage lockout circuit is active, and cleared when V_{IN} exceeds the UVLO threshold.
4	PGOOD	R	0	Power good status bit. This register will be set when the buck regulator output voltage is > nominally 10% of the output voltage set points as specified by VSEL, BUCK_OUT1 and BUCK_OUT2. This regulator has the same function as the PGOOD output pin.
3:2	Reserved	R/W	00	
1	SSL	R/W	0	Long soft-start enable bit. If this bit is set, then the internal soft start resistor is increased and the soft start time will be extended.
0	BUCK_EN	R/W	1	Buck regulator enable bit. Setting this bit will enable and turn on the buck regulator output. Clearing this bit will disable the buck regulator output.

Table 4. BUCK_OUT1 (REG2) Bit Field Description

| Bits	Name	R/W	POR	Description
7:0	BUCK_OUT1	R/W	0X1E	Buck output voltage 1 setting for VSEL = 0. Setting this register value will change the output regulation point for the buck regulator when VSEL = 0. If the buck is enabled and VSEL = 0, changing the value will immediately cause the output voltage to transition to the new set point.

Table 5. BUCK_OUT2 (REG3) Bit Field Description

Bits	Name	R/W	POR	Description
7:0	BUCK_OUT2	R/W	0X0A	Buck output voltage 2 setting for VSEL = 1. Setting this register value will change the output regulation point for the buck regulator when VSEL = 1. If the buck is enabled and VSEL = 1, changing the value will immediately cause the output voltage to transition to the new set point .

Calculating DAC Voltage Code

If the desired output voltage is 1.8V, then using Equation 6:

$$V_{OUT} = 0.7 + \left(0.01 \times REG_{BUCK\_OUT}\right) \rightarrow REG_{BUCK\_OUT} = \frac{(1.8 - 0.7)}{0.01}$$

$\rightarrow REG_{BUCK\_OUT}$ = 110 in decimal, 6E in hex, or 0110 1110 in binary

Evaluation Board Schematic − MIC23156-0YML
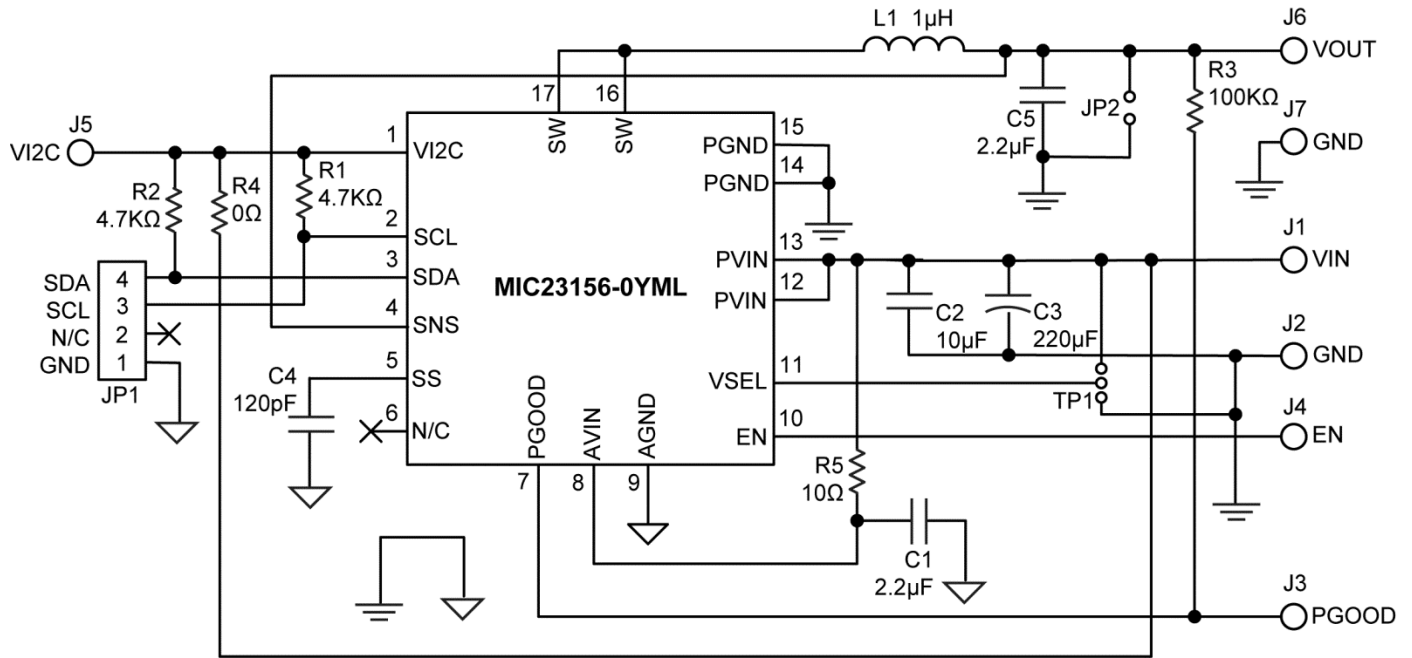
Bill of Materials

| Item	Part Name	Manufacturer	Description	Qty.
C1, C5	06036D225KAT2A	AVX[1]	2.2µF, 6.3V, X5R, 0603	2
	GRM188R60J225KE19D	Murata[2]		
	C1608X5R0J225KT	TDK[3]		
C2	06036D106MAT2A	AVX	10µF, 6.3V, X5R, 0603	1
	GRM188R60J106ME47D	Murata		
	C1608X5R0J106M	TDK		
C3	ECA-1AHG221	Panasonic[4]	Aluminum capacitor, 220µF, 10V, 20%, radial	1
C4	06035A121JAT2A	AVX	120pF, 50V, 0603	1
	GRM1885C1H121JA01D	Murata		
	C1608C0G1H121JT	TDK		
L1	CDRH4D28CLDNP-1R0P	Sumida[5]	1µH, 3.0A, 14mΩ, L5.1mm × W5.1mm × H3.0mm	1
	LQH44PN1R0NJ0	Murata	1µH, 2.0A, 48mΩ, L4.0mm × W4.0mm × H1.1mm	
R1, R2	CRCW06034K70FKEA	Vishay/Dale[6]	4.7KΩ, 1%, 1/10W, 0603	2
R3	CRCW06031003FKEA	Vishay/Dale	100KΩ, 1%, 1/10W, 0603	1
R4	CRCW06030000Z0EA	Vishay/Dale	0Ω, 1/10W, 0603	1
R5	CRCW060310R0FKEA	Vishay/Dale	10Ω, 1%, 1/10W, 0603	1
U1	**MIC23156-0YML**	**Micrel, Inc.[7]**	**1.5A, 3MHz Synchronous Buck Regulator with HyperLight Load and I²C Control for Dynamic Voltage Scaling**	**1**

Notes:

1. AVX: www.avx.com.
2. Murata: www.murata.com.
3. TDK: www.tdk.com.
4. Panasonic: www.industrial.panasonic.com.
5. Sumida: www.sumida.com.
6. Vishay: www.vishay.com.
7. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations (MLF Package)

Top Layer

Bottom Layer
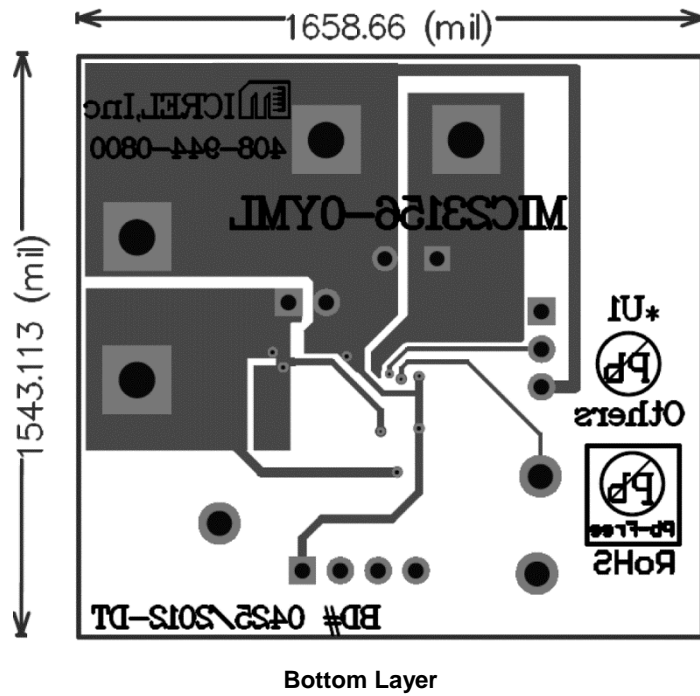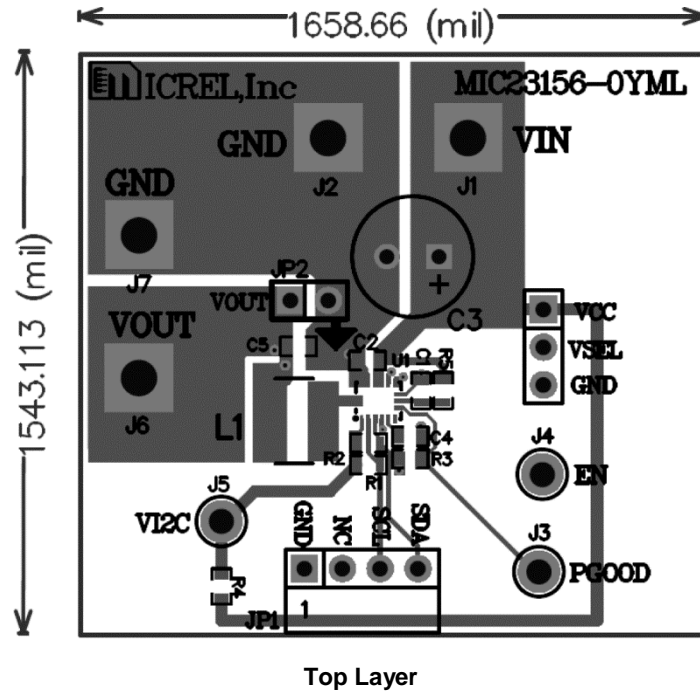
Package Information[1] and Recommended Landing Pattern (MLF Package)

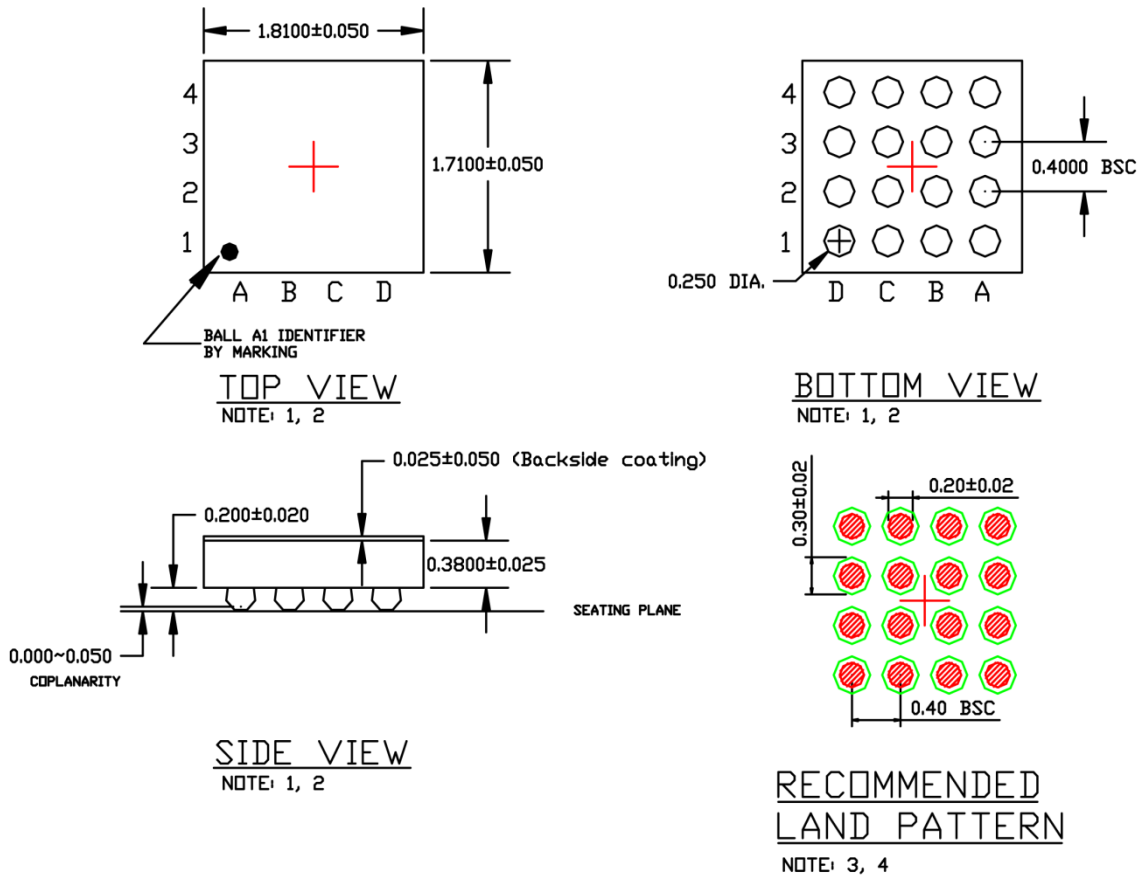TOP VIEW

BOTTOM VIEW

SIDE VIEW

RECOMMENDED LAND PATTERN
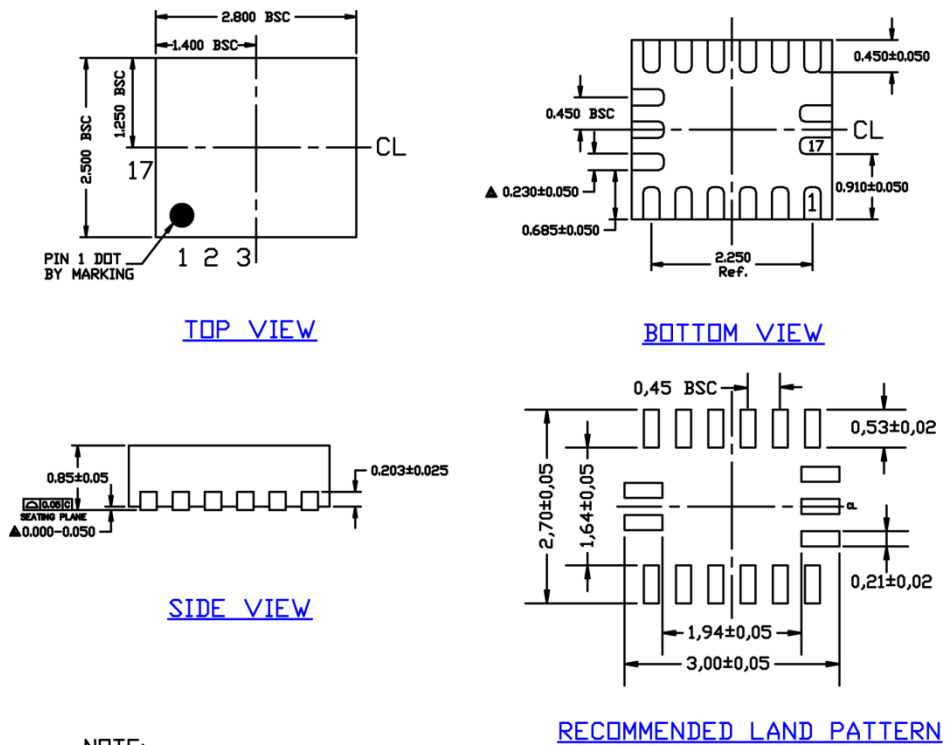
NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED
    BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.

17-Pin 2.8mm × 2.5mm MLF

Note:

1. Package information is correct as of the publication date. For updates and the most current information, go to www.micrel.com.

Package Information[1] and Recommended Landing Pattern (WLCSP Package)

1.8100±0.050

1.7100±0.050

4
3
2
1

A B C D

BALL A1 IDENTIFIER
BY MARKING

TOP VIEW
NOTE: 1, 2

4
3
2
1

D C B A

0.4000 BSC

0.250 DIA.

BOTTOM VIEW
NOTE: 1, 2

0.025±0.050 (Backside coating)

0.200±0.020

0.3800±0.025

SEATING PLANE

0.000~0.050
COPLANARITY

SIDE VIEW
NOTE: 1, 2

0.30±0.02

0.20±0.02

0.40 BSC

RECOMMENDED
LAND PATTERN
NOTE: 3, 4

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. NON-SOLDERMASK DEFINED PADS ARE RECOMMENDED FOR BOARD LAYOUT
4. SHADED RED CIRCLES REPRESENT CONTACT PAD AREA. GREEN CIRCLES REPRESENT
SOLDER MASK OPENING

16-Ball 1.81mm × 1.71mm WLCSP

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